HIGH ISOLATION X-SPDT (DP4T) SWITCH GaAs MMIC

■ GENERAL DESCRIPTION

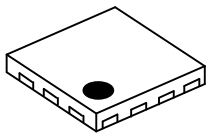
The NJG1690MD7 is a GaAs X (cross)-SPDT(DP4T) switch MMIC for switching of balanced (differential) dual band filters. It features low insertion loss and very high isolation for balanced signal input which makes it much suited for balanced filter switching.

The ESD protection circuit are integrated in the IC to achieve high ESD tolerance.

The ultra-small and ultra-thin EQFN14-D7 package is adopted.

*) X-SPDT is a paired SPDT switch controlled synchronously. The X-SPDT includes two SPDT switches whose RF lines have a crossing inside the chip.

■ PACKAGE OUTLINE



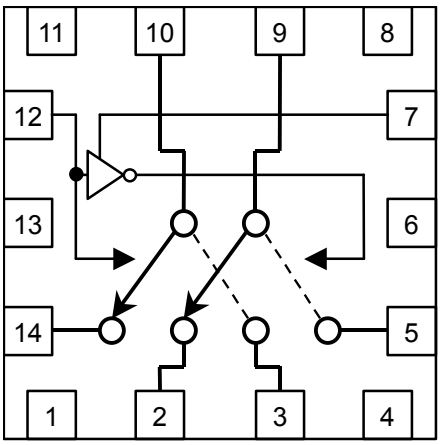
NJG1690MD7

■ FEATURES

- Low operation voltage V_{DD} =1.5~4.5V
- Low control voltage $V_{CTL(H)}$ =1.8V typ.
- High isolation
  - 37dB typ. @f=2.7GHz, P_{IN}=0dBm (with balanced mode operation)
  - 29dB typ. @f=1.0GHz, P_{IN}=0dBm
  - 24dB typ. @f=2.0GHz, P_{IN}=0dBm
  - 21dB typ. @f=2.7GHz, P_{IN}=0dBm
- Low insertion loss
  - 0.3dB typ. @f=1.0GHz, P_{IN}=0dBm
  - 0.4dB typ. @f=2.0GHz, P_{IN}=0dBm
  - 0.45dB typ. @f=2.7GHz, P_{IN}=0dBm
- Small and thin package EQFN14-D7 (Package size: 1.6x1.6x0.397mm typ.)
- RoHS compliant and Halogen Free
- MSL: 1

■ PIN CONFIGURATION

(Top View)



Pin connection

1. GND	10. PC1
2. PA2	11. GND
3. PB1	12. VCTL
4. GND	13. GND
5. PB2	14. PA1
6. GND	
7. VDD	
8. GND	
9. PC2	

■ TRUTH TABLE

"H"=$V_{CTL(H)}$, "L"=$V_{CTL(L)}$

ON PATH	VCTL
PC1-PA1, PC2-PA2	H
PC1-PB1, PC2-PB2	L

NOTE: Please note that any information on this catalog will be subject to change.

■ ABSOLUTE MAXIMUM RATINGS

(T_a=+25°C, Z_s=Z_l=50Ω)

PARAMETER	SYMBOL	CONDITIONS	RATINGS	UNITS
RF input power	P_{IN}	V_{DD} =2.7V, VCTL=0V/1.8V	28	dBm
Supply voltage	V_{DD}		5.0	V
Control voltage	V_{CTL}		5.0	V
Power dissipation	P_D	Four-layer FR4 PCB with through-hole (74.2x74.2mm), Tj=150°C	1300	mW
Operating temp.	T_{opr}		-40~+85	°C
Storage temp.	T_{stg}		-55~+150	°C

■ ELECTRICAL CHARACTERISTICS

(General conditions: T_a=+25°C, Z_s=Z_l=50Ω, V_{DD}=2.7V, $V_{CTL(L)}$=0V, $V_{CTL(H)}$=1.8V, with application circuit1)

PARAMETERS	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply voltage	V_{DD}		1.5	2.7	4.5	V
Operating current	I_{DD}	P_{IN}=0dBm	-	16	30	μA
Control voltage (LOW)	$V_{CTL(L)}$		0	-	0.4	V
Control voltage (HIGH)	$V_{CTL(H)}$		1.3	1.8	4.5	V
Control current	I_{CTL}	f=2GHz, P_{IN}=0dBm	-	5	10	μA
Insertion loss 1	LOSS1	f=1GHz, P_{IN}=0dBm	-	0.30	0.45	dB
Insertion loss 2	LOSS2	f=2GHz, P_{IN}=0dBm	-	0.40	0.55	dB
Insertion loss 3	LOSS3	f=2.7GHz, P_{IN}=0dBm	-	0.45	0.65	dB
Balanced mode isolation *Note1	B-ISL	PC-PA (PC-PB ON) PC-PB (PC-PA ON) f=2.7GHz, P_{IN}=0dBm	33	37	-	dB
Isolation 1	ISL1	PC1-PA1, PC2-PA2 PC1-PB1, PC2-PB2 f=1GHz, P_{IN}=0dBm	27	29	-	dB
Isolation 2	ISL2	PC1-PA1, PC2-PA2 PC1-PB1, PC2-PB2 f=2GHz, P_{IN}=0dBm	21	24	-	dB
Isolation 3	ISL3	PC1-PA1, PC2-PA2 PC1-PB1, PC2-PB2 f=2.7GHz, P_{IN}=0dBm	18	21	-	dB
Isolation 4	ISL4	PC1-PC2 port f=2GHz, P_{IN}=0dBm	22	25	-	dB

Note1:

The balanced mode isolation is a unique specification for isolation defined under the condition where the X-SPDT switch is used in balanced mode operation as shown in application circuit2.

The NJG1690MD7 is designed so that the isolation in the balanced mode operation is much higher than the isolation in the single-ended mode operation.

■ ELECTRICAL CHARACTERISTICS

(General conditions: T_a=+25°C, Z_s=Z_l=50Ω, V_{DD}=2.7V, $V_{CTL(L)}$=0V, $V_{CTL(H)}$=1.8V, with application circuit1)

PARAMETERS	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input power at 0.2dB compression point	$P_{-0.2dB}$	f=2GHz	20	24	-	dBm
VSWR	VSWR	f=2GHz, On port	-	1.2	1.4	
Switching time	T_{SW}	50% CTL to 10%/90% RF	-	1.5	5.0	μs

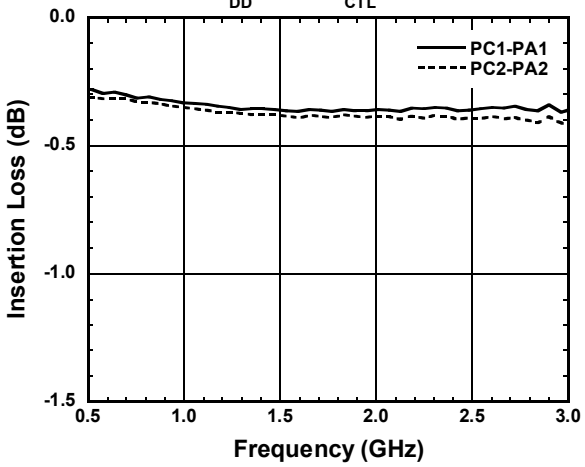
■ TERMINAL INFORMATION

No.	SYMBOL	DESCRIPTION
1	GND	Ground terminal. Please connect this terminal with ground plane as close as possible for good RF performance.
2	PA2	This port is connected to PC2 terminal by applying High-level (1.3~4.5V) at VCTL terminal. An external capacitor is required to block DC voltage of internal circuit.
3	PB1	This port is connected to PC1 terminal by applying Low-level (0~0.4V) at VCTL terminal. An external capacitor is required to block DC voltage of internal circuit.
4	GND	Ground terminal. Please connect this terminal with ground plane as close as possible for good RF performance.
5	PB2	This port is connected to PC2 terminal by applying Low-level (0~0.4V) at VCTL terminal. An external capacitor is required to block DC voltage of internal circuit.
6	GND	Ground terminal. Please connect this terminal with ground plane as close as possible for good RF performance.
7	VDD	A supply voltage terminal (1.5~4.5V). Please place a bypass capacitor between this terminal and GND for avoiding RF noise from outside.
8	GND	Ground terminal. Please connect this terminal with ground plane as close as possible for good RF performance.
9	PC2	Common RF port. This port is connected with either of PA2 or PB2. An external capacitor is required to block DC voltage of internal circuit.
10	PC1	Common RF port. This port is connected with either of PA1 or PB1. An external capacitor is required to block DC voltage of internal circuit.
11	GND	Ground terminal. Please connect this terminal with ground plane as close as possible for good RF performance.
12	VCTL	Control signal input terminal. This terminal is set to high-level (1.3V~4.5V) or low-level (0~0.4V).
13	GND	Ground terminal. Please connect this terminal with ground plane as close as possible for good RF performance.
14	PA1	This port is connected to PC1 terminal by applying High-level (1.3~4.5V) at VCTL terminal. An external capacitor is required to block DC voltage of internal circuit.

■ **ELECTRICAL CHARACTERISTICS** (With Application circuit1, Loss of external circuit are excluded)

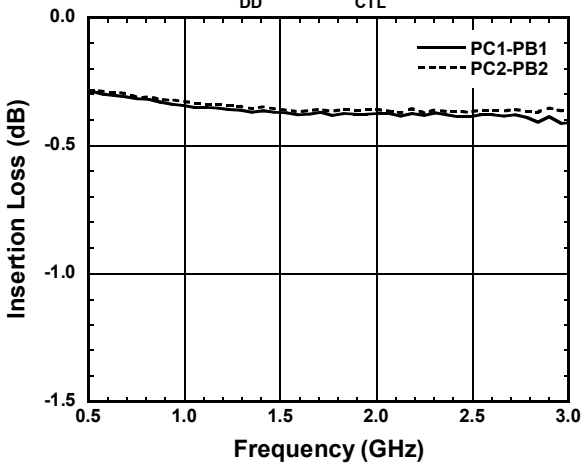
Insertion Loss vs. Frequency

(V_{DD}=2.7V, V_{CTL}=1.8V)



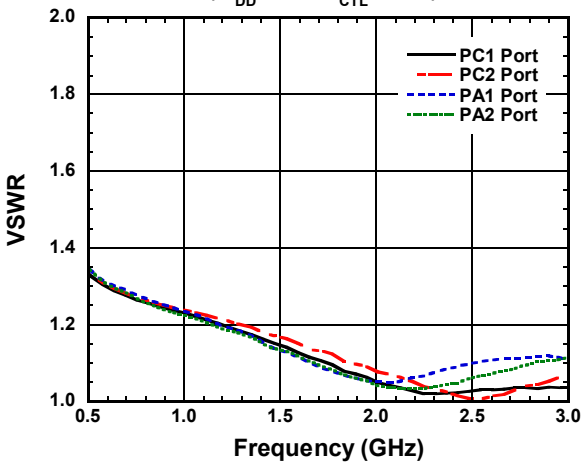
Insertion Loss vs. Frequency

(V_{DD}=2.7V, V_{CTL}=0V)



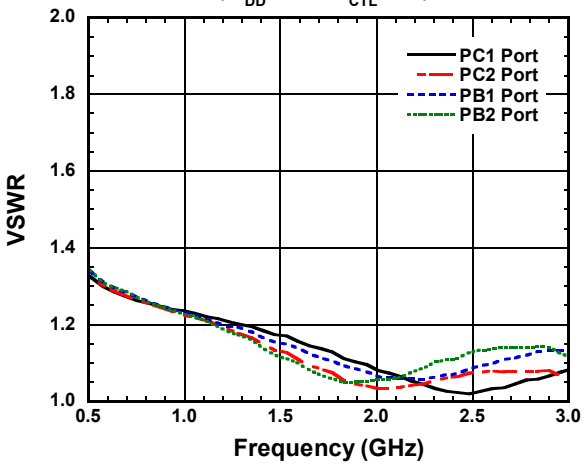
VSWR vs. Frequency

(V_{DD}=2.7V, V_{CTL}=1.8V)



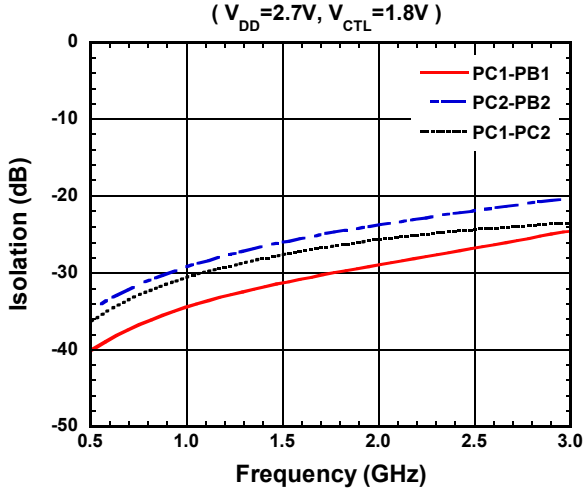
VSWR vs. Frequency

(V_{DD}=2.7V, V_{CTL}=0V)



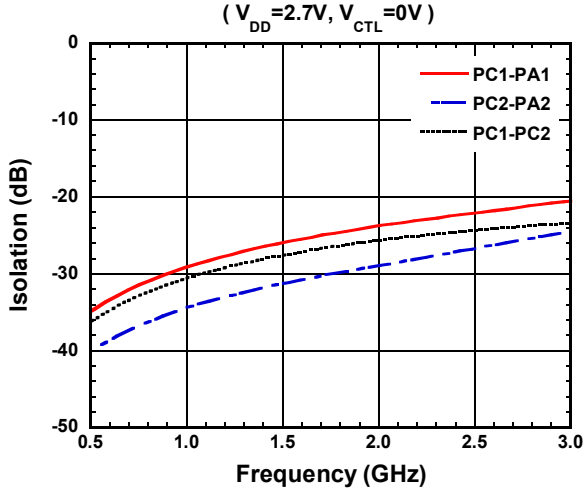
Isolation vs. Frequency

(V_{DD}=2.7V, V_{CTL}=1.8V)



Isolation vs. Frequency

(V_{DD}=2.7V, V_{CTL}=0V)

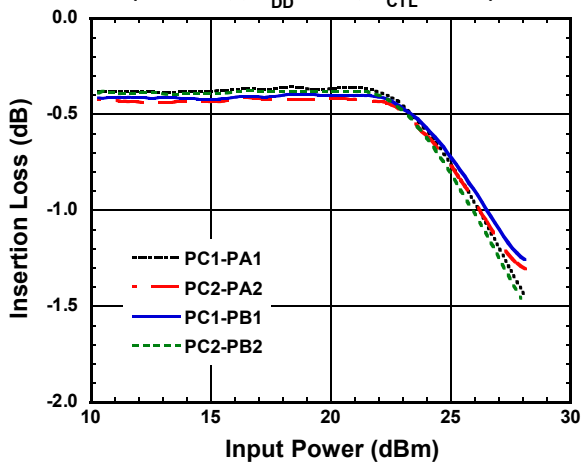


■ ELECTRICAL CHARACTERISTICS

(With Application circuit1 and 2, Loss of external circuit are excluded)

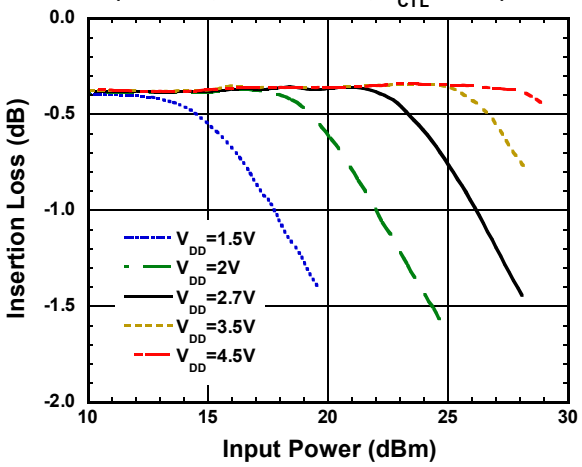
Insertion Loss vs. Input Power

(f=2GHz, , V_{DD}=2.7V, V_{CTL}=1.8V)



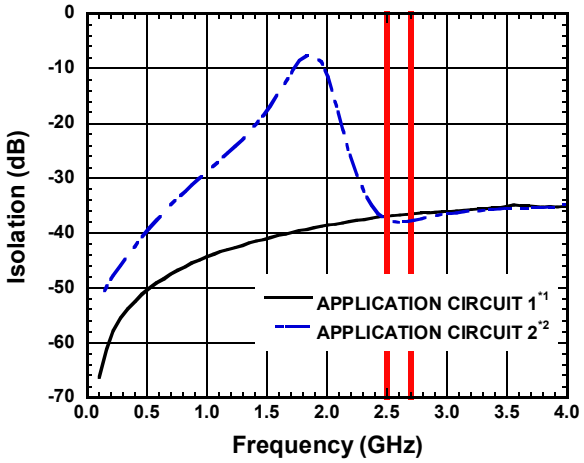
Insertion Loss vs. Input Power

(f=2GHz, PC1-PA1 ON, V_{CTL}=1.8V)



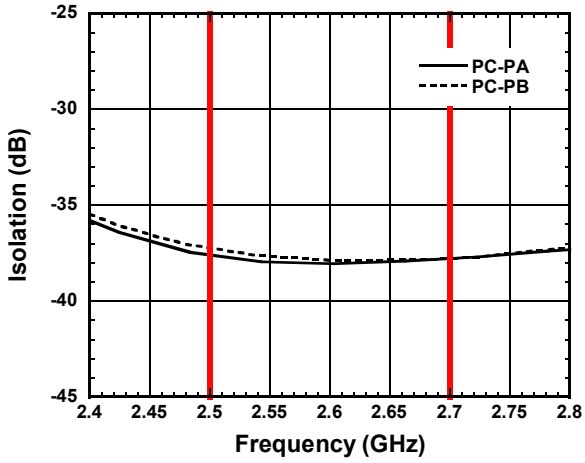
Balanced Mode Isolation vs. Frequency

(Broad band)



Balanced Mode Isolation vs. Frequency

(With Application Circuit 2)



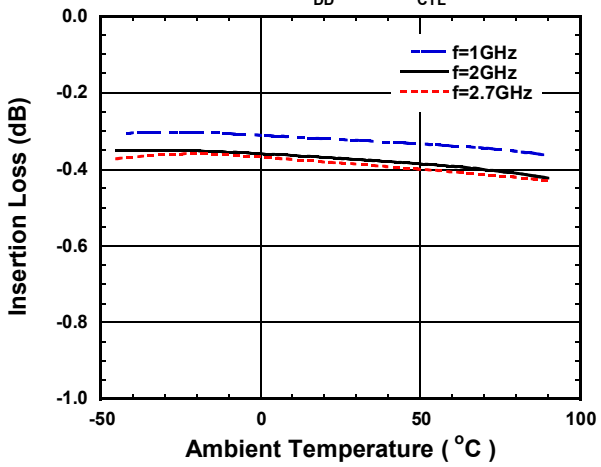
*1) The balanced mode isolation measured with the application circuit1.

*2) The balanced mode isolation measured with the application circuit2 having single-ended interfaces and baluns.

■ **ELECTRICAL CHARACTERISTICS** (With Application circuit1, Loss of external circuit are excluded)

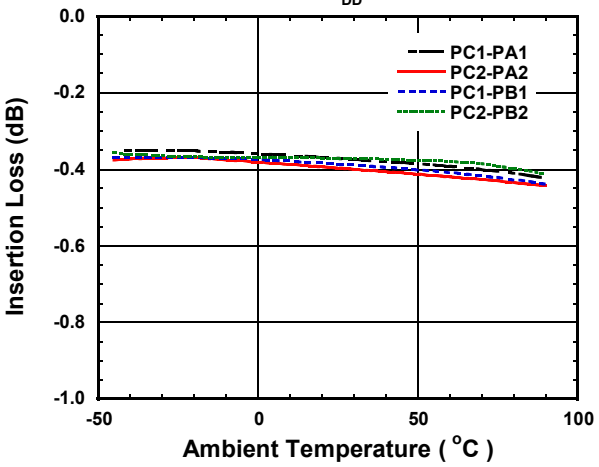
Insertion Loss vs. Ambient Temperature

(PC1-PA1 ON, V_{DD}=2.7V, V_{CTL}=1.8V)



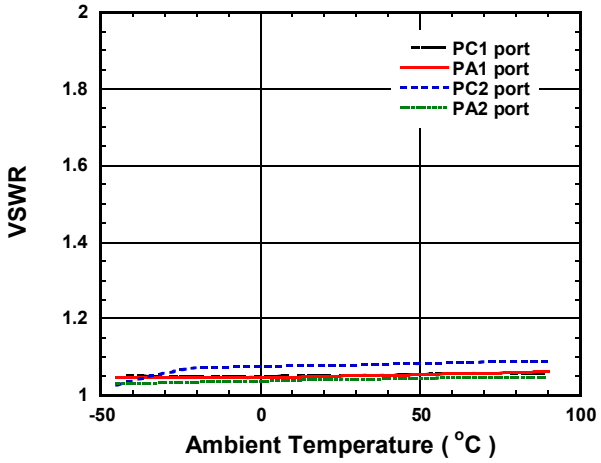
Insertion Loss vs. Ambient Temperature

(f=2GHz, V_{DD}=2.7V)



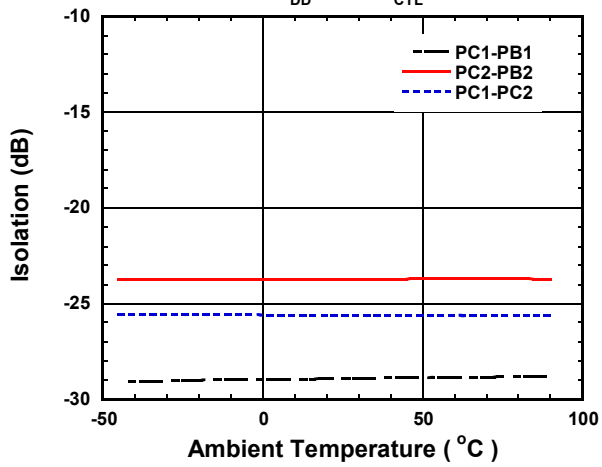
VSWR vs. Ambient Temperature

(f=2GHz, V_{DD}=2.7V, V_{CTL}=1.8V)



Isolation vs. Ambient Temperature

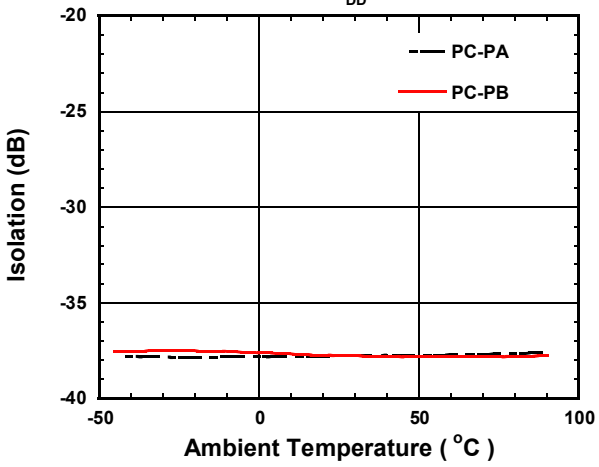
(f=2GHz, V_{DD}=2.7V, V_{CTL}=1.8V)



■ **ELECTRICAL CHARACTERISTICS** (With Application circuit1, Loss of external circuit are excluded)

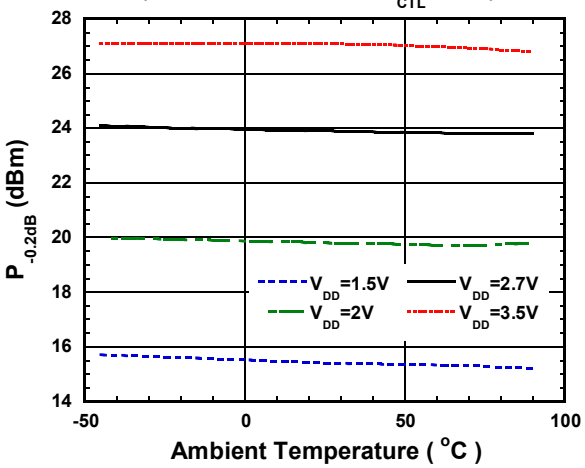
Balanced Mode Isolation vs. Temperature

(f=2.7GHz, V_{DD}=2.7V)



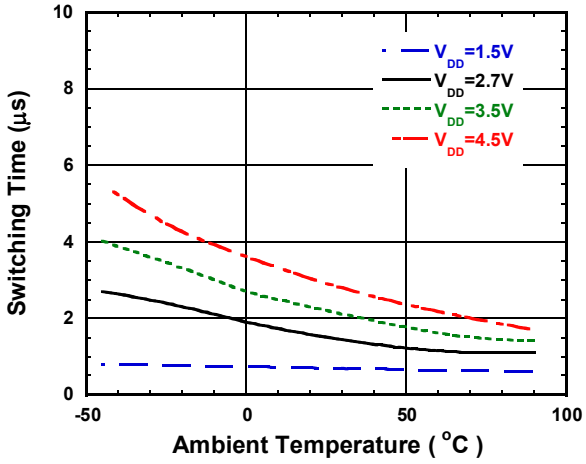
$P_{-0.2dB}$ vs. Ambient Temperature

(f=2GHz, PC1-PA1 ON, V_{CTL}=1.8V)



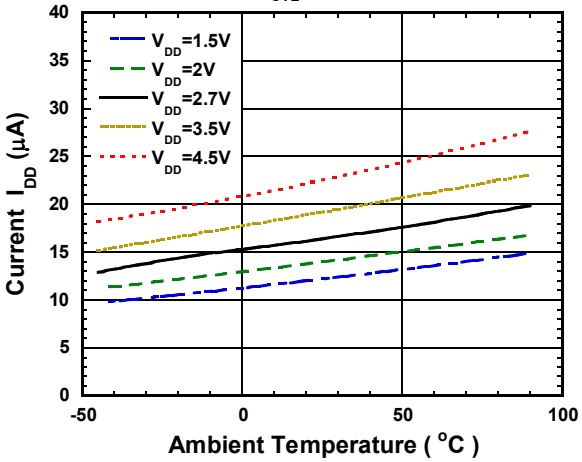
Switching Time vs. Ambient Temperature

(f=2GHz, PC1-PA1 ON)

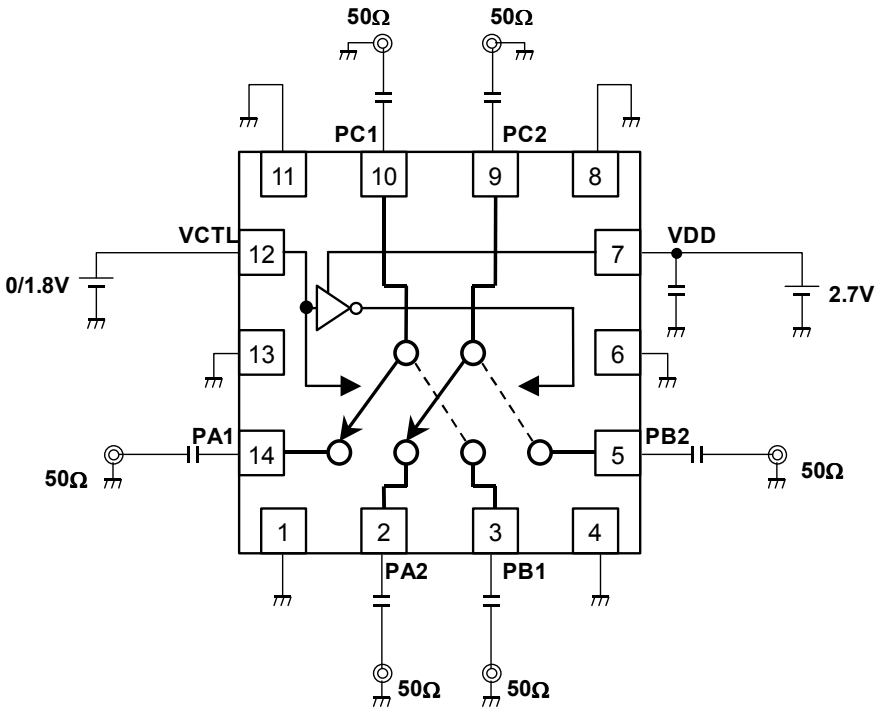


Current I_{DD} vs. Temperature

(V_{CTL}=1.8V)

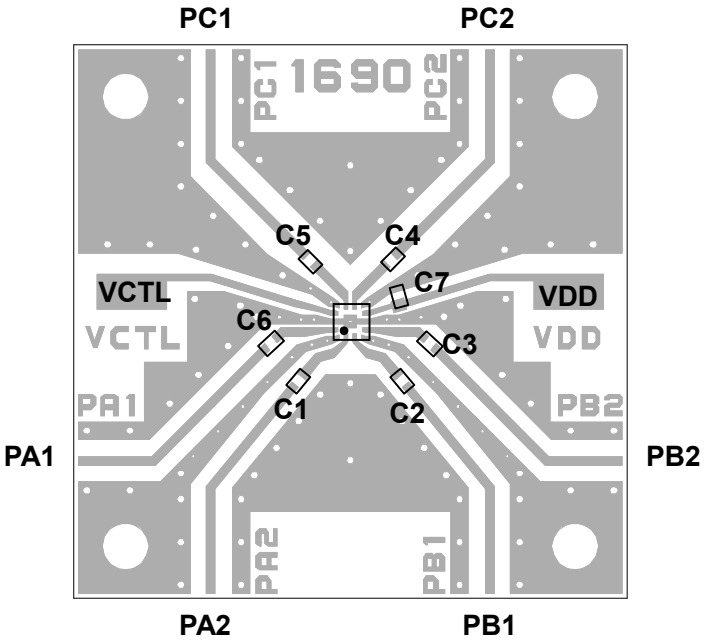


■ APPLICATION CIRCUIT 1 (Unbalanced mode)



■ PCB LAYOUT 1

(TOP VIEW)



PCB:	FR-4, t=0.2mm
Capacitor Size:	1005
Strip Line Width:	0.4mm
PCB Size:	26 x 26mm

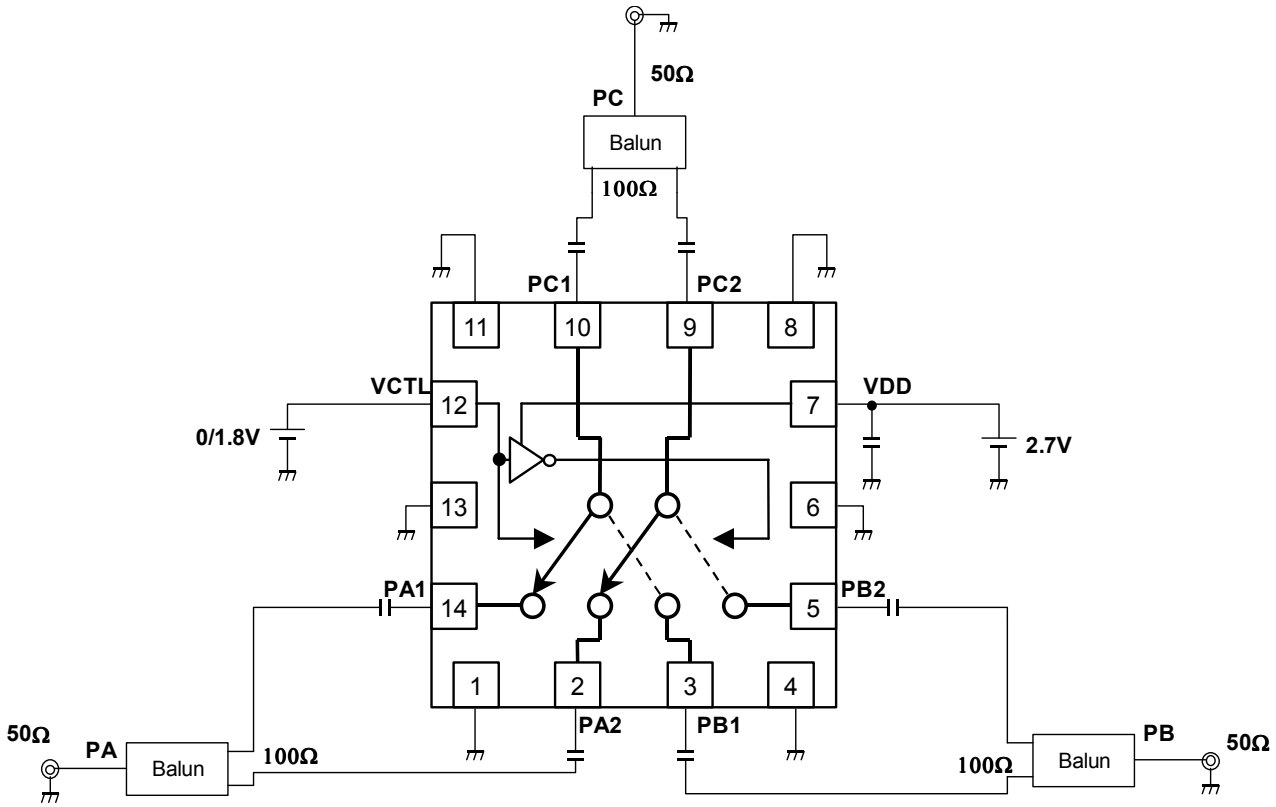
Losses of PCB, capacitors and connectors

Frequency (GHz)	Loss (dB)
1	0.35
2	0.54
2.7	0.68

■ PARTS LIST 1

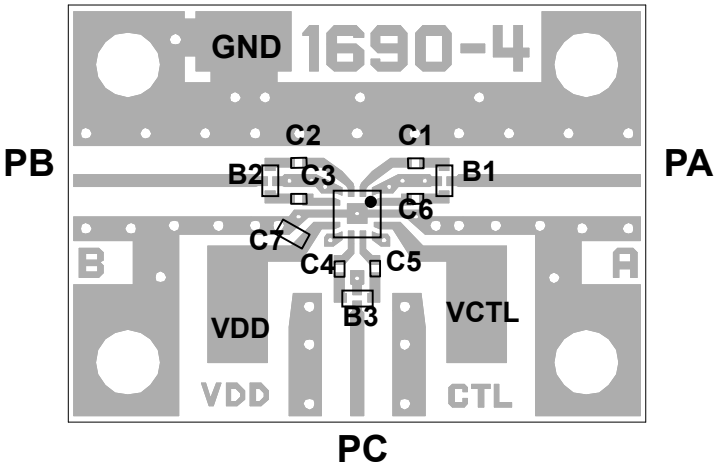
PART ID	Value	COMMENT
C1~C6	56pF	MURATA (GRM15)
C7	1000pF	MURATA (GRM15)

■ APPLICATION CIRCUIT 2 (BALANCED MODE)



■ PCB LAYOUT 2

(TOP VIEW)



PCB: FR-4, t=0.2mm
Capacitor Size: 0603, 1005
Strip Line Width: 0.4mm
PCB Size: 19.4 x 14mm

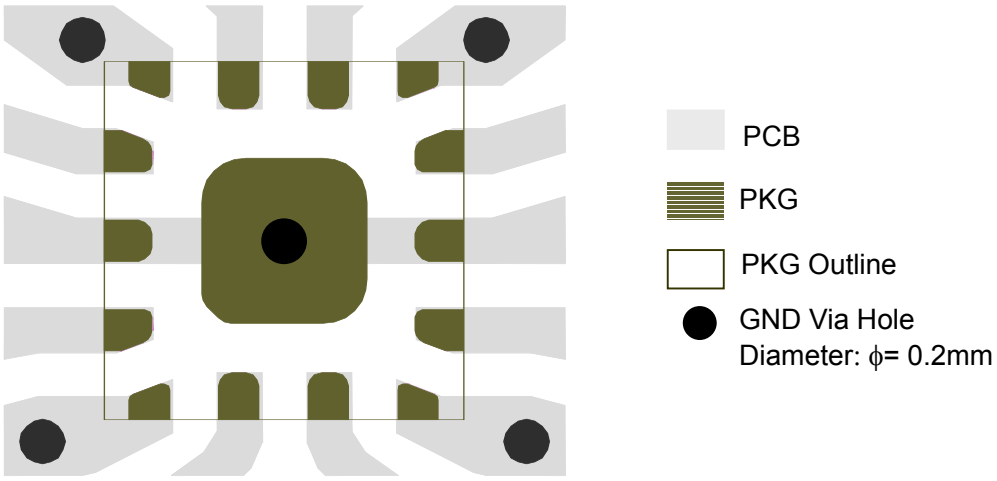
Losses of PCB, capacitors, connectors and baluns

Frequency (GHz)	Loss (dB)
2.7	0.93

■ PARTS LIST 2

PART ID	Value	COMMENT
C1~C6	56pF	MURATA (GRM03)
C7	1000pF	MURATA (GRM15)
B1~B3	2500MHz band	Balun TDK-EPC HHM1903A1

■ PCB LAYOUT FOR EQFN14-D7



■ PRECAUTIONS

[1] For good RF performance, all GND terminals must be connected to PCB ground plane of substrate, and via-holes for GND should be placed near the IC.

[2] For good RF performance, through-holes for GND should be placed close to the GND pin 6 and pin 13. One of the ways to do this is to place a via-hole at the TAB pad under this IC.

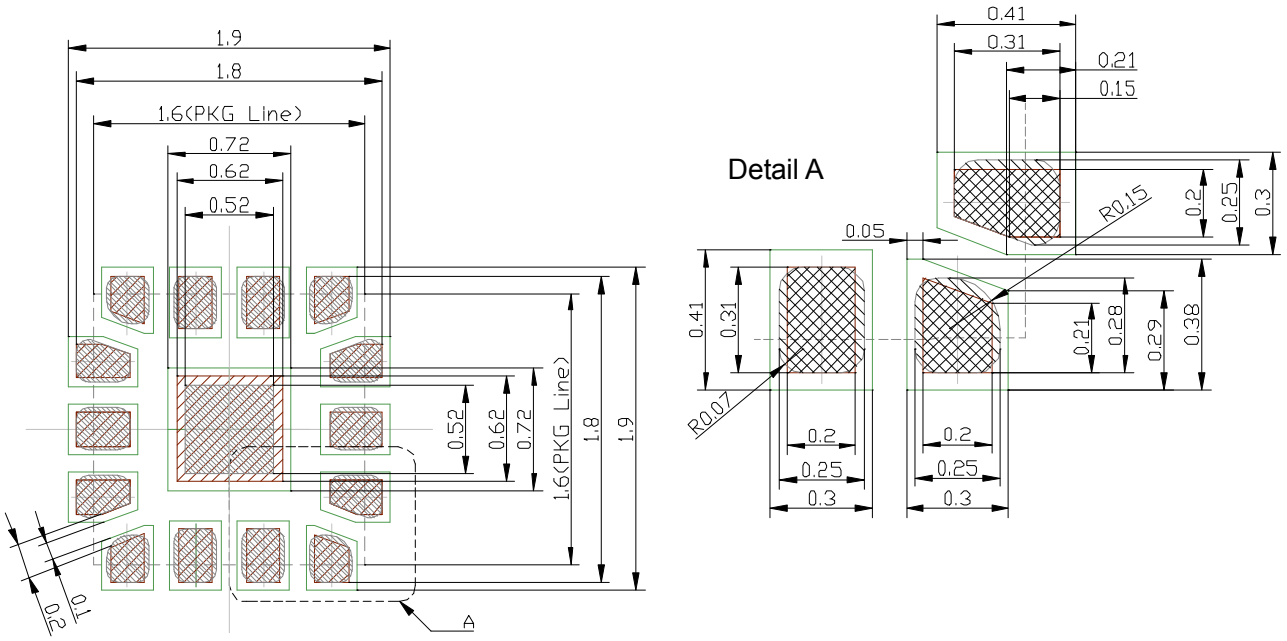
■ RECOMMENDED FOOTPRINT PATTERN (EQFN14-D7 PACKAGE Reference)

:Land

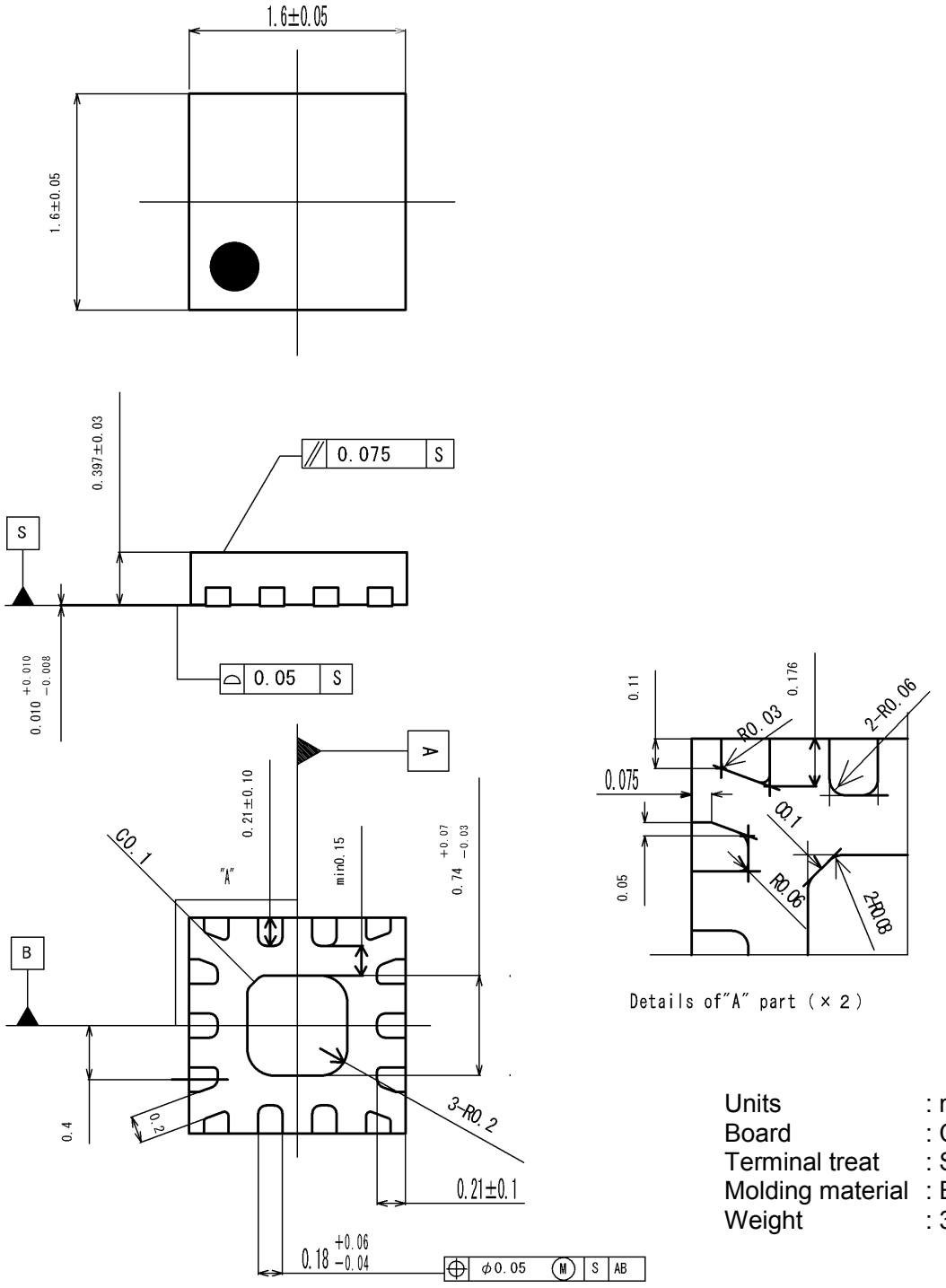
:Mask (Open area) *Metal mask thickness : 100μm

:Resist(Open area)

PKG: 1.6mm x 1.6mm
Pin pitch: 0.4mm



■ PACKAGE OUTLINE (EQFN14-D7)



Units	: mm
Board	: Cu
Terminal treat	: SnBi
Molding material	: Epoxy resin
Weight	: 3.4mg

Cautions on using this product

This product contains Gallium-Arsenide (GaAs) which is a harmful material.

- Do NOT eat or put into mouth.
- Do NOT dispose in fire or break up this product.
- Do NOT chemically make gas or powder with this product.
- To waste this product, please obey the relating law of your country.

This product may be damaged with electric static discharge (ESD) or spike voltage. Please handle with care to avoid these damages.