JUN 15 1992

P54/74FCT841A/B – (P54/74PCT841A/B) P54/74FCT843A/B – (P54/74PCT843A/B) BUS INTERFACE LATCHES

FEATURES

- Function, Pinout and Drive Compatible with the FCT, F and AM29841/843 Logic
- FCT-A speed at 9.0ns max. (Com'l)
  FCT-B speed at 6.5ns max. (Com'l)
- CMOS V_{OH} Levels for Low Power Consumption
  —— Typically 1/3 of FAST Bipolar Logic
- Edge-rate Control Circuitry for Significantly Improved Noise Characteristics
- ESD protection exceeds 2000V
- Inputs and Outputs Interface Directly with TTL,NMOS and CMOS Devices
- Outputs Meet Levels Required for CMOS Static RAM Low Power Standby Mode
- 48 mA Sink Current (Com'l), 32 mA (Mil)
  15 mA Source Current (Com'l), 12 mA (Mil)
- Buffered Common Clear and Preset Input
- High Speed Parallel Latches
- Buffered Common Latch Enable Input
- Manufactured in 0.8 micron PACE Technology™

DESCRIPTION

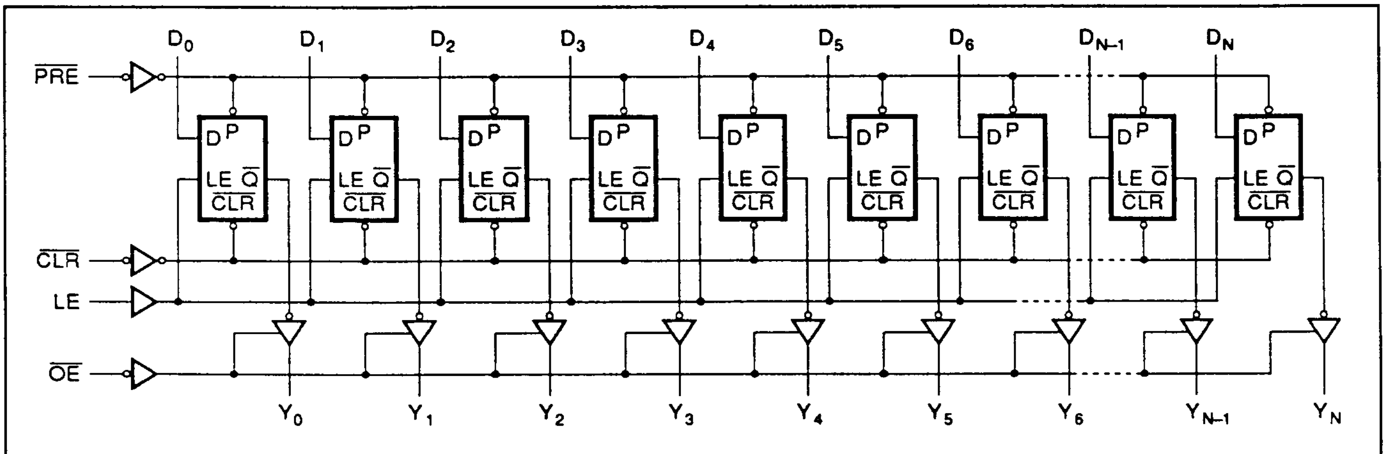
The 'FCT840 series bus interface latches are designed to eliminate the extra packages required to buffer existing latches and provide extra data width for wider address/data paths or buses carrying parity. The 'FCT841 is a buffered 10-bit wide version of the 'FCT373 function. The 'FCT843 is a 9-bit wide buffered latch with Preset ($\overline{PRE}$) and Clear ($\overline{CLR}$) controls making it ideal for parity bus interfacing in high-performance systems.

The 'FCT800 high performance interface family is designed for high-capacitance load drive capability while providing low-capacitance bus loading at both inputs and outputs. All inputs have clamp diodes and all outputs are designed for low-capacitance bus loading in the high impedance state.

The 'FCT840 interface family are manufactured using PACE Technology which is Performance Advanced CMOS Engineered to use 0.7 micron effective channel lengths giving 400 picosecond loaded* internal gate delays. PACE Technology includes two-level metal and epitaxial substrates. In addition to very high performance and very high density, the technology features latch-up protection, single event upset protection, and is supported by a Class 1 environment volume production facility.

* For a fan-in/fan-out of 4, at 85°C junction temperature and 5.0V.

FUNCTIONAL BLOCK DIAGRAM



'FCT843

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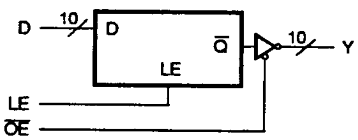
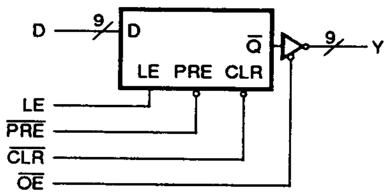
LOGIC SYMBOLS

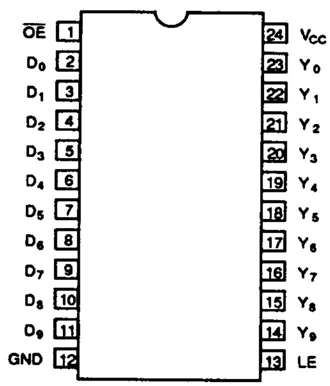
'FCT841 (10-Bit Latch)



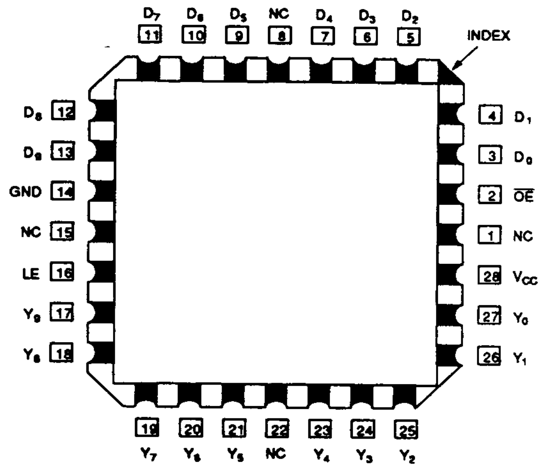
'FCT843 (9-Bit Latch)



PIN CONFIGURATONS

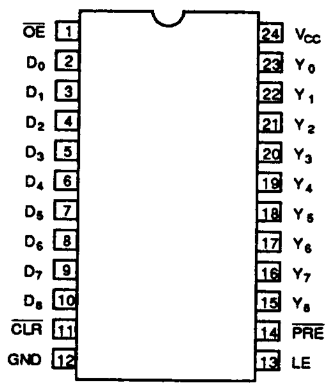


DIP (D4,P4)
SOIC (S4)

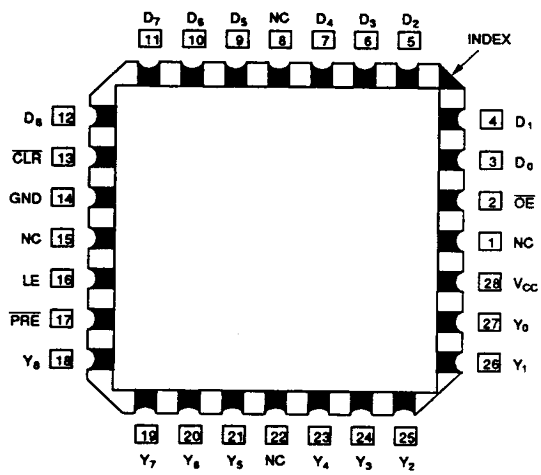


LCC (L5-1)

1564 02



DIP (D4,P4)
SOIC (S4)



LCC (L5-1)

1564 03

PIN DESCRIPTION

Name	I/O	Description
$\overline{CLR}$	I	When $\overline{CLR}$ is low, the outputs are LOW if $\overline{OE}$ is LOW. When $\overline{CLR}$ is HIGH, data can be entered into the latch.
D_1	I	The latch data inputs.
LE	I	The latch enable input. The latches are transparent when LE is HIGH. Input data is latched on the HIGH-to-LOW transition.
Y_1	O	The three-state latch outputs.
$\overline{OE}$	I	The output enable control. When $\overline{OE}$ is LOW, the outputs are enabled. When $\overline{OE}$ is HIGH, the outputs Y_1 are in the high-impedance (off) state.
$\overline{PRE}$	I	Preset line. When $\overline{PRE}$ is LOW, the outputs are HIGH if $\overline{OE}$ is LOW. Preset overrides $\overline{CLR}$.

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FUNCTION TABLES[§]
'FCT841/843

Inputs					Internal	Outputs	Function
$\overline{CLR}$	$\overline{PRE}$	$\overline{OE}$	LE	D_1	O_1	Y_1	
H	H	H	X	X	X	Z	High Z
H	H	H	H	L	L	Z	High Z
H	H	H	H	H	H	Z	High Z
H	H	H	L	X	NC	Z	Latched (High Z)
H	H	L	H	L	L	L	Transparent
H	H	L	H	H	H	H	Transparent
H	H	L	L	X	NC	NC	Latched
H	L	L	X	X	H	H	Preset
L	H	L	X	X	L	L	Clear
L	L	L	X	X	H	H	Preset
L	H	H	L	X	L	Z	Latched (High Z)
H	L	H	L	X	H	Z	Latched (High Z)

§ H = HIGH, L = LOW, X = Don't care, NC = No Change, Z = High Impedance.

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ABSOLUTE MAXIMUM RATINGS[1,2]

Symbol	Parameter	Value	Unit
T_{STG}	Storage Temperature	–65 to +150	°C
T_A	Ambient Temperature Under Bias	–65 to +135	°C
V_{CC}	V_{CC} Potential to Ground	–0.5 to +7.0	V
I_{IN}	Input Current	–30 to +5.0	mA

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Symbol	Parameter	Value	Unit
I_{OUTPUT}	Current Applied to Output	120	mA
V_{IN}	Input Voltage	–0.5 to V_{CC} + 0.5	V
V_{OUT}	Voltage Applied to Output	–0.5 to V_{CC} + 0.5	V

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Notes:

1. Operation beyond the limits set forth in the above table may impair the useful life of the device. Unless otherwise noted, these limits are over the operating free-air temperature-range.
2. Unused inputs must always be connected to an appropriate logic voltage level, preferably either V_{CC} or ground.

RECOMMENDED OPERATING CONDITIONS

Free Air Ambient Temperature	Min	Max
Military Commercial	–55°C 0°C	+125°C +70°C

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Supply Voltage (V_{CC})	Min	Max
Military Commercial	+4.5V +4.75V	+5.5V +5.25V

1564 Tbl 06

DC ELECTRICAL CHARACTERISTICS (Over recommended operating conditions)

Symbol	Parameter		Min	Typ[1]	Max	Units	V_{CC}	Conditions
V_{IH}	Input HIGH Voltage		2.0			V		
V_{IL}	Input LOW Voltage				0.8	V		
V_H	Hysteresis			0.35		V		All inputs
V_{CD}	Input Clamp Diode Voltage			–0.7	–1.2	V	MIN	I_{IN} = –18mA
V_{OH}	Output HIGH Voltage	V_{CC} = 3V, V_{IN} = 0.2V, or V_{CC} – 0.2V	V_{CC} – 0.2	V_{CC}		V		I_{OH} = –32μA
		Military/Commercial (CMOS)	V_{CC} – 0.2	V_{CC}		V	MIN	I_{OH} = –300μA
		Military (TTL)	2.4	4.3		V	MIN	I_{OH} = –12mA
		Commercial (TTL)	2.4	4.3		V	MIN	I_{OH} = –15mA
V_{OL}	Output LOW Voltage	V_{CC} = 3V, V_{IN} = 0.2V, or V_{CC} – 0.2V		GND	0.2	V		I_{OL} = 300μA
		Military/Commercial (CMOS)		GND	0.2	V	MIN	I_{OL} = 300μA
		Military (TTL)		0.3	0.5	V	MIN	I_{OL} = 32mA
		Commercial (TTL)		0.3	0.5	V	MIN	I_{OL} = 48mA
		Commercial (TTL)		0.3	0.5	V	MIN	I_{OL} = 64mA
I_{IH}	Input HIGH Current				5	μA	MAX	V_{IN} = V_{CC}
I_{IL}	Input LOW Current				–5	μA	MAX	V_{IN} = GND
I_{IH}	Input HIGH Current[3]				5	μA	MAX	V_{IN} = 2.7V
I_{IL}	Input LOW Current[3]				–5	μA	MAX	V_{IN} = 0.5V
I_{OZH}	Off State I_{OUT} HIGH-Level Output Current				10	μA	MAX	V_{OUT} = V_{CC}
I_{OZL}	Off State I_{OUT} LOW-Level Output Current				–10	μA	MAX	V_{OUT} = GND
I_{OZH}	Off State I_{OUT} HIGH-Level Output Current[3]				10	μA	MAX	V_{OUT} = 2.7V
I_{OZL}	Off State I_{OUT} LOW-Level Output Current[3]				–10	μA	MAX	V_{OUT} = 0.5V
I_{OS}	Output Short Circuit Current[2]		–75	–120	–225	mA	MAX	V_{OUT} = 0.0V
C_{IN}	Input Capacitance[3]			5	10	pF	MAX	All inputs
C_{OUT}	Output Capacitance[3]			9	12	pF	MAX	All outputs

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Notes:

1. Typical limits are at V_{CC} = 5.0V, T_A = +25°C ambient.
2. Not more than one output should be shorted at a time. Duration of short should not exceed one second. The use of high speed test apparatus and/or sample and hold techniques are preferable in order to minimize internal chip heating and more accurately reflect operational values. Otherwise prolonged shorting of a high output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.
3. This parameter is guaranteed but not tested.

DC CHARACTERISTICS (Over recommended operating conditions unless otherwise specified.)

Symbol	Parameter	Typ[1]	Max	Units	Conditions
I_{CC}	Quiescent Power Supply Current (CMOS inputs)	.003	0.3	mA	V_{CC} = MAX, $V_{IN} \leq$ 0.2v or f_1 = 0, Outputs Open
ΔI_{CC}	Quiescent Power Supply Current (TTL inputs)		2.0	mA	V_{CC} = MAX, V_{in} = 3.4V[2], f = 0, Outputs Open
I_{CCD}	Dynamic Power Supply Current[3]	0.15	0.25	mA/ mHz	V_{CC} = MAX, One Input Toggling, 50% Duty Cycle, Outputs Open, $\overline{OE}$ = GND, LE = V_{CC}, $V_{IN} \leq$ 0.2V or $V_{IN} \geq V_{CC}$ – 0.2V
I_C	Total Power Supply Current[5]	1.7	4.0	mA	V_{CC} = MAX, 50% Duty Cycle, Outputs Open, One Bit Toggling at f_1 = 10MHz, $\overline{OE}$ = GND, LE = V_{CC}, $V_{IN} \leq$ 0.2V or $V_{IN} \geq V_{CC}$ – 0.2V
		2.0	5.0	mA	V_{CC} = MAX, 50% Duty Cycle, Outputs Open, One Bit Toggling at f_1 = 10mHz, $\overline{OE}$ = GND, LE = V_{CC}, V_{IN} = 3.4V or V_{IN} = GND
		3.2	6.5[4]	mA	V_{CC} = MAX, 50% Duty Cycle, Outputs Open, Eight Bits Toggling at f_1 = 2.5MHz, $\overline{OE}$ = GND, LE = V_{CC}, $V_{IN} \leq$ 0.2V or $V_{IN} \geq V_{CC}$ – 0.2V
		5.2	14.5[4]	mA	V_{CC} = MAX, 50% Duty Cycle, Outputs Open, Eight Bits Toggling at f_1 = 2.5MHz, $\overline{OE}$ = GND, LE = V_{CC}, V_{IN} = 3.4V or V_{IN} = GND

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Notes:

1. Typical values are at V_{CC} = 3.3V, +25°C ambient.
2. Per TTL driven input (V_{IN} = 2.7V); all other inputs at V_{CC} or GND.
3. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
4. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
5. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$

   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD}(f_0/2 + f_1 N_1)$

   I_{CC} = Quiescent Current with CMOS input levels

   ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 2.7V)

   D_H = Duty Cycle for TTL Inputs High

   N_T = Number of TTL Inputs at D_H

   I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)

   f_0 = Clock Frequency for Register Devices (Zero for Non-Register Devices)

   f_1 = Input Frequency

   N_1 = Number of Inputs at f_1

   All currents are in milliamps and all frequencies are in megahertz.

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

Sym.	Parameter	Test Conditions[1]	'FCT841A/843A MIL Min.[2]	'FCT841A/843A MIL Max.	'FCT841A/843A COM'L Min.[2]	'FCT841A/843A COM'L Max.	'FCT841B/843B MIL Min.[2]	'FCT841B/843B MIL Max.	'FCT841B/843B COM'L Min.[2]	'FCT841B/843B COM'L Max.
t_{PLH} t_{PHL}	Propagation Delay D_I to Y_I (LE = HIGH)	C_L = 50pF R_L = 500Ω		10.0		9.0		7.5		6.5
		C_L = 300pF[3] R_L = 500Ω		15.0		13.0		15.0		13.0
t_{SU}	Data to LE Set-up Time	C_L = 50pF	2.5		2.5		2.5		2.5	
t_H	Data to LE Hold Time	R_L = 500Ω	3.0		2.5		2.5		2.5	
t_{PLH} t_{PHL}	Propagation Delay LE to Y_I	C_L = 50pF R_L = 500Ω		13.0		12.0		10.5		8.0
		C_L = 300pF[3] R_L = 500Ω		20.0		16.0		18.0		15.5
t_{PLH}	Propagation Delay $\overline{PRE}$ to Y_I	C_L = 50pF R_L = 500Ω		14.0		12.0		10.0		8.0
t_{REM}	Recovery Time $\overline{PRE}$ to Y_I			17.0		14.0		13.0		10.0
t_{PHL}	Propagation Delay $\overline{CLR}$ to Y_I			14.0		13.0		11.0		10.0
t_{REM}	Recovery Time $\overline{CLR}$ to Y_I			17.0		14.0		10.0		10.0
t_W	LE Pulse Width[3] HIGH		5.0		4.0		4.0		4.0	
t_W	$\overline{PRE}$ Pulse Width[3] LOW		7.0		5.0		4.0		4.0	
t_W	$\overline{CLR}$ Pulse Width[3] LOW		5.0		4.0		4.0		4.0	
t_{PZH} t_{PZL}	Output Enable Time $\overline{OE}$ to Y_I	C_L = 50pF R_L = 500Ω		13.0		11.5		8.5		8.0
		C_L = 300pF[3] R_L = 500Ω		25.0		23.0		15.0		14.0
t_{PHZ} t_{PLZ}	Output Disable Time $\overline{OE}$ to Y_I	C_L = 5pF[3] R_L = 500Ω		9.0		7.0		6.5		6.0
		C_L = 50pF R_L = 500Ω		10.0		8.0		7.5		7.0

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Notes:
1. See test circuit and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. This parameters are guaranteed but not tested.

ORDERING INFORMATION

PxxFCT	xxxx	x	x
Temp. Range	Device Type	Package	Process

Process

Blank	Commercial
M	Military Temperature
MB	MIL-STD-883, Class B

Package

P	Plastic DIP
D	CERDIP
S	Small Outline IC
L	Leadless Chip Carrier

Device Type

841A	10-Bit Non-inverting Latch
843A	9-Bit Non-inverting Latch
841B	8-Bit Non-inverting Latch
843B	Fast 10-Bit Non-inverting Latch

Temp. Range

74	Commercial
54	Military

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