



P/ACTIVE™ SCHOTTKY DIODE MEMORY BUS TERMINATOR

Features

- Provides proper bus termination independent of card loading conditions
- Schottky diode technology; fast turn on and reverse recovery characteristics
- 36 integrated diodes in a single package offers 18 channel, dual rail clamping action
- 24-pin QSOP package saves board space and eases layout in space critical bus termination applications
- Available in 24 pin TSSOP package for component height constrained modules

Applications

- SDRAM Memory Bus Termination
- PCI v2.1 Bus Termination for Intel-based Pentium® and Pentium Pro systems

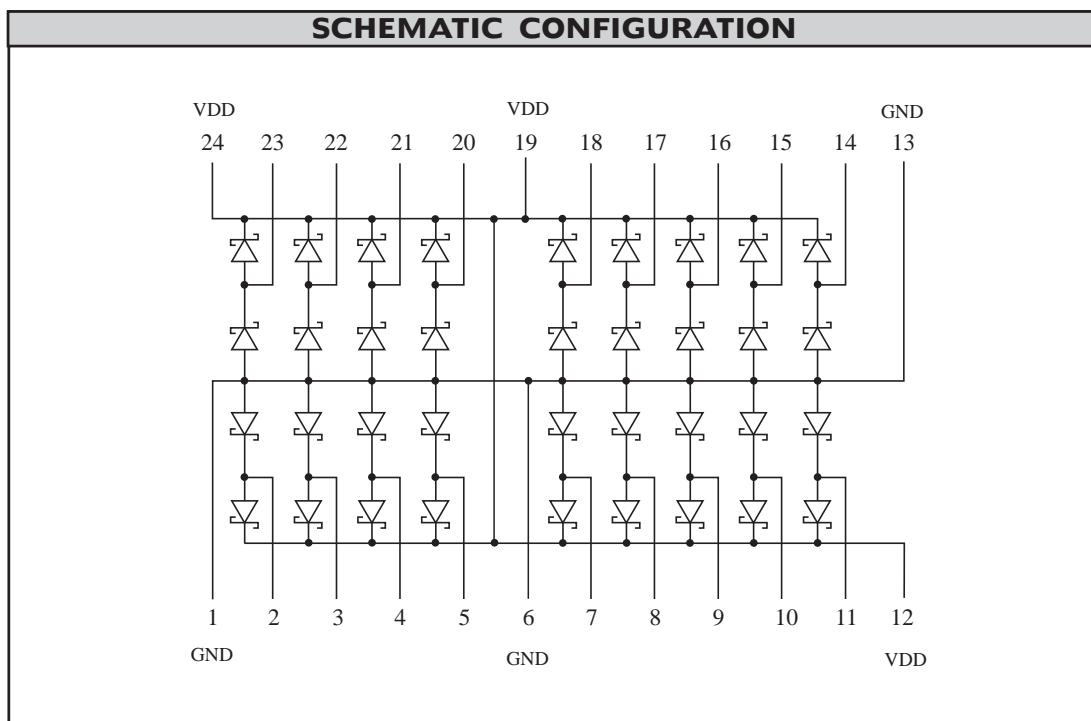
Refer to AP-201 Termination Application Note for further information.

Product Description

Reflections on high speed Memory Buses lead to undershoot and overshoot disturbances which may result in improper system operation. Resistor terminations, when used to terminate high speed memory or data lines, increase power consumption and degrade output (high) levels resulting in reduced noise immunity. Schottky diode termination is the best overall solution for applications in which power consumption and noise immunity are critical considerations.

CAMD's P/Active DN010 Schottky Diode Memory Bus Terminator† is specifically designed to minimize undershoot/overshoot disturbances caused by reflection noise on SDRAM bus lines as well as v2.1 66MHz PCI buses.

This highly integrated Schottky diode network provides very effective termination performance for high speed Memory Bus lines under variable loading conditions. The packaged device supports up to 18 terminated lines — each of which can be simultaneously clamped to both ground and power supply rail.



P/Active™ is a trademark of California Micro Devices Corp.
Pentium Pro is a registered trademark of Intel.

† Covered by one or more of U.S. Pat. Nos. 5,355,014, 5,370,766, and 5,514,612 and other pending applications.



STANDARD SPECIFICATION		
Absolute Maximum Ratings		
Parameter	Symbol	Rating
Supply Voltage	V_{DD}	-0.3V to 7V
Channel clamp current (continuous)	I_{clamp}	±50mA
Operating Temperature		0°C to 70°C
Storage Temperature	T_{stg}	-60°C to 150°C
Package Power Rating	QSOP @ 70°C	1.00W, max.
	QSOP @ 70°C	1.00W, max.

The absolute maximum ratings are limiting values, to be applied individually, beyond which the device may be permanently damaged. Functional operation under any of these conditions is not guaranteed. Exposing the device to its absolute maximum rating may affect its reliability.

DIODE CHARACTERISTICS (TA = 0°C TO 70°C)				
Parameter	Condition	Min	Typ	Max
Diode forward Voltage	$I_F = 16mA$		0.65V	0.85V
	$I_F = 50mA$		0.80V	1.0V
Max. Bus Speed (See Note 1)	$Z_0 = 50\Omega$, Logic Swing 0.4V to 3.0V		125MHz	
Channel leakage	$0 \leq V_{IN} \leq V_{DD}$		0.1µA	5µA
Input Capacitance	$f = 1MHz$, $V_{IN} = 2.5V$, $T_A = 25^\circ C$, $V_{DD} = 5.0V$		5pF	
ESD Protection	MIL-STD-883, Method 3015	2KV		

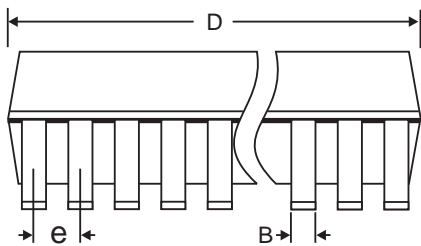
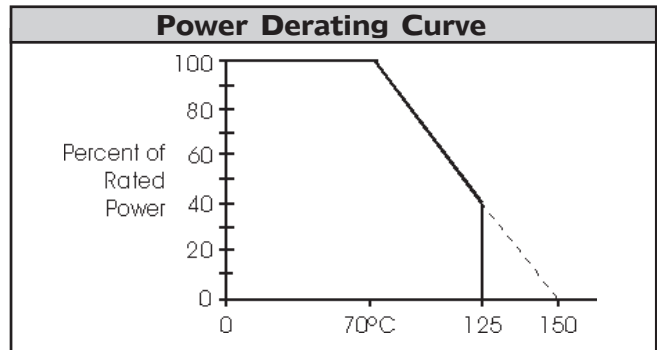
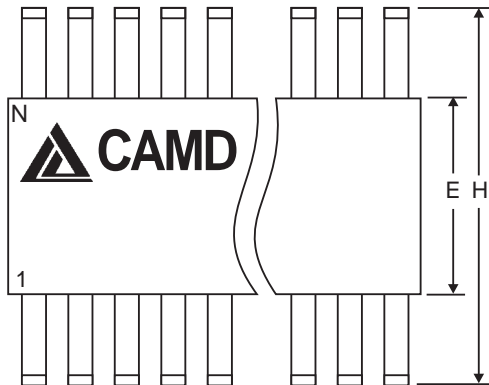
STANDARD PART ORDERING INFORMATION				
Package		Ordering Part Number		
Pins	Style	Tubes	Tape & Reel	Part Marking
24	QSOP	PACDN010Q/T	PACDN010Q/R	PACDN010Q
24	TSSOP	PACDN010T/T	PACDN010T/R	PACDN010T

Note 1:

The presence of a Schottky diode for clamping bus overshoots will cause additional delays of signal edges. These delays are the result of diode characteristics such as forward voltage, diode capacitance and the reverse recovery phenomenon. The ground clamp diode is most critical, particularly if VLSI circuits such as static or dynamic memories are directly connected to busses without any buffer stages. The incremental delay observed on a positive edge following a negative transition that forward biased the Schottky diode is less than 800 pS. That represents less than 10% of the 125 MHz (8 nS period) bus cycle time.



QSOP - TOP VIEW



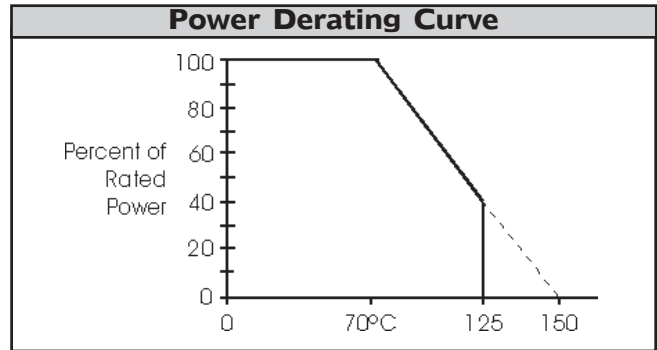
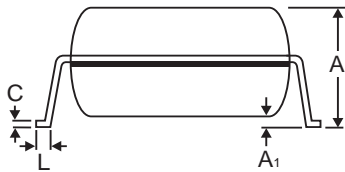
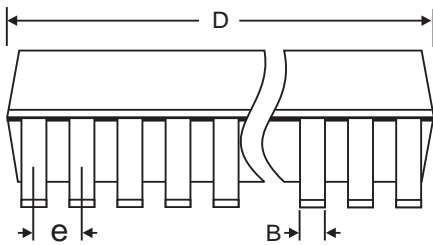
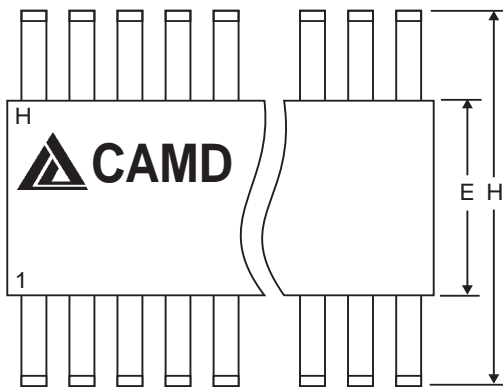
MECHANICAL SPECIFICATIONS	
Lead Plating	Tin-Lead
Lead Material	Copper Alloy
Lead Coplanarity	0.004" (0.102mm)
Substrate Material	Silicon
Body Material	Molded Epoxy
Flammability	UL94V-0



Package Dimensions, Power Dissipation & Information				
Package	QSOP			
Pins	24			
JEDEC	MO137			
	mm		inches	
	min	max	min	max
A	1.35	1.75	0.053	0.069
A ₁	0.10	0.25	0.004	0.010
B	0.20	0.30	0.008	0.012
C	0.18	0.25	0.007	0.010
D	8.56	8.73	0.337	0.344
E	3.81	3.98	0.150	0.157
e	0.64 BSC		0.025 BSC	
H	5.79	6.19	0.228	0.244
L	0.40	1.27	0.016	0.050
P _D @ 70°C	1.00W			
# / tube	58 pcs			
# / tape & reel	2,500 pcs			



TSSOP - TOP VIEW



MECHANICAL SPECIFICATIONS	
Lead Plating	Tin-Lead
Lead Material	Copper Alloy
Lead Coplanarity	0.004" (0.102mm)
Substrate Material	Silicon
Body Material	Molded Epoxy
Flammability	UL94V-0

Package Dimensions, Power Dissipation & Information				
Package	TSSOP			
Pins	24			
JEDEC	MO153			
	mm		inches	
	min	max	min	max
A	-	1.10	-	0.433
A ₁	0.05	0.15	0.002	0.006
B	0.19	0.30	0.0075	0.0118
C	0.09	0.20	0.0035	0.0079
D	7.70	7.90	0.303	0.311
E	4.30	4.50	0.169	0.177
e	0.65 BSC		0.0256 BSC	
H	6.25	6.50	0.246	0.256
L	0.50	0.70	0.020	0.028
P _D @ 70°C	1.00W			
# / tube	62 pcs			
# / tape & reel	2,500 pcs			