UM82C550 Asynchronous Communication Element with FIFOs

Features:

- Capable of running all existing 82C450 software
- Pin for pin compatible with the existing UM82C450 except for CSOUT (24) and NC (29). The former CSOUT and NC pins will be TXRDY and RXRDY, respectively
- After reset, all registers are identical to the UM82C450 register set
- In the FIFO mode, transmitter and receiver are each buffered with 16 byte FIFO's to reduce the number of interrupts presented to the CPU.
- Adds or deletes standard asynchronous communication bits (start, stop, and parity) to or from the serial data
- Full double buffering in the CHARACTER mode eliminates need for precise synchronization
- Independently controlled transmit, receive, line status, and data set interrupts.
- Programmable baud generator divides any input clock by 1 to $(2^{16} - 1)$ and generates the 16x clock
- Independent receiver clock input
- MODEM control functions (CTS, RTS, DSR, DTR, RI, and DCD)
- Fully progrmmable serial-interface characteristics:
  - 5-, 6-, 7-, or 8-bit characters
  - Even, odd, or no-parity bit generation and detection
  - 1-, 1½-, or 2-stop bit generation
  - Baud generation (DC to 256K baud)
- False start bit detection
- Complete status reporting capabilities
- TRI-STATE TTL drive for the data and control buses
- Line break generation and detection
- Internal diagnostic capabilities:
  - Loopback controls for communications link fault isolation
  - Break parity overrun framing error simulation
- Fully prioritized interrupt system controls

Pin Configurations