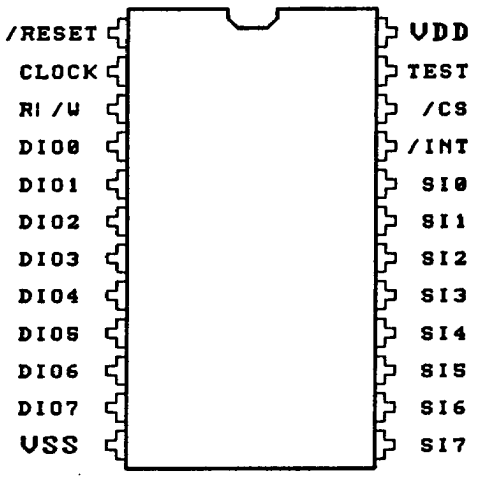
OCTAL SENSOR INTERFACE 74HC10490

The **74HC10490** is a **CMOS** integrated circuit that is designed to interface to any type of mechanical contact or optical switch to eliminate contact bounce or transient signal effects. The **74HC10490** provides eight sensor inputs that have internal pullups and are Schmitt input buffered. This means that any unused inputs do not have to be tied to **VDD** or **VSS**, e.g., the unused inputs can be left floating. The **74HC10490** can be used in both microprocessor or in non-microprocessor based sensor interface applications. In the case of a microprocessor based application, the **74HC10490** has input masking capability to prevent interrupts from occurring when an input changes state. In the case of a non-microprocessor based application, input signals **/CS** and **R/W** can be left floating because **/CS** has an internal pulldown and **R/W** has an internal pullup.



The input **CLK** signal is used to drive the digital contact bounce eliminator circuitry that takes an input signal from a bouncing contact or a transient sensor output and generates a clean digital signal four clock periods after the input has stabilized. The output **TEST** signal is the internally divided **CLK** signal, where the divide rate can be programmed from a default of 2 up to a maximum value of 64 in increments of 2. The output **INTERRUPT** signal is a true low open collector output that requires a pullup for proper operation and can be wired-or connected to other **74HC10490 INTERRUPT** outputs within a system design. The **74HC10490** data bus input/output signals are controlled by the **/CS** and **R/W** input signals. Figure 1 shows a generalized block diagram of the **74HC10490**.

When the input **/CS** signal is high, the data bus signals are always in a tri-state mode. When the input **/CS** signal is low and the input **R/W** signal is high, the data bus signals are set to the output mode. When the input **/CS** signal is low and the input **R/W** signal is low, the data bus signals are set to the input mode. The input **/CS** signal must be framed by the input **R/W** signal for proper operation of the **74HC10490**, (see Figures 2 and 3 for additional timing information).

MAXIMUM RATING		VALUE	UNIT
V_{DD}	DC SUPPLY VOLTAGE	-0.5 to 7.0	V
V_{IK}	DC INPUT, OUTPUT VOLTGE (CLAMP VOLTAGE)	-1.5 to V_{DD} + 1.5	V
I	DC CURRENT DRAIN PER PIN, ANY INPUT OR OUTPUT	25	mA
I	DC CURRENT DRAIN V_{CC} AND GND PINS	50	mA
T_{stg}	STORAGE TEMPERATURE	-65 to + 150	°C
T_L	LEAD TEMPERATURE (10 SECOND SOLDERING)	300	°C

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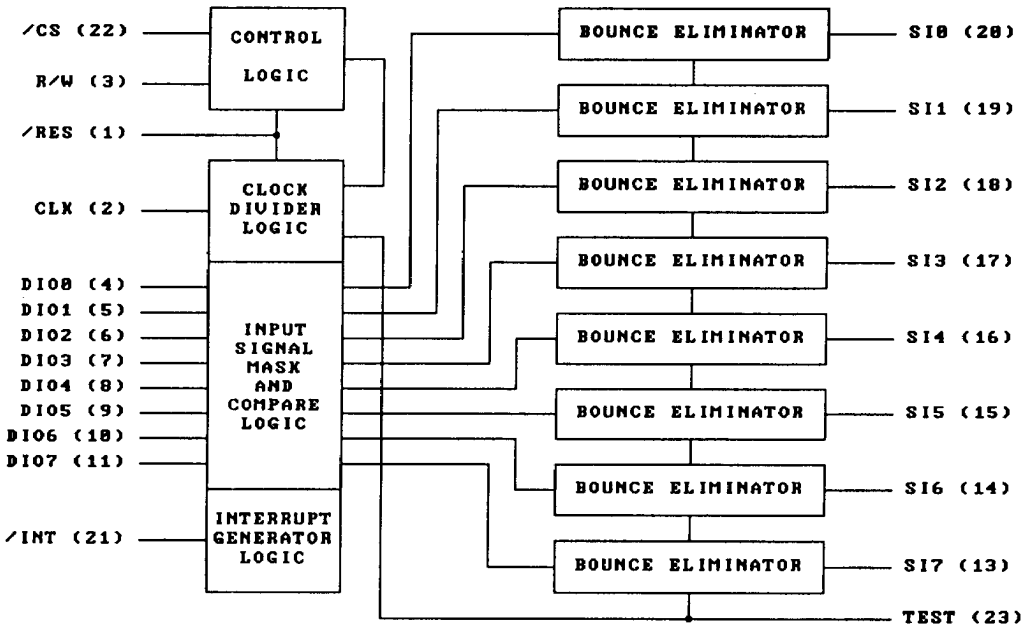

FIGURE 1. 74HC10490 BLOCK DIAGRAM

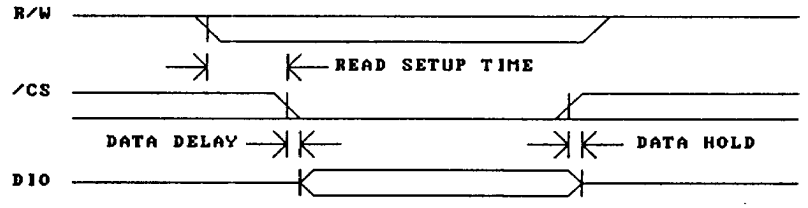

FIGURE 2. READ TIMING

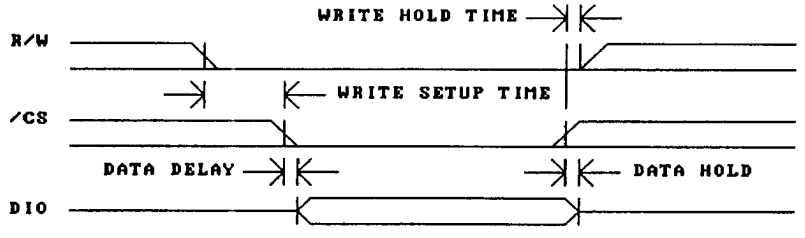

FIGURE 3. WRITE TIMING

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RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN	MAX	UNIT
V_{DD}	DC SUPPLY VOLTAGE (TO GUARANTEE FUNCTIONALITY)	3.0	6.0	V
V_{DD}	DC SUPPLY VOLTAGE (FOR DC AND AC SPECS)	4.5	5.5	V
V_{in}, V_{out}	INPUT VOLTAGE, OUTPUT VOLTAGE	0.0	V_{DD}	V
T_A	COMMERCIAL OPERATING TEMPERATURE	0	+70	°C

ELECTRICAL CHARACTERISTICS (VOLTAGES REFERENCED TO V_{SS})

SYM.	PARAMETER	TEST CONDITIONS	V_{DD}	25°C TYPICAL	IND GUAR LIMIT	UNIT
V_{IH}	MIN. HIGH-LEVEL INPUT VOLTAGE	V_{out} = 0.1V or V_{DD} - 0.1 V, $\|I_{IH}\|$ = 20µA	4.5 5.5	2.4 2.9	3.15 3.85	V
V_{IL}	MAX. LOW LEVEL INPUT VOLTAGE	V_{out} = 0.1V or V_{DD} - 0.1 V, $\|I_{IL}\|$ = 20µA	4.5 5.5	1.8 2.2	1.35 1.65	V
V_{OH}	MIN. HIGH-LEVEL OUTPUT VOLTAGE	V_{in} = V_{IH} or V_{IL} I_{OH} = - 20µA	4.5 5.5	4.5 5.5	4.4 5.4	V
V_{OH}	MIN. HIGH-LEVEL OUTPUT VOLTAGE	V_{in} = V_{IH} or V_{IL} I_{OH} = - 4mA	4.5	4.0	3.7	V
V_{OL}	MAX. HIGH-LEVEL OUTPUT VOLTAGE	V_{in} = V_{IH} or V_{IL} I_{OL} = 20µA	4.5 5.5	0.001 0.001	0.1 0.1	V
V_{OL}	MAX. HIGH-LEVEL OUTPUT VOLTAGE	V_{in} = V_{IH} or V_{IL} I_{OL} = 4mA	4.5	0.2	0.4	V
I_{in}	MAX. INPUT LEAKAGE CURRENT, CLOCK	V_{in} = V_{DD} or V_{SS}	5.5	± 1x10^{-4}	± 1.0	µA
I_{in}	MAX. INPUT LEAKAGE CURRENT, /RES, R/W, SI0-SI7	V_{in} = V_{SS}	5.5	–	-45	µA
I_{in}	MAX. INPUT LEAKAGE CURRENT, /CS	V_{in} = V_{DD}	5.5	–	120	µA
I_{OZ}	MAX. OUTPUT LEAKAGE CURRENT, DIO0-DIO7	Output = High Imp. V_{out} = V_{DD} or V_{SS}	5.5	± 0.05	± 5	µA
I_{OZ}	MAX. OUTPUT LEAKAGE CURRENT, /INT	Output = High Imp. V_{out} = V_{DD}	5.5	± 0.05	± 5	µA
I_{DD}	MAX. QUIESCENT SUPPLY CURRENT	V_{in} = V_{DD} or V_{SS} I_{out} = 0µA	5.5	–	750	µA
C_{in}	MAX. INPUT CAPACITANCE		–	–	10	pF
C_{out}	MAX.OUTPUT CAPACITANCE	Output = High Imp.	–	–	12.5	pF

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SWITCHING CHARACTERISTICS (T_A = 25°C, C_L = 50 pF, V_{DD} = 5V DC)

CHARACTERISTIC	MIN	25°C TYPICAL	MAX	UNIT
OUTPUT RISE TIME				
BIDIRECTIONAL DATA BUS	–	6	12	ns
TEST	–	6	12	ns
/INT (1K PULLUP)	–	6	11	ns
OUTPUT FALL TIME				
BIDIRECTIONAL DATA BUS	–	7	13	ns
TEST	–	7	12	ns
/INT	–	7	12	ns
PROPAGATION TIME, SENSOR INPUT TO DATA OUTPUT DEFAULT DIVIDE RATE, N = 2 INPUT CLOCK FREQUENCY, MHz $T = F \times 10^{-9}$ ns for example, F = 1 MHz T = 1000 ns 4 NT + 65 = 8065 ns = 8.065 µs	8T + 20	8T + 45	8T + 65	ns
PROGRAM DIVIDE RATE, N = 2, 4,···, 64	4NT + 20	4NT + 45	4NT + 65	ns
READ SETUP TIME (READ OR WRITE OPERATION)	10	–	–	ns
DATA DELAY TIME (READ OPERATION)	–	15	25	ns
DATA DELAY TIME (WRITE OPERATION)	–	–	50	ns
DATA HOLD TIME (READ OPERATION)	10	20	–	ns
DATA HOLD TIME (WRITE OPERATION)	20	–	–	ns
WRITE HOLD TIME	0	10	–	ns
/CS PULSE WIDTH	100	–	–	ns
EXTERNAL CLOCK INPUT	–	1	10	MHz

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THEORY OF OPERATION

The **74HC10490** Octal Sensor Interface is composed of a number of functional elements as shown in the generalized block diagram of Figure 1. The bounce eliminator circuitry blocks are composed of a string of shift registers, an output data latch and a block input/output comparator consisting of an exclusive-or gate. The operating concept is that the block input/output is compared, and if of different polarity, allows the shift registers to begin shifting a clock pulse toward the clock input of the data latch, whose data input is the sensor input to be debounced. If the sensor input changes state during the four clock debounce period, the shift register string is immediately reset and the four clock debounce period is restarted.

The debounce clock is derived from the input clock divider block. Of the eight bit input data bus (DIO0-DIO7), the clock divide ratio is determined by the lower group of bits, DIO1-DIO5. The least significant bit, DIO0, is always set to a 1 so that the minimum/default divide rate is always a value of 2 because the clock divider is really a down counter with a carry output and, therefore, 2 clock pulses are required before a carry output is generated. If the DIO1 and DIO2 bits are set to a 1, then the loaded divider value is a binary XX000111 or 7 and, therefore, the divide rate will be a value of 8 because 8 clock pulses to the down counter are required before a carry output is generated. At this point, it is clear that the allowed divide rates are even numbers 2 through 64. The carry out signal becomes the debounce clock and is available through the TEST output of the **74HC10490**.

The interrupt generator block consists of an input mask latch, a combination comparator and transparent latch to generate a pulse whenever any unmasked input changes state, and an interrupt signal output latch that is reset on power-up and at the end of any read cycle. The input mask latch circuitry simply does not allow any masked input signal change to enter the comparator logic circuitry. It is necessary to do a dummy read operation after power-up to clear an interrupt that may have latched as a result of existing input signal conditions. This dummy read operation to clear the **74HC10940** interrupt output must be done before the microprocessor based interrupt facility is enabled. Since the interrupt generator block responds to changes in the state of the input signals, this means that interrupts are generated for both H->L and L->H changes of state. It is a function of the microprocessor based software to determine which edge has generated the interrupt.

The control logic block consists of various gating and latch logic to synchronize the input signals, control the write register sequencer circuitry, and to generate all of the appropriate internal reset and interrupt output signals. It is important to understand that the **74HC10490** does not have an address line input and that there are two internal registers that can be written to. As a result, an input write sequencer is used to determine which of the two registers actually receives the input data byte. Any read operation resets the sequencer. Also, the mask register is always written to in the first write operation after a reset of the sequencer. The concept is that sensor input mask write operations are those that may occur often in the monitoring of various sensor inputs whereas a divider ratio write operation to set up the debounce clock period would most likely occur as part of a power-on initialization process.

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THEORY OF OPERATION (continued)

Based on the above theory of operation statement, it is appropriate to review the important operating parameters that must be adhered to in order for the **74HC10490** to perform properly. These are as follows:

1) The /CS input signal must be framed by the R/W input signal.
2) A read operation always resets the interrupt output.
3) A read operation always resets the write register sequencer.
4) The mask byte must always be written first and the divide ratio must always be written second.

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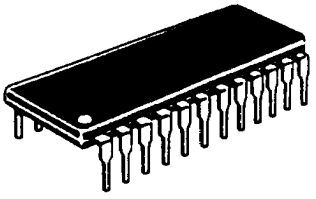

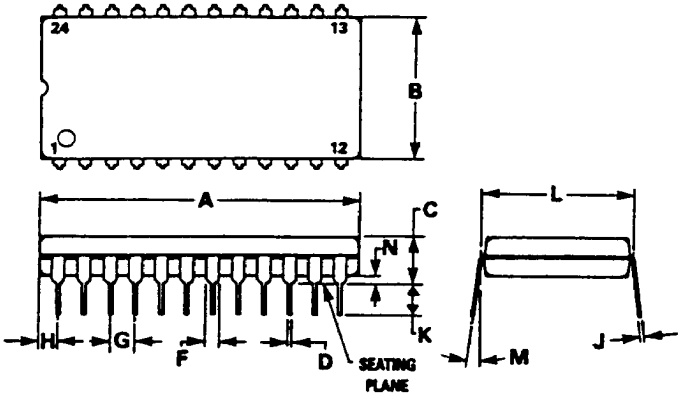

NOTES:
1. POSITIONAL TOLERANCE OF LEADS (D), SHALL BE WITHIN 0.25 mm (0.010) AT MAXIMUM MATERIAL CONDITION, IN RELATION TO SEATING PLANE AND EACH OTHER.
2. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSION B DOES NOT INCLUDE MOLD FLASH.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	31.37	32.13	1.235	1.265
B	13.72	14.22	0.540	0.560
C	3.94	5.08	0.155	0.200
D	0.36	0.56	0.014	0.022
F	1.02	1.52	0.040	0.060
G	2.54 BSC		0.100 BSC	
H	1.65	2.03	0.065	0.080
J	0.20	0.38	0.008	0.015
K	2.92	3.43	0.115	0.135
L	15.24 BSC		0.600 BSC	
M	0°	15°	0°	15°
N	0.51	1.02	0.020	0.040

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