64K (8K x 8) Low Voltage CMOS E^2PROM

Features

- 2.7 V to 3.6 V Supply
  - Full Read and Write Operation
- Low Power Dissipation
  - 8 mA Active Current
  - 50 µA CMOS Standby Current
- Read Access Time - 200 ns
- Byte Write - 3 ms
- Direct Microprocessor Control
  - DATA Polling
  - READY/BUSY Open Drain Output
- High Reliability CMOS Technology
  - Endurance: 100,000 Cycles
  - Data Retention: 10 years
- Low Voltage CMOS Compatible Inputs and Outputs
- JEDEC Approved Byte-Wide Pinout
- Commercial and Industrial Temperature Ranges

Description

The AT28LV64 is a low-voltage, low-power Electrically Erasable and Programmable Read Only Memory. Its 64K of memory is organized 8,192 words by 8 bits. Manufactured with Atmel's advanced nonvolatile CMOS technology, the device offers access times to 200 ns with power dissipation less than 30 mW. When the device is deselected the standby current is less than 50 µA.

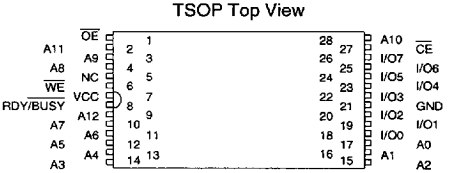
The AT28LV64 is accessed like a Static RAM for the read or write cycles without the need for external components. During a byte write, the address and data are latched internally, freeing the microprocessor address and data bus for other operations. Following the initiation of a write cycle, the device will go to a busy state and automatically clear and write the latched data using an internal control timer. The device includes two methods for detecting the end of a write cycle, level detection of RDY/$\overline{\text{BUSY}}$ and $\overline{\text{DATA}}$ polling of I/O_7. Once the end of a write cycle has been detected, a new access for a read or write can begin.

Atmel's 28LV64 has additional features to ensure high quality and manufacturability. The device utilizes error correction internally for extended endurance and for improved data retention characteristics. An extra 32 bytes of E^2PROM are available for device identification or tracking.

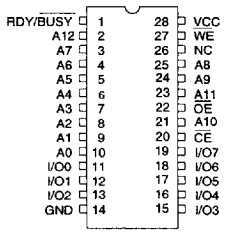
Pin Configurations

Pin Name	Function
A0 - A12	Addresses
$\overline{\text{CE}}$	Chip Enable
$\overline{\text{OE}}$	Output Enable
$\overline{\text{WE}}$	Write Enable
I/O0 - I/O7	Data Inputs/ Outputs
RDY/$\overline{\text{BUSY}}$	Ready/$\overline{\text{Busy}}$ Output
NC	No Connect

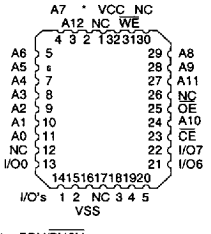
TSOP Top View



PDIP, SOIC Top View



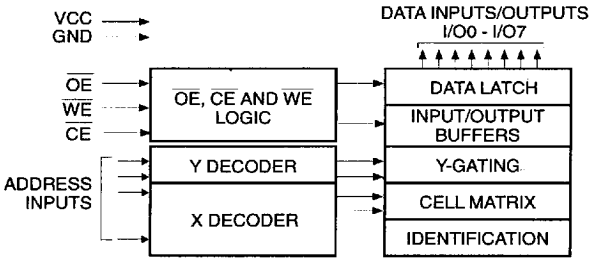
PLCC Top View



* = RDY/$\overline{\text{BUSY}}$

Note: PLCC package pins 1 and 17 are DON'T CONNECT.

Block Diagram



Absolute Maximum Ratings*

Temperature Under Bias	-55°C to +125°C
Storage Temperature	-65°C to +150°C
All Input Voltages (including N.C. Pins) with Respect to Ground	-0.6 V to +6.25 V
All Output Voltages with Respect to Ground	-0.6 V to V_{CC} +0.6 V
Voltage on $\overline{OE}$ and A9 with Respect to Ground	-0.6 V to +13.5 V

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Device Operation

READ: The AT28LV64 is accessed like a Static RAM. When $\overline{CE}$ and $\overline{OE}$ are low and $\overline{WE}$ is high, the data stored at the memory location determined by the address pins is asserted on the outputs. The outputs are put in a high impedance state whenever $\overline{CE}$ or $\overline{OE}$ is high. This dual line control gives designers increased flexibility in preventing bus contention.

BYTE WRITE: Writing data into the AT28LV64 is similar to writing into a Static RAM. A low pulse on the $\overline{WE}$ or $\overline{CE}$ input with $\overline{OE}$ high and $\overline{CE}$ or $\overline{WE}$ low (respectively) initiates a byte write. The address location is latched on the falling edge of $\overline{WE}$ (or $\overline{CE}$); the new data is latched on the rising edge. Internally, the device performs a self-clear before write. Once a byte write has been started, it will automatically time itself to completion. Once a programming operation has been initiated and for the duration of t_{WC}, a read operation will effectively be a polling operation.

READY/$\overline{BUSY}$: Pin 1 is an open drain READY/$\overline{BUSY}$ output that can be used to detect the end of a write cycle. RDY/$\overline{BUSY}$ is actively pulled low during the write cycle and is released at the completion of the write. The open drain connection allows for OR-tying of several devices to the same RDY/$\overline{BUSY}$ line.

$\overline{DATA}$ POLLING: The AT28LV64 provides $\overline{DATA}$ POLLING to signal the completion of a write cycle. During a write cycle, an attempted read of the data being written results in the complement of that data for I/O_7 (the other outputs are indeterminate). When the write cycle is finished, true data appears on all outputs.

WRITE PROTECTION: Inadvertent writes to the device are protected against in the following ways. (a) V_{CC} sense— if V_{CC} is below 1.8 V (typical) the write function is inhibited. (b) V_{CC} power on delay— once V_{CC} has reached 2.0 V the device will automatically time out 10 ms (typical) before allowing a byte write. (c) Write Inhibit— holding any one of $\overline{OE}$ low, $\overline{CE}$ high or $\overline{WE}$ high inhibits byte write cycles.

DEVICE IDENTIFICATION: An extra 32 bytes of E^2PROM memory are available to the user for device identification. By raising A9 to 12 ± 0.5 V and using address locations 1FE0H to 1FFFH the additional bytes may be written to or read from in the same manner as the regular memory array.

D.C. and A.C. Operating Range

		AT28LV64-20	AT28LV64-30
Operating Temperature (Case)	Com.	0°C - 70°C	0°C - 70°C
	Ind.	-40°C - 85°C	-40°C - 85°C
V_{CC} Power Supply		3.0 V to 3.6 V	2.7 V to 3.6 V

Operating Modes

Mode	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	I/O
Read	V_{IL}	V_{IL}	V_{IH}	D_{OUT}
Write[2]	V_{IL}	V_{IH}	V_{IL}	D_{IN}
Standby/Write Inhibit	V_{IH}	X[1]	X	High Z
Write Inhibit	X	X	V_{IH}	
Write Inhibit	X	V_{IL}	X	
Output Disable	X	V_{IH}	X	High Z

Notes: 1. X can be V_{IL} or V_{IH}.
2. Refer to A.C. Programming Waveforms.

D.C. Characteristics

Symbol	Parameter	Condition	Min	Max	Units
I_{LI}	Input Load Current	V_{IN} = 0 V to V_{CC} + 1.0 V		5	µA
I_{LO}	Output Leakage Current	$V_{I/O}$ = 0 V to V_{CC}		5	µA
I_{SB}	V_{CC} Standby Current CMOS	$\overline{CE}$ = V_{CC} - 0.3 V to V_{CC} + 1.0 V		50	µA
I_{CC}	V_{CC} Active Current A.C.	f = 5 MHz; I_{OUT} = 0 mA $\overline{CE}$ = V_{IL}		8	mA
V_{IL}	Input Low Voltage			0.6	V
V_{IH}	Input High Voltage		2.0		V
V_{OL}	Output Low Voltage	I_{OL} = 1 mA		0.3	V
		I_{OL} = 2 mA for RDY/$\overline{BUSY}$		0.3	V
V_{OH}	Output High Voltage	I_{OH} = -100 µA	2.0		V

Pin Capacitance (f = 1 MHz, T = 25°C) [1]

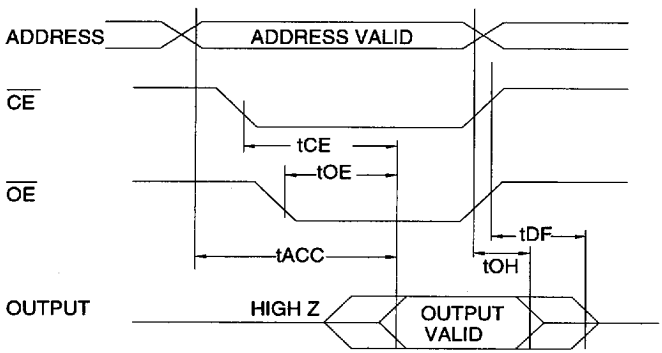
	Typ	Max	Units	Conditions
C_{IN}	4	6	pF	V_{IN} = 0 V
C_{OUT}	8	12	pF	V_{OUT} = 0 V

Note: 1. This parameter is characterized and is not 100% tested.

A.C. Read Characteristics

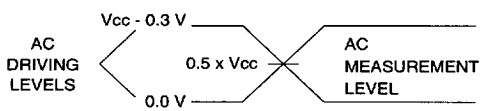
Symbol	Parameter	AT28LV64-20		AT28LV64-30		Units
		Min	Max	Min	Max	
t_{ACC}	Address to Output Delay		200		300	ns
t_{CE} (1)	$\overline{CE}$ to Output Delay		200		300	ns
t_{OE} (2)	$\overline{OE}$ to Output Delay	0	80	0	150	ns
t_{DF} (3,4)	$\overline{CE}$ or $\overline{OE}$ High to Output Float	0	55	0	60	ns
t_{OH}	Output Hold from $\overline{OE}$, $\overline{CE}$ or Address, whichever occurred first	0		0		ns

A.C. Read Waveforms(1,2,3,4)



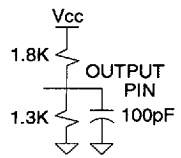
Notes:
1. $\overline{CE}$ may be delayed up to $t_{ACC} - t_{CE}$ after the address transition without impact on t_{ACC}.
2. $\overline{OE}$ may be delayed up to $t_{CE} - t_{OE}$ after the falling edge of $\overline{CE}$ without impact on t_{CE} or by $t_{ACC} - t_{OE}$ after an address change without impact on t_{ACC}.
3. t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$ whichever occurs first (C_L = 5 pF).
4. This parameter is characterized and is not 100% tested.

Input Test Waveforms and Measurement Level



t_R, t_F < 20 ns

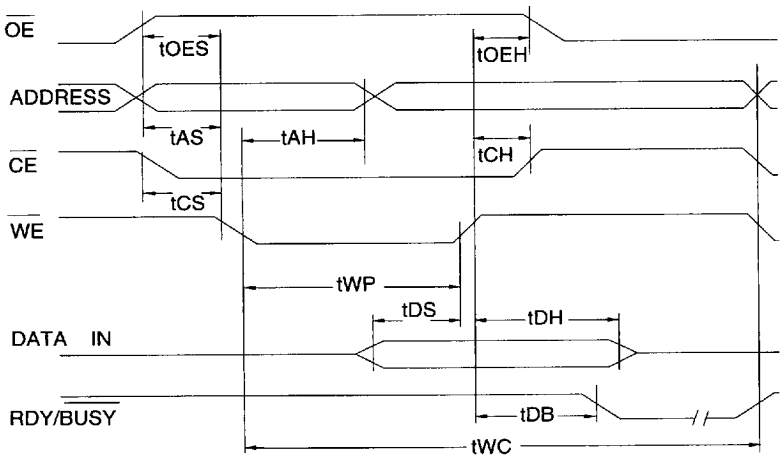
Output Test Load



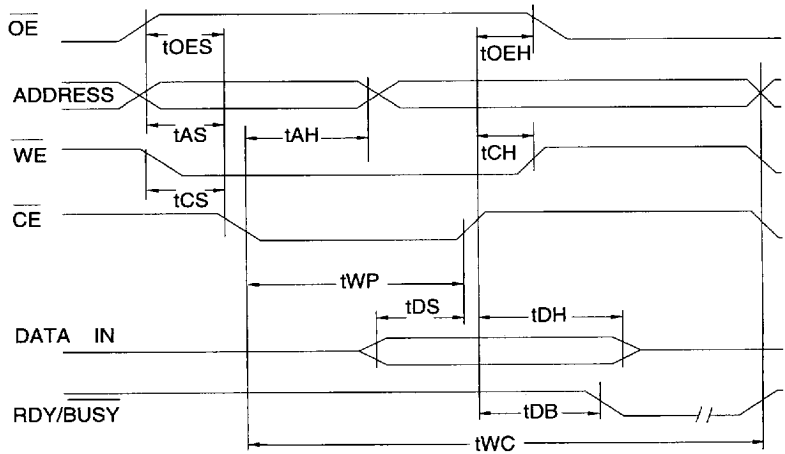
A.C. Write Characteristics

Symbol	Parameter	Min	Max	Units
t_{AS}, t_{OES}	Address, $\overline{OE}$ Set-up Time	10		ns
t_{AH}	Address Hold Time	100		ns
t_{WP}	Write Pulse Width ($\overline{WE}$ or $\overline{CE}$)	150	1000	ns
t_{DS}	Data Set-up Time	100		ns
t_{DH},t_{OEH}	Data, $\overline{OE}$ Hold Time	10		ns
t_{DB}	Time to Device Busy		50	ns
t_{WC}	Write Cycle Time		3	ms

A.C. Write Waveforms- $\overline{WE}$ Controlled



A.C. Write Waveforms- $\overline{CE}$ Controlled

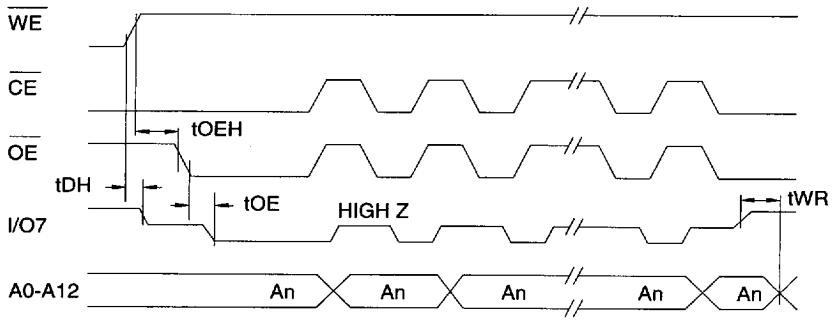


$\overline{\text{Data}}$ Polling Characteristics[1]

Symbol	Parameter	Min	Typ	Max	Units
t_{DH}	Data Hold Time	10			ns
t_{OEH}	$\overline{OE}$ Hold Time	10			ns
t_{OE}	$\overline{OE}$ to Output Delay[2]				ns
t_{WR}	Write Recovery Time	0			ns

Notes: 1. These parameters are characterized and not 100% tested.
2. See A.C. Read Characteristics.

$\overline{\text{Data}}$ Polling Waveforms



Ordering Information[1]

t_{ACC} (ns)	I_{CC} (mA)		Operating Voltage	Ordering Code	Package	Operation Range
	Active	Standby				
200	8	0.05	3.0 V to 3.6 V	AT28LV64-20JC AT28LV64-20PC AT28LV64-20SC AT28LV64-20TC	32J 28P6 28S 28T	Commercial (0°C to 70°C)
200	8	0.05	3.0 V to 3.6 V	AT28LV64-20JI AT28LV64-20PI AT28LV64-20SI AT28LV64-20TI	32J 28P6 28S 28T	Industrial (-40°C to 85°C)
300	8	0.05	2.7 V to 3.6 V	AT28LV64-30JC AT28LV64-30PC AT28LV64-30SC AT28LV64-30TC	32J 28P6 28S 28T	Commercial (0°C to 70°C)
300	8	0.05	2.7 V to 3.6 V	AT28LV64-30JI AT28LV64-30PI AT28LV64-30SI AT28LV64-30TI	32J 28P6 28S 28T	Industrial (-40°C to 85°C)

Note: 1. See Valid Part Number table below.

Valid Part Numbers

The following table lists standard Atmel products that can be ordered.

Device Numbers	Speed	Package and Temperature Combinations
AT28LV64	20	JC, JI, PC, PI, SC, SI, TC, TI
AT28LV64	30	JC, JI, PC, PI, SC, SI, TC, TI

Package Type	
32J	32 Lead, Plastic J-Leaded Chip Carrier (PLCC)
28P6	28 Lead, 0.600" Wide, Plastic Dual Inline Package (PDIP)
28S	28 Lead, 0.300" Wide, Plastic Gull Wing, Small Outline (SOIC)
28T	28 Lead, Plastic Thin Small Outline Package (TSOP)