International
IOR Rectifier

Preliminary Data Sheet No. PD60032-N

IR2131(J)(S)

3 HIGH SIDE AND 3 LOW SIDE DRIVER

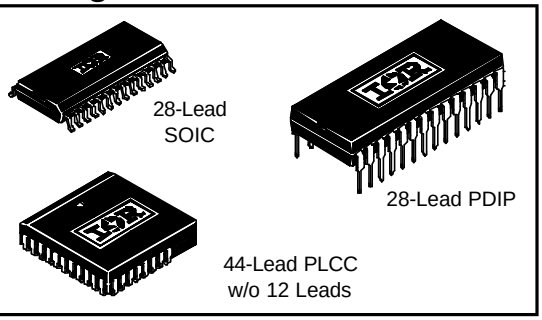
Features

- Floating channel designed for bootstrap operation
  Fully operational to +600V
  Tolerant to negative transient voltage
  dV/dt immune
- Gate drive supply range from 10 to 20V
- Undervoltage lockout for all channels
- Over-current shutdown turns off all six drivers
- Independent 3 high side & 3 low side drivers
- Matched propagation delay for all channels
- 2.5V logic compatible
- Outputs out of phase with inputs

Product Summary

V_{OFFSET}	600V max.
I_O+/-	160 mA / 360 mA
V_{OUT}	10 - 20V
$t_{on/off}$ (typ.)	1.3 & 0.6 µs
Deadtime (typ.)	700 ns

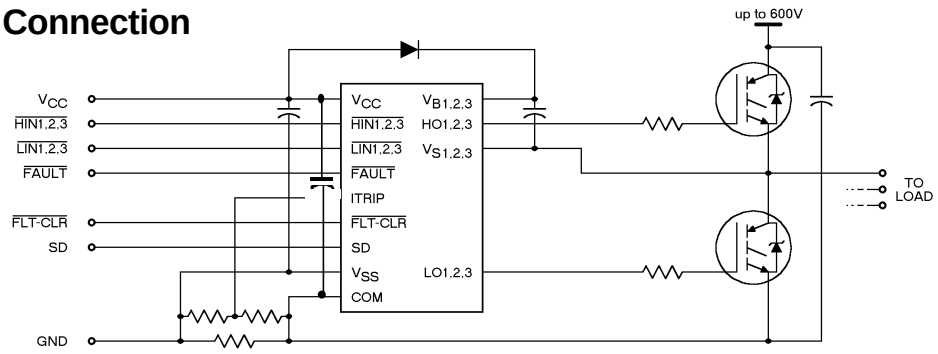
Packages



Description

The IR2131(J)(S) is a high voltage, high speed power MOSFET and IGBT driver with three independent high and low side referenced output channels. Proprietary HVIC technology enables ruggedized monolithic construction. Logic inputs are compatible with CMOS or LSTTL outputs, down to 2.5V logic. A current trip function which terminates all six outputs can be derived from an external current sense resistor. A shutdown input is provided for a customized shutdown function. An open drain $\overline{FAULT}$ signal is provided to indicate that any of the shutdowns has occurred. The output drivers feature a high pulse current buffer stage designed for minimum driver cross-conduction. Propagation delays are matched to simplify use in high frequency applications. The floating channels can be used to drive N-channel power MOSFETs or IGBTs in the high side configuration which operate up to 600 volts.

Typical Connection



(Refer to Lead Assignments for correct pin configuration). This/These diagram(s) show electrical connections only. Please refer to our Application Notes and DesignTips for proper circuit board layout.

Absolute Maximum Ratings

Absolute Maximum Ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to COM. The Thermal Resistance and Power Dissipation ratings are measured under board mounted and still air conditions. Additional Information is shown in Figures 7 through 10.

Parameter		Value		
Symbol	Definition	Min.	Max.	Units
$V_{B1,2,3}$	High Side Floating Supply Voltage	-0.3	625	V
$V_{S1,2,3}$	High Side Floating Offset Voltage	$V_{B1,2,3}$ - 25	$V_{B1,2,3}$ + 0.3	
$V_{HO1,2,3}$	High Side Floating Output Voltage	$V_{S1,2,3}$ - 0.3	$V_{B1,2,3}$ + 0.3	
V_{CC}	Low Side and Logic Fixed Supply Voltage	-0.3	25	
V_{SS}	Logic Ground	V_{CC} - 25	V_{CC} + 0.3	
$V_{LO1,2,3}$	Low Side Output Voltage	-0.3	V_{CC} + 0.3	
V_{IN}	Logic Input Voltage ($\overline{HIN1,2,3}$, $\overline{LIN1,2,3}$, $\overline{FLT-CLR}$, SD & ITRIP)	V_{SS} - 0.3	V_{SS} + 15	
V_{FLT}	$\overline{FAULT}$ Output Voltage	V_{SS} - 0.3	V_{CC} + 0.3	
dV_S/dt	Allowable Offset Supply Voltage Transient	—	50	V/ns
P_D	Package Power Dissipation @ $T_A \leq +25°C$ (28 Lead DIP)	—	1.5	W
	(28 Lead SOIC)	—	1.6	
	(44 Lead PLCC)	—	2.0	
Rth_{JA}	Thermal Resistance, Junction to Ambient (28 Lead DIP)	—	83	°C/W
	(28 Lead SOIC)	—	78	
	(44 Lead PLCC)	—	63	
T_J	Junction Temperature	—	150	°C
T_S	Storage Temperature	-55	150	
T_L	Lead Temperature (Soldering, 10 seconds)	—	300	

Recommended Operating Conditions

The Input/Output logic timing diagram is shown in Figure 1. For proper operation the device should be used within the recommended conditions. All voltage parameters are absolute voltages referenced to COM. The V_S offset rating is tested with all supplies biased at 15V differential.

Parameter		Value		
Symbol	Definition	Min.	Max.	Units
$V_{B1,2,3}$	High Side Floating Supply Voltage	$V_{S1,2,3}$ + 10	$V_{S1,2,3}$ + 20	V
$V_{S1,2,3}$	High Side Floating Offset Voltage	Note 1	600	
$V_{HO1,2,3}$	High Side Floating Output Voltage	$V_{S1,2,3}$	$V_{B1,2,3}$	
V_{CC}	Low Side and Logic Fixed Supply Voltage	10	20	
V_{SS}	Logic Ground	-5	5	
$V_{LO1,2,3}$	Low Side Output Voltage	0	V_{CC}	
V_{IN}	Logic Input Voltage ($\overline{HIN1,2,3}$, $\overline{LIN1,2,3}$, $\overline{FLT-CLR}$, SD & ITRIP)	V_{SS}	V_{SS} + 5	
V_{FLT}	$\overline{FAULT}$ Output Voltage	V_{SS}	V_{CC}	
T_A	Ambient Temperature	-40	125	°C

Note 1: Logic operational for V_S of -5V to +600V. Logic state held for V_S of -5V to $-V_{BS}$. (Please refer to the Design Tip DT97-3 for more details).
Note 2: All input pins, CA- and CAO pins are internally clamped with a 5.2V zener diode.

Dynamic Electrical Characteristics

V_{BIAS} (V_{CC}, $V_{BS1,2,3}$) = 15V, $V_{S1,2,3}$ = V_{SS} = COM, C_L = 1000 pF and T_A = 25°C unless otherwise specified. The dynamic electrical characteristics are defined in Figures 4 through 5.

Symbol	Parameter Definition	Value Min.	Typ.	Max.	Units	Test Conditions
t_{on}	Turn-On Propagation Delay	0.6	1.3	2.0	µs	V_{IN} = 0 & 5V
t_{off}	Turn-Off Propagation Delay	0.2	0.6	1.0		$V_{S1,2,3}$ = 0 to 600V
t_r	Turn-On Rise Time	—	80	150	ns	
t_f	Turn-Off Fall Time	—	40	100		
t_{itrip}	ITRIP to Output Shutdown Propagation Delay	400	700	1000		V_{IN}, V_{ITRIP} = 0 & 5V
t_{bl}	ITRIP Blanking Time	—	400	—		V_{ITRIP} = 1V
t_{flt}	ITRIP to $\overline{FAULT}$ Indication Delay	400	700	1000		V_{IN}, V_{ITRIP} = 0 & 5V
$t_{flt,in}$	Input Filter Time (All Six Inputs)	—	310	—		V_{IN} = 0 & 5V
t_{fltclr}	$\overline{FLT-CLR}$ to $\overline{FAULT}$ Clear Time	400	800	1200		V_{IN}, V_{IT}, V_{FC} = 0&5V
t_{sd}	SD to Output Shutdown Propagation Delay	400	700	1000		V_{IN}, V_{SD} = 0 & 5V
DT	Deadtime	400	700	1200		V_{IN} = 0 & 5V

NOTE: For high side PWM, HIN pulse width must be ≥ 1.5µsec

Static Electrical Characteristics

V_{BIAS} (V_{CC}, $V_{BS1,2,3}$) = 15V, $V_{S1,2,3}$ = V_{SS} = COM and T_A = 25°C unless otherwise specified. The V_{IN}, V_{TH} and I_{IN} parameters are referenced to V_{SS} and are applicable to all six logic input leads: $\overline{HIN1,2,3}$ & $\overline{LIN1,2,3}$. The V_O and I_O parameters are referenced to COM and $V_{S1,2,3}$ and are applicable to the respective output leads: HO1,2,3 or LO1,2,3.

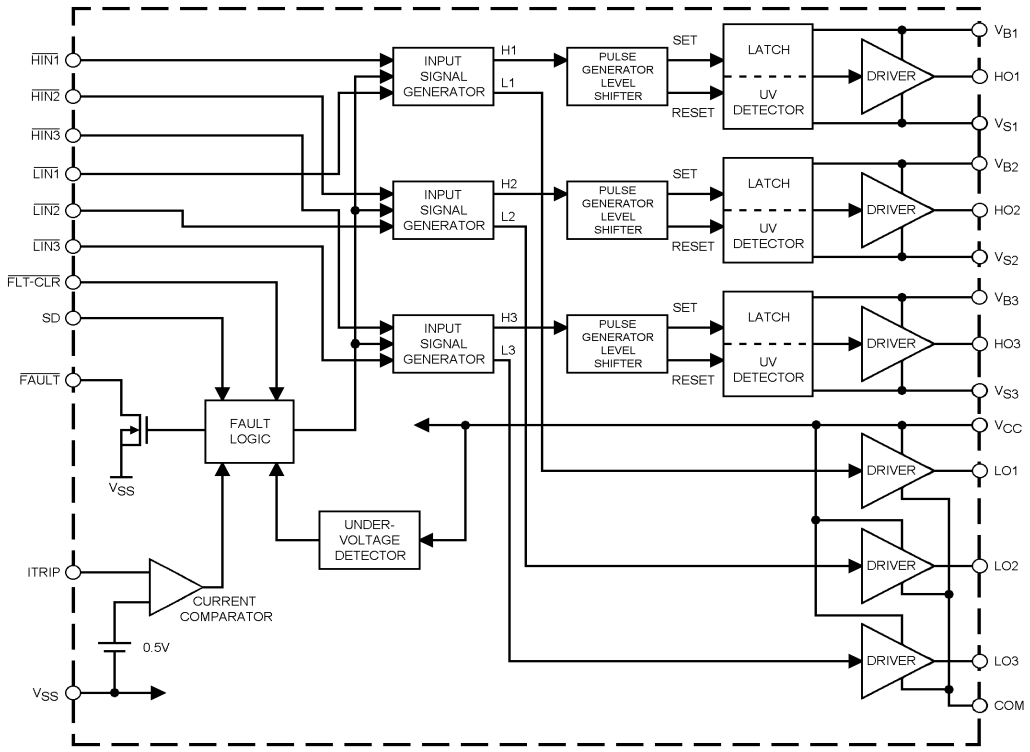
Symbol	Parameter Definition	Value Min.	Typ.	Max.	Units	Test Conditions
V_{IH}	Logic "0" Input Voltage (OUT = LO)	2.2	—	—	V	
V_{IL}	Logic "1" Input Voltage (OUT = HI)	—	—	0.8		
$V_{FCLR,IH}$	Logic "0" Fault Clear Input Voltage	2.2	—	—		
$V_{FCLR,IL}$	Logic "1" Fault Clear Input Voltage	—	—	0.8		
$V_{SD,TH+}$	Shutdown Input Positive Going Threshold	1.2	1.8	2.1		
$V_{SD,TH-}$	Shutdown Input Negative Going Threshold	0.9	1.5	1.8		
$V_{IT,TH+}$	ITRIP Input Positive Going Threshold	250	485	600	mV	
$V_{IT,TH-}$	ITRIP Input Negative Going Threshold	200	400	550		
V_{OH}	High Level Output Voltage, V_{BIAS} - VO	—	—	100		V_{IN} = 0V, I_O = 0A
V_{OL}	Low Level Output Voltage, VO	—	—	100		V_{IN} = 5V, I_O = 0A
I_{LK}	Offset Supply Leakage Current	—	—	50	µA	V_B = V_S = 600V
I_{QBS}	Quiescent V_{BS} Supply Current	—	30	100		V_{IN} = 0V or 5V
I_{QCC}	Quiescent V_{CC} Supply Current	—	3.0	4.5	mA	V_{IN} = 0V or 5V
I_{IN+}	Logic "1" Input Bias Current (OUT = HI)	—	190	300	µA	V_{IN} = 0V
I_{IN-}	Logic "0" Input Bias Current (OUT = LO)	—	50	100		V_{IN} = 5V
I_{ITRIP+}	"High" ITRIP Bias Current	—	75	150		ITRIP = 5V
I_{ITRIP-}	"Low" ITRIP Bias Current	—	—	100	nA	ITRIP = 0V
I_{FCLR+}	Logic "1" Fault Clear Bias Current	—	125	250	µA	$\overline{FLT-CLR}$ = 0V
I_{FCLR-}	Logic "0" Fault Clear Bias Current	—	75	150		$\overline{FLT-CLR}$ = 5V
I_{SD+}	Logic "1" Shutdown Bias Current	—	75	150		SD = 5V
I_{SD-}	Logic "0" Shutdown Bias Current	—	—	100	nA	SD = 0V

Static Electrical Characteristics -- Continued

V_{BIAS} (V_{CC}, $V_{BS1,2,3}$) = 15V, $V_{S1,2,3}$ = V_{SS} = COM and T_A = 25°C unless otherwise specified. The V_{IN}, V_{TH} and I_{IN} parameters are referenced to V_{SS} and are applicable to all six logic input leads: $\overline{HIN1,2,3}$ & $\overline{LIN1,2,3}$. The V_O and I_O parameters are referenced to COM and $V_{S1,2,3}$ and are applicable to the respective output leads: HO1,2,3 or LO1,2,3.

Parameter		Value				
Symbol	Definition	Min.	Typ.	Max.	Units	Test Conditions
V_{BSUV+}	V_{BS} Supply Undervoltage Positive Going Threshold	8.2	8.7	9.2	V	
V_{BSUV-}	V_{BS} Supply Undervoltage Negative Going Threshold	7.8	8.3	8.8		
V_{CCUV+}	V_{CC} Supply Undervoltage Positive Going Threshold	8.2	8.7	9.2		
V_{CCUV-}	V_{CC} Supply Undervoltage Negative Going Threshold	7.8	8.3	8.8		
$R_{on,FLT}$	$\overline{FAULT}$ Low On-Resistance	—	55	75	Ω	
I_{O+}	Output High Short Circuit Pulsed Current	160	250	—	mA	V_O = 0V, V_{IN} = 0V PW ≤ 10 µs
I_{O-}	Output Low Short Circuit Pulsed Current	360	500	—		V_O = 15V, V_{IN} = 5V PW ≤ 10 µs

Functional Block Diagram

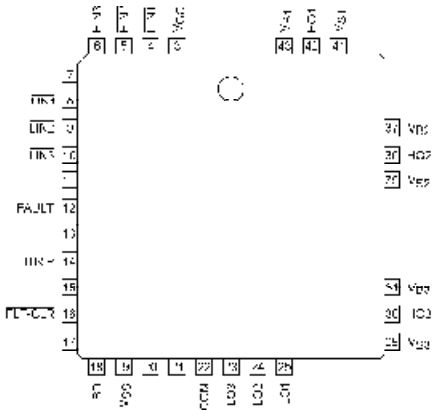


Lead Definitions

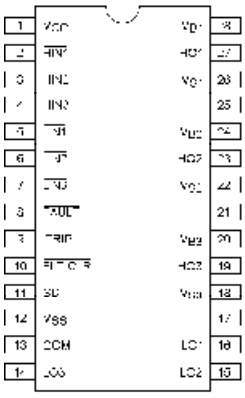
Lead Symbol	Description
$\overline{HIN1,2,3}$	Logic inputs for high side gate driver outputs (HO1,2,3), out of phase
$\overline{LIN1,2,3}$	Logic inputs for low side gate driver output (LO1,2,3), out of phase
$\overline{FLT-CLR}$	Logic input for fault clear
SD	Logic input for shutdown
$\overline{FAULT}$	Indicates over-current or undervoltage lockout (low side) has occurred, negative logic
V_{CC}	Low side and logic fixed supply
ITRIP	Input for over-current shutdown
V_{SS}	Logic ground
$V_{B1,2,3}$	High side floating supplies
HO1,2,3	High side gate drive outputs
$V_{S1,2,3}$	High side floating supply returns
LO1,2,3	Low side gate drive outputs
COM	Low side return

Lead Assignments

28 Lead DIP



44 Lead PLCC w/o 12 Leads



28 Lead SOIC (Wide Body)

IR2131	IR2131J	IR2131S
Part Number		

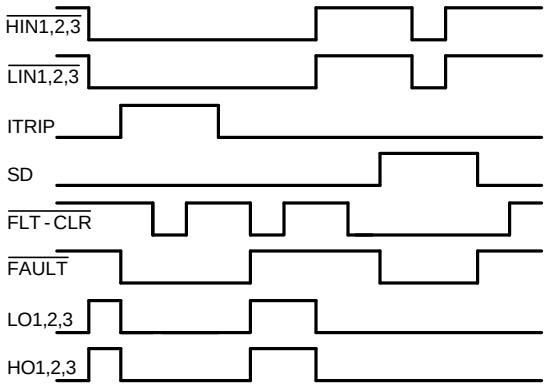


Figure 1. Input/Output Timing Diagram

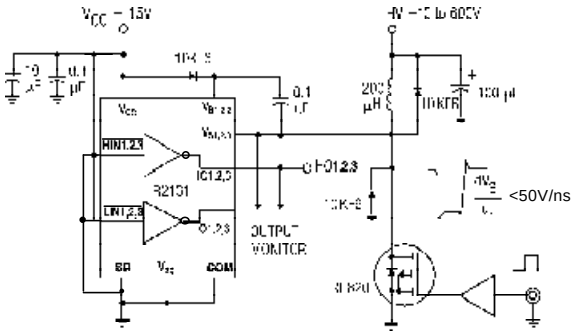


Figure 2. Floating Supply Voltage Transient Test Circuit

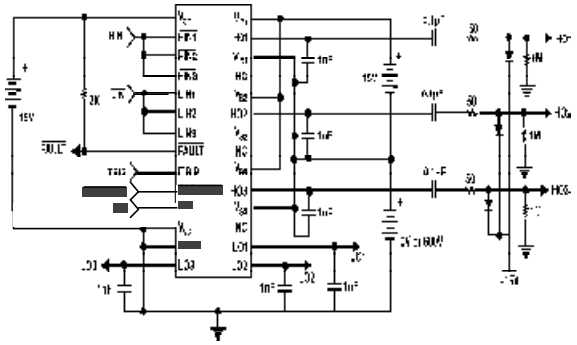


Figure 3. Switching Time Test Circuit

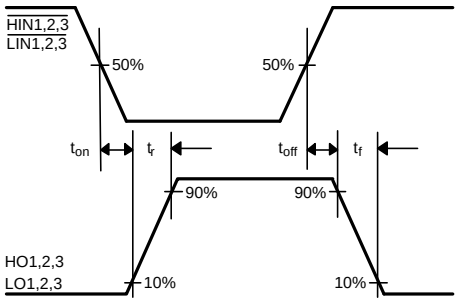


Figure 4. Switching Time Waveform Definitions

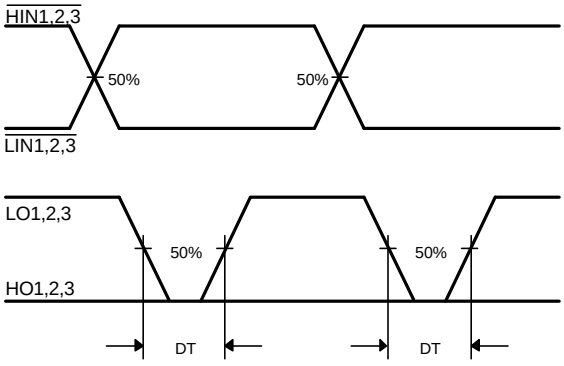


Figure 5. Deadtime Waveform Definitions

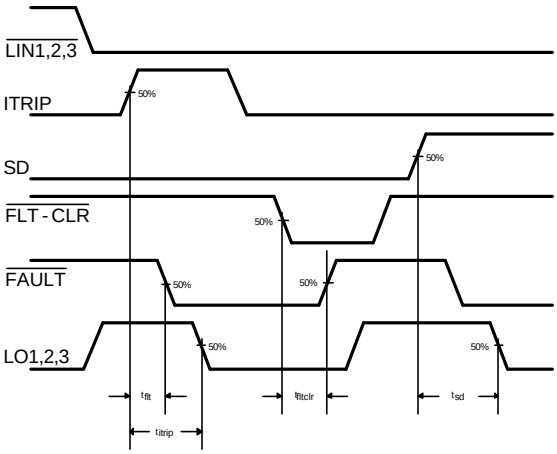


Figure 6. Shutdown Waveform Definitions

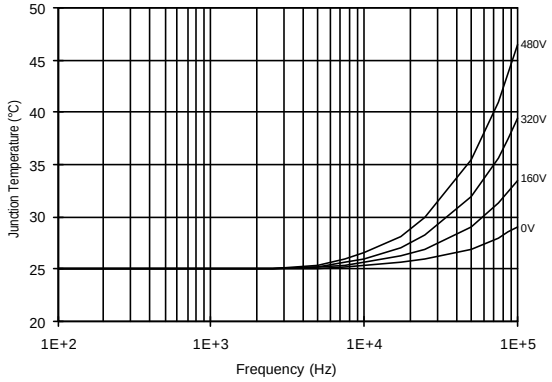


Figure 7. IR2131 T_J vs. Frequency (IRF820)
R_{GATE} = 33Ω, V_{CC} = 15V

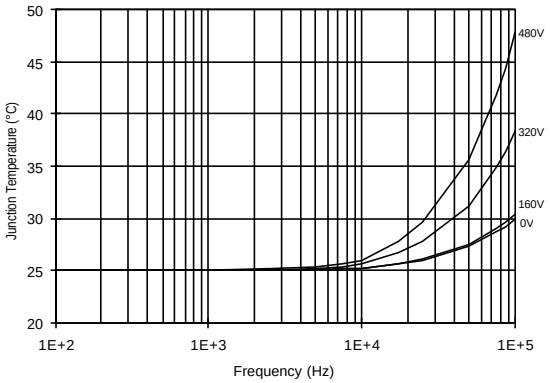


Figure 8. IR2131 T_J vs. Frequency (IRF830)
R_{GATE} = 20Ω, V_{CC} = 15V

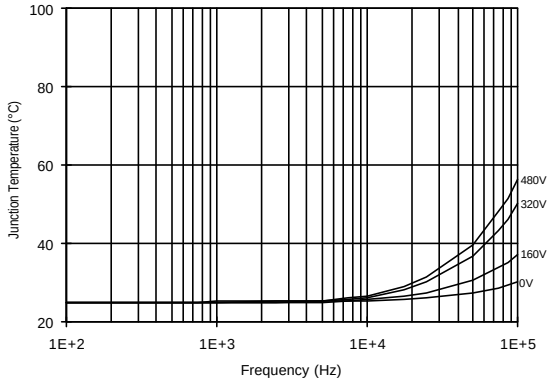


Figure 9. IR2131 T_J vs. Frequency (IRF840)
R_{GATE} = 15Ω, V_{CC} = 15V

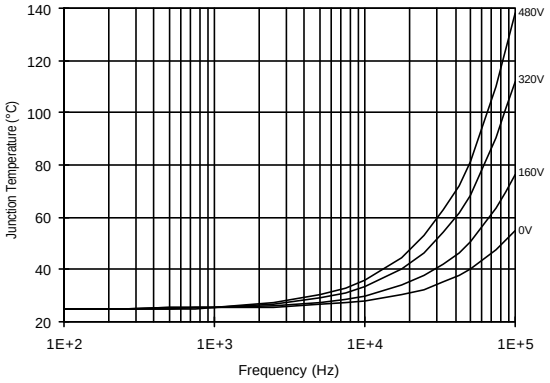
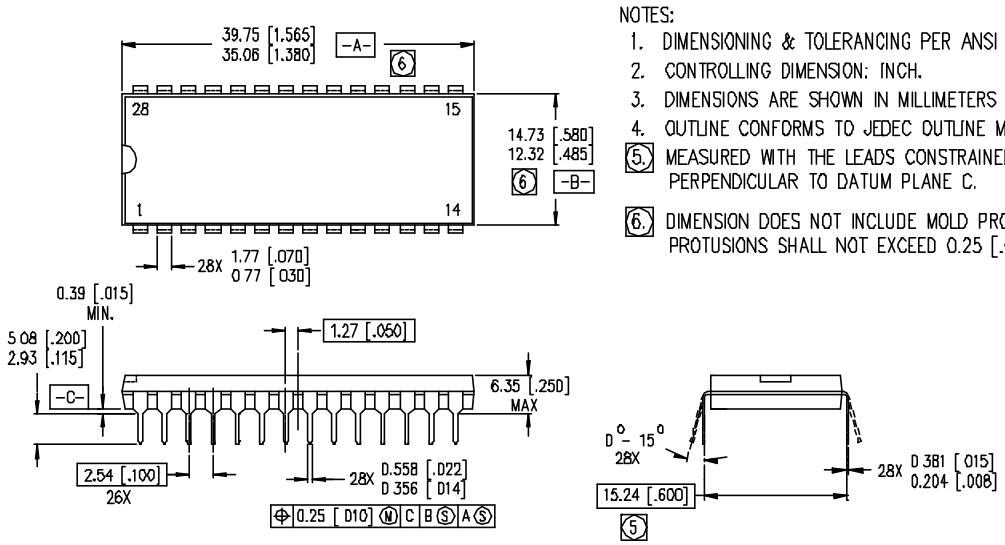


Figure 10. IR2131 T_J vs. Frequency (IRF450)
R_{GATE} = 10Ω, V_{CC} = 15V

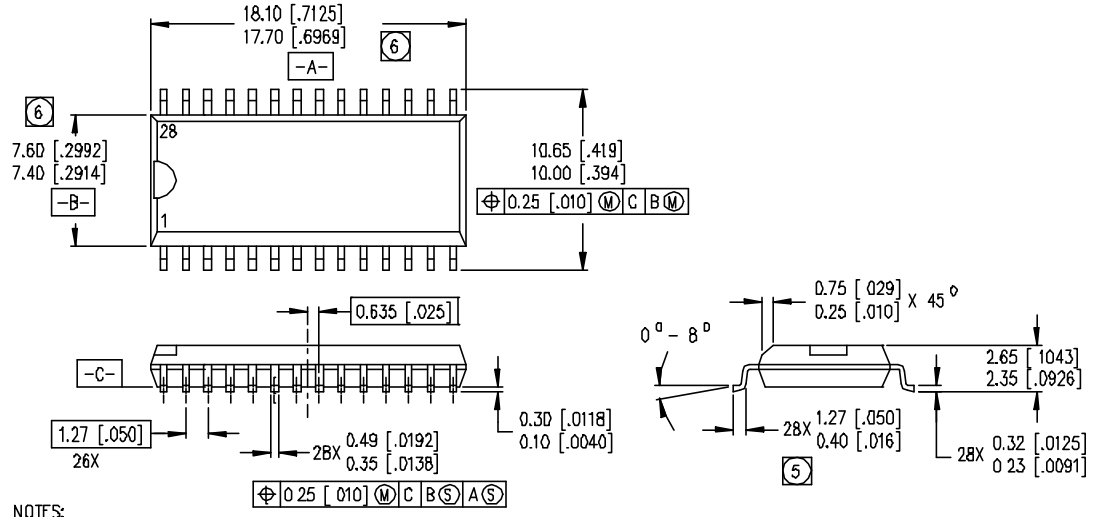
Case outlines



NOTES:
1. DIMENSIONING & TOLERANCING PER ANSI Y14.5M-1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
4. OUTLINE CONFORMS TO JEDEC OUTLINE MS-011AB.
5. MEASURED WITH THE LEADS CONSTRAINED TO BE PERPENDICULAR TO DATUM PLANE C.
6. DIMENSION DOES NOT INCLUDE MOLD PROTUSIONS. MOLD PROTUSIONS SHALL NOT EXCEED 0.25 [.010].

28-Lead PDIP (wide body)

01-6011
01-3024 02 (MS-011AB)

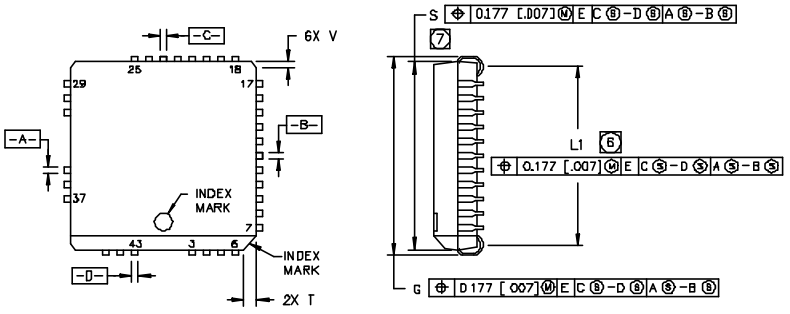


NOTES:
1. DIMENSIONING & TOLERANCING PER ANSI Y14.5M-1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
4. OUTLINE CONFORMS TO JEDEC OUTLINE MS-013AE.

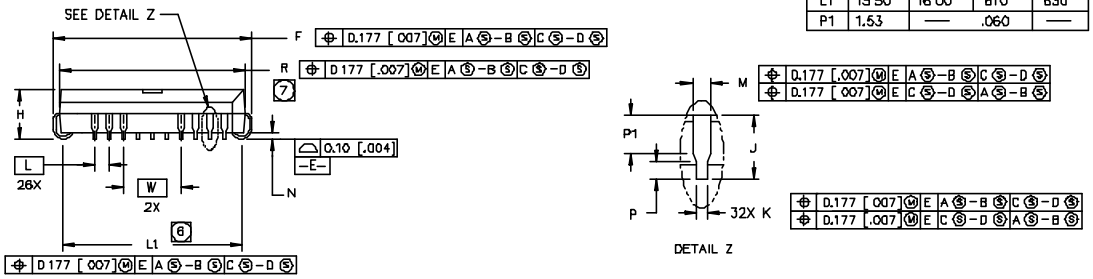
5. DIMENSION IS THE LENGTH OF LEAD FOR SOLDERING TO A SUBSTRATE.
6. DIMENSION DOES NOT INCLUDE MOLD PROTUSIONS. MOLD PROTUSIONS SHALL NOT EXCEED 0.15 [.006].

28-Lead SOIC (wide body)

01-6013
01-3040 02 (MS-013AE)



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
F	17.40	17.65	.685	.695
G	17.40	17.65	.685	.695
H	4.20	4.57	.165	.180
J	2.29	3.04	.090	.120
K	0.33	0.48	.013	.019
L	1.27 BSC		.050 BSC	
M	0.66	0.81	.026	.032
N	0.51	—	020	—
P	0.64	—	.025	—
R	16.51	16.66	650	656
S	16.51	16.66	.650	.656
T	1.07	1.21	042	048
V	—	0.50	—	020
W	5.08 BSC		.200 BSC	
L1	15.50	16.00	610	630
P1	1.53	—	.060	—



NOTES

1. DIMENSIONING & TOLERENCING PER ANSI Y14.5M-1982.
2. DIMENSIONS SHOWN IN MILLIMETERS [INCHES].
3. CONTROLLING DIMENSION: INCH
4. CONFORMS TO JEDEC OUTLINE MS-018AC.
5. DATUMS -A-, -B-, -C-, & -D- ARE DETERMINED BY WHERE THE TOP OF THE LEADS EXIT PLASTIC BODY AT MOLD PARTING LINE.

(6) TO BE MEASURED AT -E- SEATING PLANE.

(7) DIMENSIONS DO NOT INCLUDE MOLD FLASH, ALLOWABLE FLASH IS 0.254 [.010].

01-6009 00

44-Lead PLCC w/o 12 leads

01-3004 02(mod.) (MS-018AC)