MT90401

SONET/SDH System Synchronizer

Product Brief

PB5429 ISSUE 4 January 2001

Features

- Meets requirements of Telcordia GR-253-CORE for SONET internal clocks and GR-1244-CORE for Stratum 3 clocks
- Meets requirements of ITU-T G.813 Option 1 and Option 2 for SDH Equipment Clocks (SEC)
- Provides OC-3/STM-1, DS3, E3, 19.44MHz, DS2, E1, T1, 8kHz and ST-BUS clock outputs
- Accepts two independent reference inputs
- Selectable 1.544MHz, 2.048MHz, 19.44MHz or 8kHz input reference frequencies
- Holdover accuracy of 0.02 ppm
- Intrinsic jitter under 200 picoseconds pk-pk unfiltered on the 19.44MHz and 155.52MHz clocks
- Output clock phase can be trimmed to support master-slave arrangements
- Hardware Mode, or optional Microport Mode with 8 bit microprocessor port access
- 3.3V supply
- JTAG boundary scan

Applications

- SONET/SDH Add/Drop multiplexers
- SONET/SDH uplinks
- Integrated access devices
- ATM edge switches

Ordering Information

MT90401AB 80 Pin LQFP

-40 to +85°C

Description

The MT90401 is a digital phase locked loop (DPLL) that is designed to synchronize SDH (Synchronous Digital Hierarchy) and SONET (Synchronous Optical Network) networking equipment. The MT90401 is used to ensure that the timing of outgoing signals remains within the limits specified by Telcordia, ANSI and the ITU during normal operation and in the presence of disturbances on the incoming synchronization signals.

The MT90401 can operate in free-run, locked or holdover mode. The loop filter corner frequency can be selected to suit SONET applications or to suit SDH applications. The MT90401 uses an external 20MHz oscillator as its master clock and it does not require external loop filter components.

In Hardware Mode, the MT90401 can be controlled and monitored via external pins. In Microport Mode, a microprocessor can be used for more comprehensive control and monitoring.

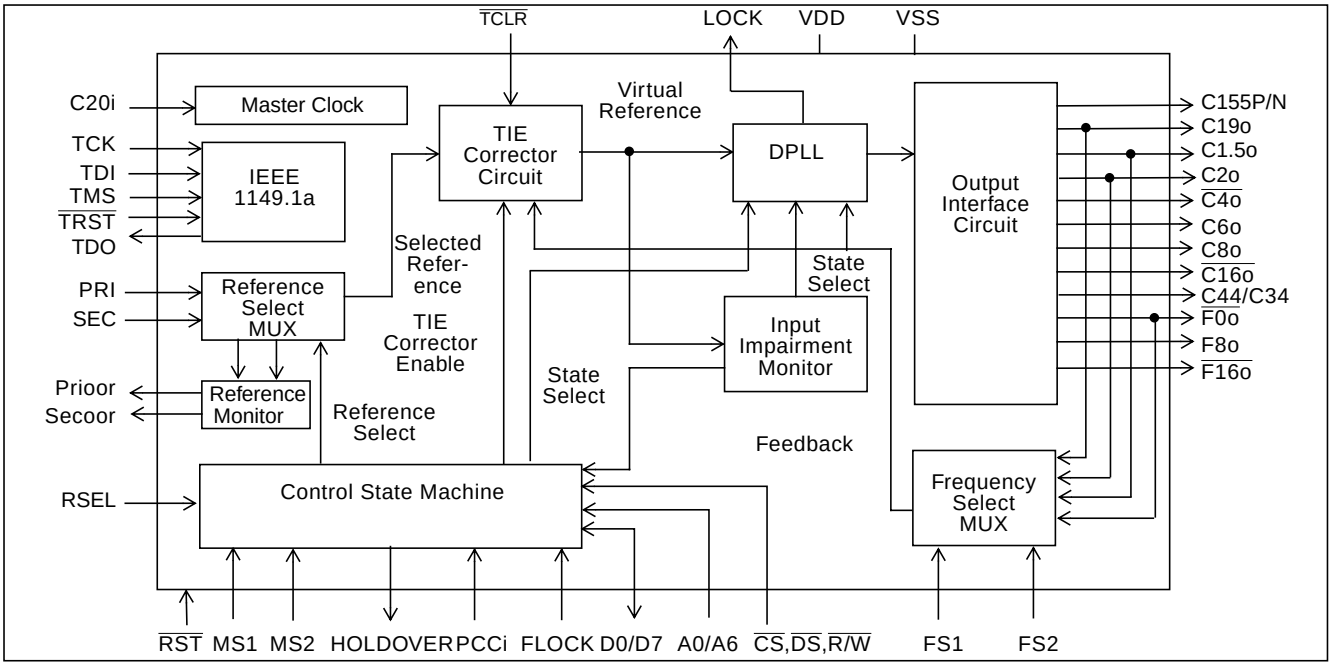


Figure 1 - Functional Block Diagram

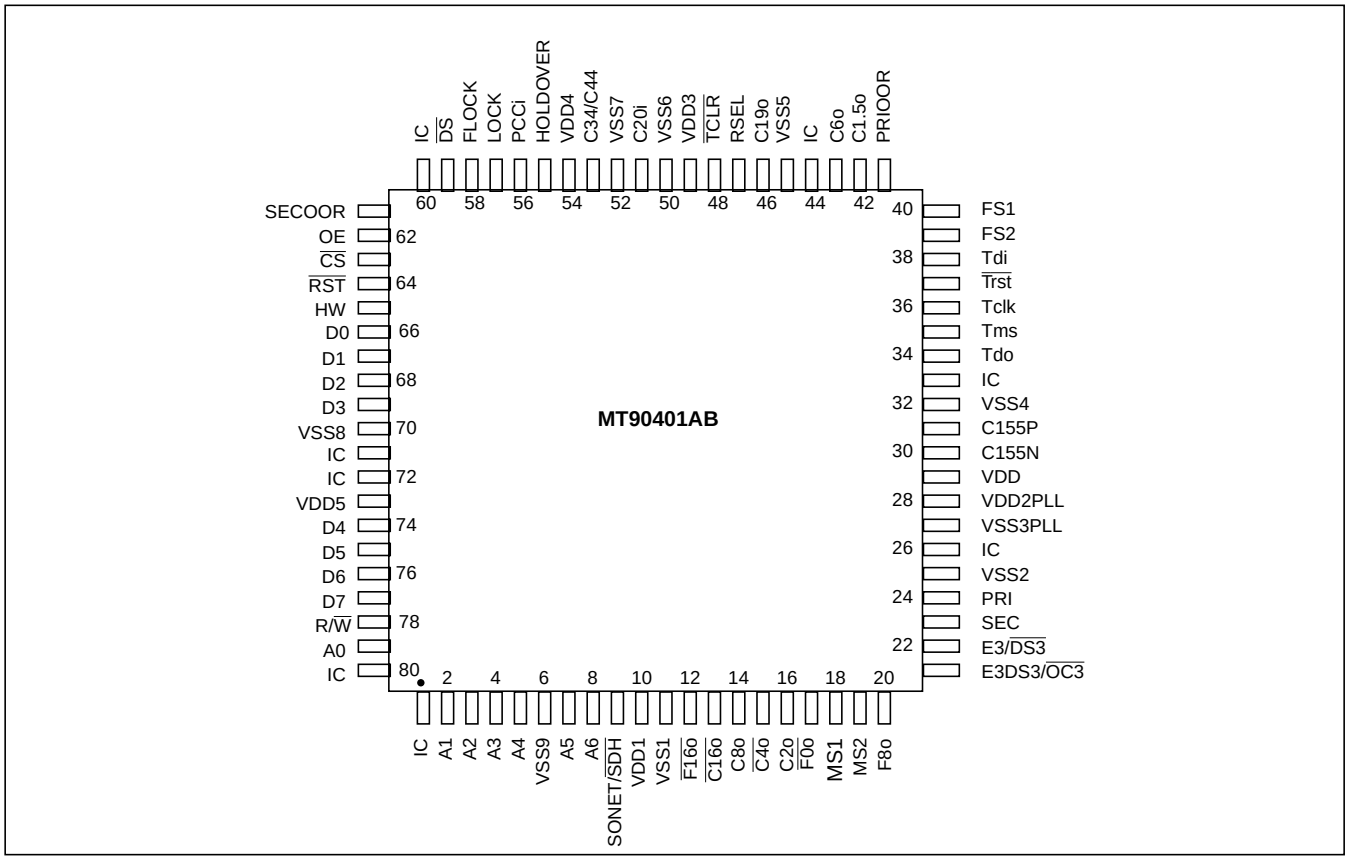


Figure 2 - Pin Connections 80 Pin LQFP for MT90401

Pin Description

Pin #	Name	Description
1	IC	**Internal Connection**. Leave unconnected.
2-5	A1 - A4	**Address 1 to 4 (5V tolerant Inputs).** Address and control inputs for the non-multiplexed parallel processor interface.
6	V_{SS9}	**Digital ground.** 0 Volts
7, 8	A5, A6	**Address 5, Address 6 (5V tolerant Input).** Address and control input for the non-multiplexed parallel processor interface.
9	SONET/$\overline{SDH}$	**SONET/$\overline{SDH}$ (Input).** In hardware mode set this pin high to have a loop filter corner frequency of 70 millihertz and limit the phase slope to 885 ns per second. Set this pin low to have a corner frequency of approximately 1.1 hertz and limit the phase slope to 50 ns per 125 microseconds. This pin performs no function if the device is not in hardware mode.
10	V_{DD1}	**Positive Power Supply.** Digital supply (+3.3V $\pm$5%).
11	V_{SS1}	**Digital ground.** 0 Volts
12	$\overline{F16o}$	**Frame Pulse ST-BUS 8.192 Mb/s (CMOS Output).** This is an 8kHz 61ns active low framing pulse, which marks the beginning of an ST-BUS frame. This is typically used for ST-BUS operation at 8.192 Mb/s.
13	$\overline{C16o}$	**Clock 16.384MHz (CMOS Output).** This output is used for ST-BUS operation with a 16.384MHz clock.

Pin Description (continued)

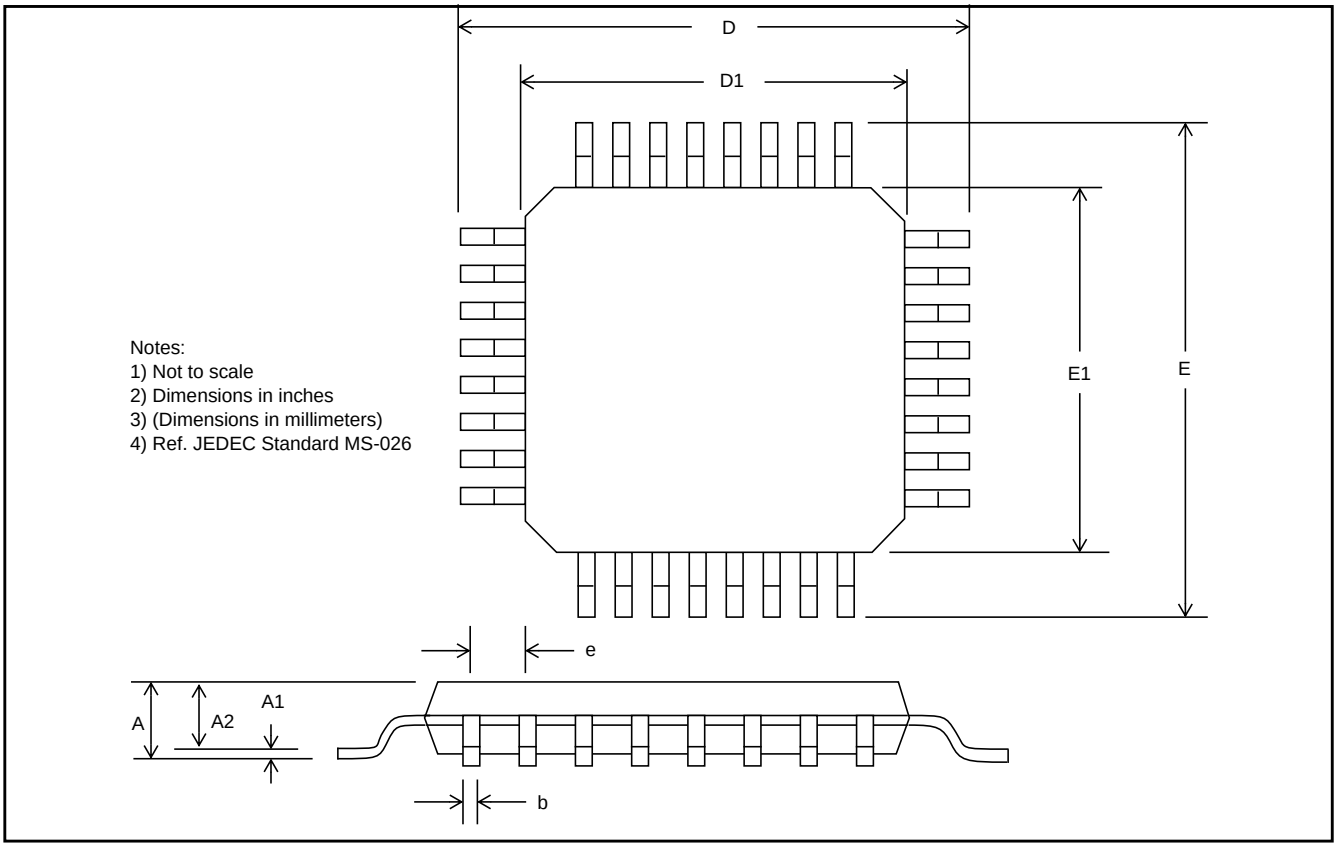
Pin #	Name	Description
14	C8o	**Clock 8.192MHz (CMOS Output).** This output is used for ST-BUS operation at 8.192Mb/s.
15	$\overline{\text{C4o}}$	**Clock 4.096MHz (CMOS Output).** This output is used for ST-BUS operation at 2.048Mb/s and 4.096Mb/s.
16	C2o	**Clock 2.048MHz (CMOS Output).** This output is used for ST-BUS operation at 2.048Mb/s.
17	$\overline{\text{F0o}}$	**Frame Pulse ST-BUS 2.048Mb/s (CMOS Output).** This is an 8kHz 244ns active low framing pulse, which marks the beginning of an ST-BUS frame. This is typically used for ST-BUS operation at 2.048Mb/s and 4.096Mb/s.
18	MS1	**Mode/Control Select 1 (Input).** The logic level at this input is gated in by the rising edge of F8o. See pin description for MS2. This pin performs no function if the device is not in hardware mode.
19	MS2	**Mode/Control Select 2 (Input).** This input determines the state (Normal, Holdover or Freerun) of operation. The logic level at this input is gated in by the rising edge of F8o. This pin performs no function if the device is not in hardware mode.
20	F8o	**Frame Pulse Generic (CMOS Output).** This is an 8kHz 122ns active high framing pulse, which marks the beginning of a TDM frame. This is typically used for TDM streams operating at 8.192 Mb/s.
21	E3DS3/$\overline{\text{OC3}}$	**E3DS3 or OC-3 Selection (Input).** In Hardware Mode a low on this pin enables the differential 155.52MHz output clock on the C155N/C155P pins; this will also cause the C34/C44 pin to output its nominal clock frequency divided by 4. In Hardware Mode, a high on this pin disables the differential 155.52MHz output clock on the C155N/C155P pins; this will also cause the C34/C44 pin to output its nominal clock frequency. This pin performs no function if the device is not in Hardware Mode.
22	E3/$\overline{\text{DS3}}$	**E3 or DS3 Selection (Input).** In Hardware Mode a low on this pin selects a clock rate of 44.736MHz for the C34/C44 pin, while a high selects a clock rate of 34.368MHz. This pin performs no function if the device is not in hardware mode.
23	SEC	**Secondary Reference (Input).** This is one of two (PRI & SEC) input reference sources (falling edge) used for synchronization. One of four possible frequencies (8kHz, 1.544MHz, 2.048MHz or 19.44MHz) may be used. In hardware mode the selection of the input reference is based upon the MS1, MS2 and RSEL control inputs.
24	PRI	**Primary Reference (Input).** This is one of two (PRI & SEC) input reference sources (falling edge) used for synchronization. One of four possible frequencies (8kHz, 1.544MHz, 2.048MHz or 19.44MHz) may be used. In hardware mode the selection of the input reference is based upon the MS1, MS2 and RSEL control inputs.
25	V_{SS2}	**Digital ground.** 0 Volts
26	IC	**Internal Connection.** Leave unconnected
27	V_{SS3} PLL	**Analog ground.** 0 Volts
28	V_{DD2}PLL	**Positive Analog Power Supply.** Analog supply (+3.3V ±5%).
29	VDD_3	**Positive Power Supply.** Digital supply (+3.3V ±5%).
30 31	C155N, C155P	**LVDS 155.52 MHz (Output)).** Differential outputs generating a 155.52MHz clock
32	VSS_4	**Digital ground.** 0 Volts
33	IC	**Internal Connection.** Leave unconnected
34	Tdo	**IEEE 1149.1a Test Data Output (Output).** If not used, this pin should be left unconnected.

Pin Description (continued)

Pin #	Name	Description
35	Tms	**IEEE 1149.1a Test Mode Selection (Input)**. If not used, this pin should be pulled high.
36	Tclk	**IEEE 1149.1a Test Clock Signal (Input)**. If not used, this pin should be pulled high.
37	$\overline{\text{Trst}}$	**IEEE 1149.1a Reset Signal (Input).** If not used, this pin should be held low.
38	Tdi	**IEEE 1149.1a Test Data Input (Input).** If not used, this pin should be pulled high.
39	FS2	**Frequency Select 2 (Input).** This input, in conjunction with FS1, selects which of four possible frequencies (8kHz, 1.544MHz, 2.048MHz or 19.44MHz) may be input to the PRI and SEC inputs.
40	FS1	**Frequency Select 1 (Input).** This input, in conjunction with FS2, selects which of four possible frequencies (8kHz, 1.544MHz, 2.048MHz or 19.44MHz) may be input to the PRI and SEC inputs.
41	PRIOOR	**Primary Reference Out Of Range (CMOS Output).** A logic high at this pin indicates that the primary reference is off the PLL center frequency by more than 12 ppm. The calibration is done on a 1 second basis using a signal derived from the 20MHz clock input on C20i. When the accuracy of the 20MHz clock is ± 4.6ppm the effective out of range limits of the PRIOOR pin will be ±16.6ppm.
42	$\overline{\text{C1.5o}}$	**Clock 1.544MHz (CMOS Output).** This output is used in T1 applications.
43	C6	**Clock 6.312MHz (CMOS Output).** This output is used for DS2 or J2 applications.
44	IC	**Internal Connection.**Tie low for normal operation**.**
45	VSS_5	**Digital ground.** 0 Volts
46	C19o	**Clock 19.44MHz (CMOS Output).** This output is used in OCN/STS-N and STM-N applications.
47	RSEL	**Reference Source Select (Input).** A logic low selects the PRI (primary) reference source as the input reference signal and a logic high selects the SEC (secondary) input. The logic level at this input is gated in by the rising edge of F8o.
48	$\overline{\text{TCLR}}$	**TIE Circuit Clear (Input).** A logic low at this input clears the Time Interval Error (TIE) correction circuit resulting in a realignment of output phase with input phase. The $\overline{\text{TCLR}}$ pin should be held low for a minimum of 300ns. When this pin is held low, the time interval error correction circuit is disabled.
49	VDD_3	**Positive Power Supply. Digital supply** (+3.3V ±5%).
50	VSS_6	**Digital ground.** 0 Volts.
51	C20i	**20 MHz Clock Input (5V tolerant Input).** This pin is the input for the master 20MHz clock.
52	V_{SS7}	**Digital ground.** 0Volts
53	C34/C44	**Controlled Clock 34.368MHz / Clock 44.736MHz (CMOS Output).** This output clock is programmable to be either 34.368MHz (for E3 applications) or 44.736MHz (for DS3 applications). The output clock is controlled via control pins in Hardware Mode or control bits when the device is in Microport Mode. If the E3DS3/$\overline{\text{OC3}}$ control pin (in hardware mode) or if the E3DS3/$\overline{\text{OC3}}$ control bit (in microport mode) is high, the C34/C44 pin will output its nominal frequency. If the E3DS3/OC3 control pin or control bit is low, the C34/C44 pin will output its nominal frequency divided by 4. (C8.5o/C11o)
54	V_{DD4}	**Positive Power Supply.** Digital supply (+3.3V ±5%).
55	HOLDOVER	**Holdover (CMOS Output).** This output goes high when the device is in holdover mode.

Pin Description (continued)

Pin #	Name	Description
56	PCCi	**Phase Continuity Control Input (3V Input).** The signal at this pin affects the state changes between Primary Holdover Mode and Primary Normal Mode and Primary Holdover Mode and Secondary Normal Mode. The logic level at this input is gated by the rising edge of F8o.
57	LOCK	**Lock Indicator (CMOS Output).** This output goes high when the PLL is in frequency lock to the input reference.
58	FLOCK	**Fast Lock Mode (Input).** In hardware mode, hold this pin high to lock 8 times faster than normal to the input reference. This pin performs no function if the device is not in hardware mode. In Fast Lock Mode, the wander generation of the PLL is, of necessity, compromised.
59	$\overline{DS}$	**Data Strobe (5V tolerant Input)**. This input is the active low data strobe of the Motorola processor interface.
60	IC	**Internal Connection.** Tie low for normal operation.
61	SECOOR	**Secondary Reference Out Of Capture Range (CMOS Output).** A logic high at this pin indicates that the secondary reference is off the PLL center frequency by more than 12 ppm. The calibration is done on a 1 second basis using a signal derived from the 20MHz clock input on the C20i pin. When the accuracy of the 20MHz clock is $\pm$ 4.6ppm the effective out of range limits of the SECOOR pin will be $\pm$16.6ppm.
62	OE	**Output Enable (Input)**. Tie high for normal operation. Tie low to force output clocks pins $\overline{F16}$, $\overline{C16}$, C8, $\overline{C4}$, C2, $\overline{F0}$ to a high impedance state.
63	CS	**Chip Select (5V tolerant Input)**. This active low input enables the non-multiplexed Motorola parallel microprocessor interface of the MT90401. When $\overline{CS}$ is set to high, the microprocessor interface is idle and all bus I/O pins will be in a high impedance state.
64	$\overline{RST}$	**RESET (5V tolerant Input).** This active low input puts the MT90401 in a reset condition. $\overline{RST}$ should be set to high for normal operation. The MT90401 should be reset after power-up and after the selected reference frequency is changed. The $\overline{RST}$ pin must be held low for a minimum of 1µsec. to reset the device properly.
65	HW	**Hardware Mode (Input)**. If this pin is tied low, the device is in microport mode and is controlled via the microport. If it is tied high, the device is in hardware mode and is controlled via the control pins MS1, MS2, FS1, FS2, FLOCK and SONET/$\overline{SDH}$.
66-69	D0 - D3	**Data 0 to Data 3 (5V tolerant Three-state I/O)**. These signals combined with D0,D1 and D4-D7 form the bidirectional data bus of the parallel processor interface (D0 is the least significant bit).
70	V_{SS8}	**Digital ground.** 0 Volts.
71	IC	**Internal Connection.** Tie low for normal operation.
72	IC	**Internal Connection.** Tie low for normal operation.
73	V_{DD5}	**Positive Power Supply.** Digital supply (+3.3V $\pm$5%).
74-77	D4 - D7	**Data 4 to Data 7 (5V tolerant Three-state I/O).** These signals combined with D0-D3 form the bidirectional data bus of the parallel processor interface (D7 is the most significant bit).
78	R/$\overline{W}$	**Read/$\overline{Write}$ Strobe (5V tolerant Input).** In Motorola mode (R/$\overline{W}$), this input controls the direction of the data bus D[0:7] during a microprocessor access. When R/$\overline{W}$ is high, the parallel processor is reading data from the MT90401. When low, the parallel processor is writing data to the MT90401.
79	A0	**Address 0 (5V tolerant Input).** Address and control input for the non-multiplexed parallel processor interface. A0 is the least significant input.
80	IC	**Internal Connection.** Tie low for normal operation.



Dim	80-Pin		100-Pin		128-Pin		208-Pin		256-Pin	
	Min	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**
A	-	0.063 (1.60)	-	0.063 (1.60)	-	0.063 (1.60)	-	0.063 (1.60)	-	0.063 (1.60)
A1	0.002 (0.05)	0.006 (0.15)	0.002 (0.05)	0.006 (0.15)	0.002 (0.05)	0.006 (0.15)	0.002 (0.05)	0.006 (0.15)	0.002 (0.05)	0.006 (0.15)
A2	0.053 (1.35)	0.057 (1.45)	0.053 (1.35)	0.057 (1.45)	0.053 (1.35)	0.057 (1.45)	0.053 (1.35)	0.057 (1.45)	0.053 (1.35)	0.057 (1.45)
b	0.009 (0.22)	0.015 (0.38)	0.007 (0.17)	0.011 (0.27)	0.001 (0.17)	0.011 (0.27)	0.001 (0.17)	0.011 (0.27)	0.005 (0.13)	0.009 (0.23)
D	0.630 (16.00 BSC)		0.630 (16.00 BSC)		0.866 (22.00 BSC)		1.181 (30.00 BSC)		1.181 (30.00 BSC)	
D1	0.551 (14.00 BSC)		0.551 (14.00 BSC)		0.787 (20.00 BSC)		1.102 (28.00 BSC)		1.102 (28.00 BSC)	
e	0.025 (0.65 BSC)		0.020 (0.50 BSC)		0.020 (0.50 BSC)		0.020 (0.50 BSC)		0.016 (0.40 BSC)	
E	0.630 (16.00 BSC)		0.630 (16.00 BSC)		0.630 (16.00 BSC)		1.181 (30.00 BSC)		1.181 (30.0 BSC)	
E1	0.551 (14.00 BSC)		0.551 (14.00 BSC)		0.551 (14.00 BSC)		1.102 (28.00 BSC)		1.102 (28.00 BSC)	

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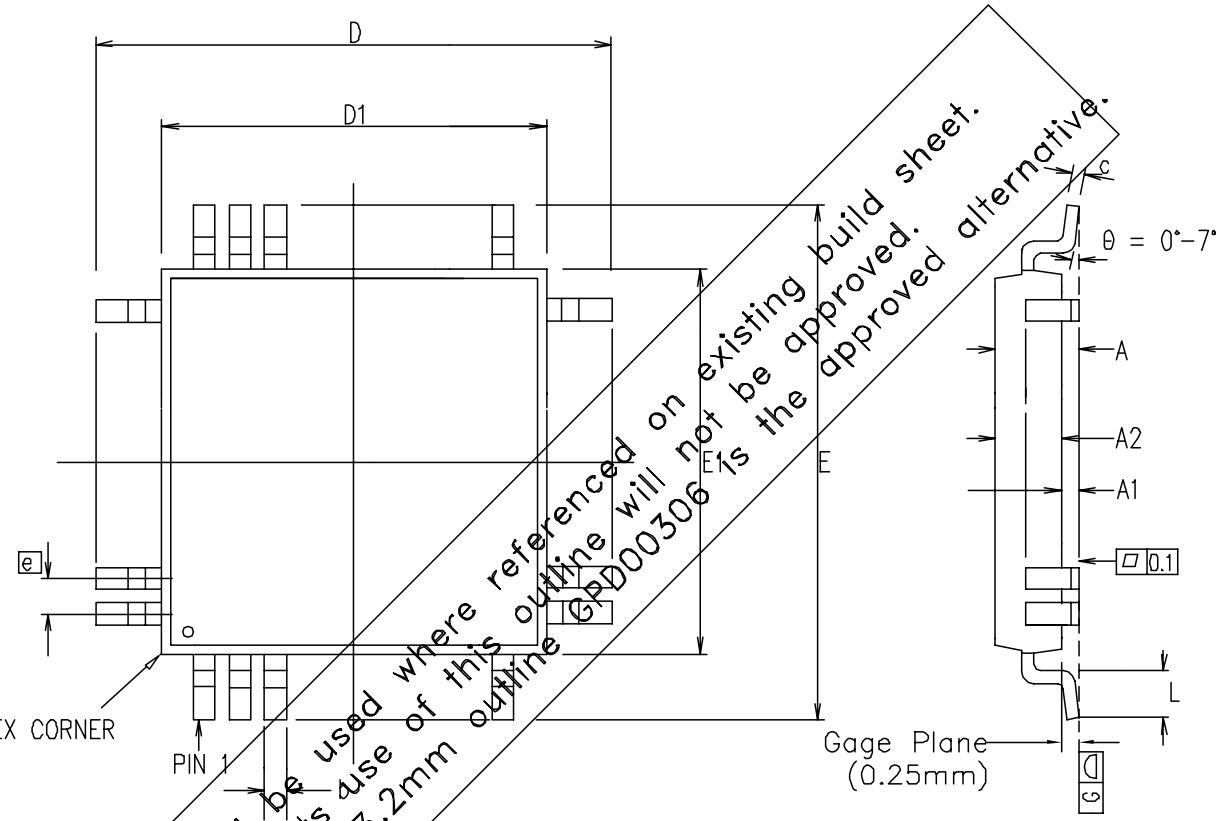

Symbol	Control Dimensions in millimetres			Altern. Dimensions in inches	
	MIN	MAX		MIN	MAX
A	---	3.40		---	0.134
A1	0.25	---		0.010	---
A2	2.55	3.05		0.100	0.120
D	23.90 BSC			0.941 BSC	
D1	20.00 BSC			0.787 BSC	
E	17.90 BSC			0.705 BSC	
E1	14.00 BSC			0.551 BSC	
L	0.73	1.03		0.029	0.041
e	0.80 BSC			0.031 BSC	
b	0.30	0.45		0.012	0.018
c	0.11	0.23		0.004	0.009
	Pin features				
N	80				
ND	24				
NE	16				
NOTE	RECTANGULAR				

Conforms to JEDEC MO-112 CB-1 Iss. B

This body outline must be used where referenced on existing build sheet.
However, this outline will not be approved.
The corresponding body +3.2mm outline GPD00306 is the approved alternative.

Notes:
1. Pin 1 indicator may be a corner chamfer, dot or both.
2. Controlling dimensions are in millimeters.
3. The top package body size may be smaller than the bottom package body size by a max. of 0.15 mm.
4. Dimension D1 and E1 do not include mould protusion.
5. Dimension b does not include dambar protusion.
6. Coplanarity, measured at seating plane G, to be 0.10 mm max.

This drawing supersedes 418/ED/51210/004 (Swindon)

ORIGINATING SITE: SWINDON

ISSUE	1	2	3	4	
ACN	201355	203202	204758	207068	
DATE	28OCT96	20OCT97	23JUN98	2JUL99	
APPROVED					

MITEL SEMICONDUCTOR

Title: Package Outline Drawing for 80L MQFP (GP) (14x20x2.8) mm, Body+3.9 mm

Drawing Number

GPD00240

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