STANDARD MICROSYSTEMS CORPORATION

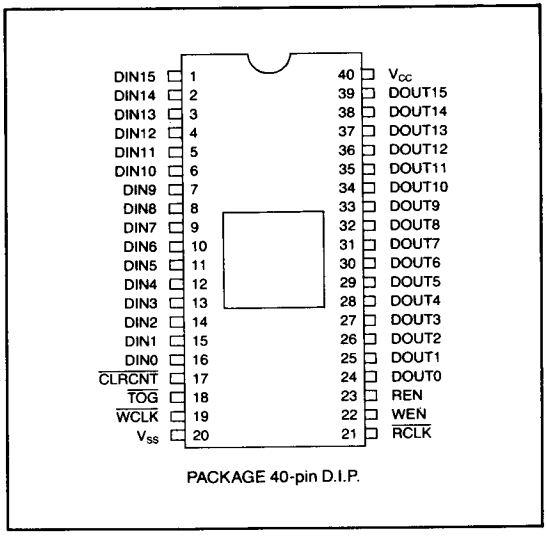
CRT 94C12
PRELIMINARY

Quad Row Buffer QRB

FEATURES

- ☐ Low Cost Solution to CRT Memory Contention Problem
- ☐ Provides Enhanced Processor Throughput for CRT Display Systems
- ☐ Replaces Shift Registers or Several RAM and Counter IC's in CRT Display System
- ☐ Permits Display of One Data Row While Next Data Row is Being Loaded
- ☐ Data May be Written into Buffer at Less Than the Video Painting Rate
- ☐ Row Buffer Architecture Permits Second Data Row to be Loaded Anytime during the Display of the Preceding Data Row
- ☐ Permits Active Video on All Scan Lines of Data Row
- ☐ Dynamically Variable Number of Characters per Data Row—...64, 80, 132,...up to a Maximum of 135
- ☐ Stackable for "Invisible Attributes" or Character Widths of Greater than 8 Bits
- ☐ Supports Both Double Row Buffer and Attribute Assemble Modes of the CRT 9007
- ☐ Three-State Outputs
- ☐ Up to 4 MHz Read/Write Data Rate
- ☐ Compatible with SMC CRT 9007
- ☐ 40 Pin Dual-In-Line Package
- ☐ Low Power CMOS Technology
- ☐ +5 Volt Only Power Supply
- ☐ TTL Compatible

PIN CONFIGURATION



PACKAGE 40-pin D.I.P.

GENERAL DESCRIPTION

The CRT 94C12 Quad Row Buffer (QRB) is a CMOS VLSI device which provides a low cost solution to memory contention between the system processor and the CRT controller in video display systems yet provides a maximum performance solution when combined with the CRT 9007 and the CRT 9041 VPAC family components.

The CRT 94C12 QRB is a RAM-based buffer which provides four rows of buffering. It appears to the system as two pairs of octal shift registers of dynamically variable length (2-135 bytes) plus steering logic.

The CRT 94C12 can support both the double row buffer and the attribute assemble operation modes of the CRT 9007. These operation modes permit the loading of one data row while the previous data row is being displayed. The loading of data may take place during any of the scan line times of the data row. This relaxed time-constraint allows the processor to perform additional processing on the data or service other high priority interrupt conditions which may occur during a single video scan line. The result is enhanced processor throughput and flicker-free display of data. In addition the attribute assemble mode allows an 8-bit data bus to be used when implementing parallel attributes.

SECTION V

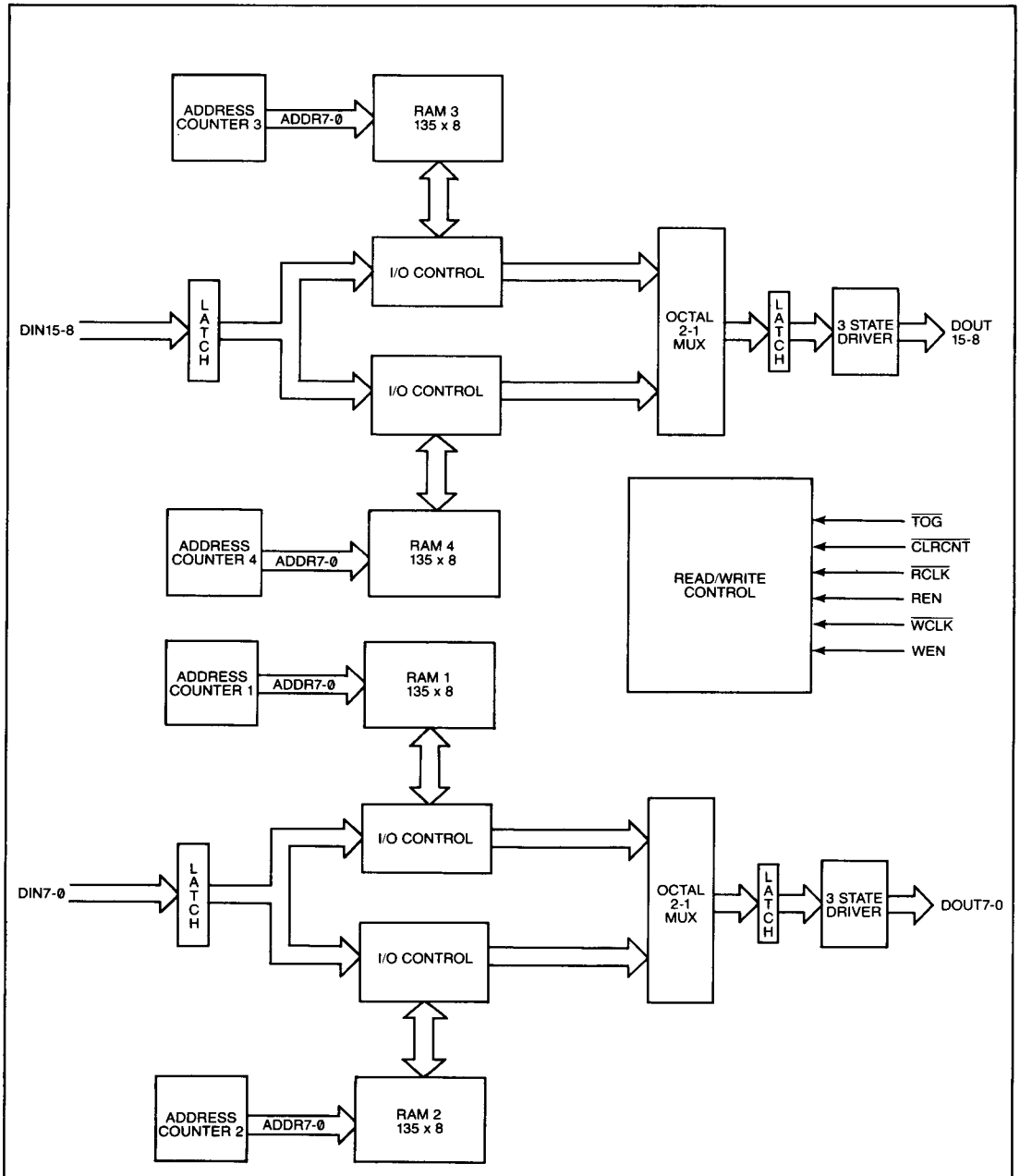


FIGURE 1: CRT 94C12 QUAD ROW BUFFER BLOCK DIAGRAM

DESCRIPTION OF PIN FUNCTIONS

PIN NO.	NAME	SYMBOL	FUNCTION
1-16	Data inputs	DIN15-DIN0	DIN15-DIN0 are the data inputs from the system memory.
24-39	Data outputs	DOUT15-DOUT0	DOUT15-DOUT0 are the data outputs from the CRT 94C12 internal data output latch. Valid information will appear on DOUT0-DOUT15 two $\overline{\text{RCLK}}$ periods after the rising edge of REN. This introduces two pipeline delays when supplying data to the character generator.
21	$\overline{\text{Read Clock}}$	$\overline{\text{RCLK}}$	$\overline{\text{RCLK}}$ increments the current "read" address register, clocks data through the "read" buffer and moves data through the internal pipeline at the trailing edge.
18	$\overline{\text{Toggle Signal}}$	$\overline{\text{TOG}}$	$\overline{\text{TOG}}$ alternates the function of each buffer between read and write. $\overline{\text{TOG}}$ normally occurs at every data row boundary. Switching of the buffers occurs when both $\overline{\text{TOG}}$ and $\overline{\text{CLRCNT}}$ are low.
17	$\overline{\text{Clear Counter}}$	$\overline{\text{CLRCNT}}$	$\overline{\text{Clear Counter}}$ clears the current "read" address counter at the next $\overline{\text{RCLK}}$ positive edge. $\overline{\text{CLRCNT}}$ is normally asserted low at the beginning of each horizontal retrace interval. $\overline{\text{CLRCNT}}$ clears the current "write" address counter when the $\overline{\text{TOG}}$ is active.
23	Read Enable	REN	REN enables the loading of data from the selected "read" buffer into the output latch. Data is loaded when $\overline{\text{Read Clock}}$ is active.
22	Write Enable	WEN	WEN allows input data to be written into the selected "write" buffer during $\overline{\text{WCLK}}$ active. WEN has an internal pullup resistor allowing it to assume a high if pin 22 is left open.
19	$\overline{\text{Write Clock}}$	$\overline{\text{WCLK}}$	$\overline{\text{WCLK}}$ clocks input data into the selected "write" buffer and increments the current "write" address register when WEN is high.
40	Power Supply	V_{CC}	+ 5 Volt supply
20	Ground	GND	Ground

OPERATION

Figure 1 illustrates the internal architecture of the CRT 94C12. It contains 135 bytes of RAM in each of its four buffers. In normal operation, data is written into the input latch on the positive-going edge of Write Clock ($\overline{\text{WCLK}}$). When Write Enable (WEN) goes high, the next $\overline{\text{WCLK}}$ causes data from the input latch to be written into the selected buffer (1 or 2) and the associated address counter to be incremented by one. Loading of the selected RAM buffer continues until WEN goes inactive or until the buffer has been fully loaded. At the next data row boundary, the Toggle Signal ($\overline{\text{TOG}}$) will go low. When Clear Counter ($\overline{\text{CLRCNT}}$) goes low, the next Read Clock ($\overline{\text{RCLK}}$) will begin to reset both buffer address counters to zero, switching the buffer just loaded from a "write buffer" to a "read buffer", permitting the next row of data to be written into the other buffer. Data from the current "read" buffer is read out of the buffer and to the output latch whenever Read Enable (REN) is high during a Read Clock ($\overline{\text{RCLK}}$). Each read-out from the buffer RAM causes the "read" address counter to be incremented. REN is normally high during the entire visible line time of each scan line of the data row. $\overline{\text{CLRCNT}}$ resets the present "read" address counter. The negative edge of $\overline{\text{CLRCNT}}$ is detected by the CRT 94C12 and internal "read" address counter.

Figures 2 and 3 illustrate the functional timing for reading from and writing to the CRT 94C12. The CRT 94C12 is compatible with the VPAC family of devices (CRT 9007, CRT 8002, CRT 9021 and the CRT 9041) and provides up to sixteen bits per character of row buffering with a single device. The sixteen bits can be divided between character data and attributes as required allowing the support of character-by-character, or invisible, attributes. This capability can be implemented using a 16-bit data bus with the double row buffer operation mode of the CRT 9007 or an 8-bit data bus using the attribute assemble operation mode. Typical configurations employing the VPAC family of parts are illustrated in Figures 5 and 6.

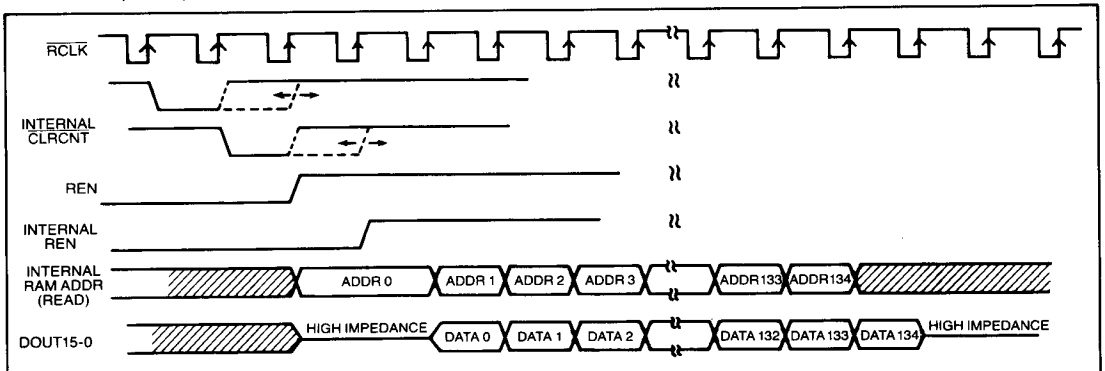


FIGURE 2: CRT 94C12 QUAD ROW BUFFER READ TIMING

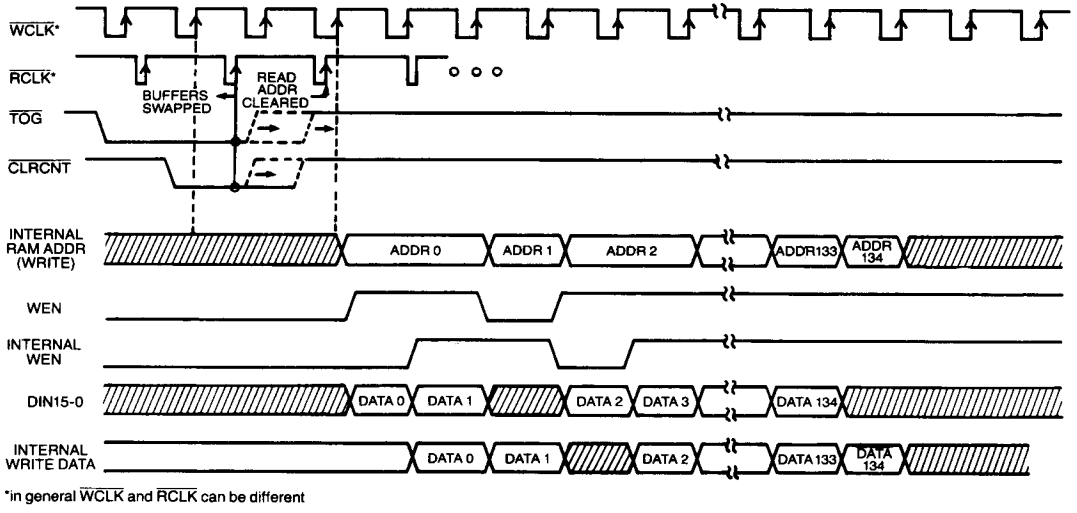


FIGURE 3: CRT 94C12 QUAD ROW BUFFER WRITE TIMING

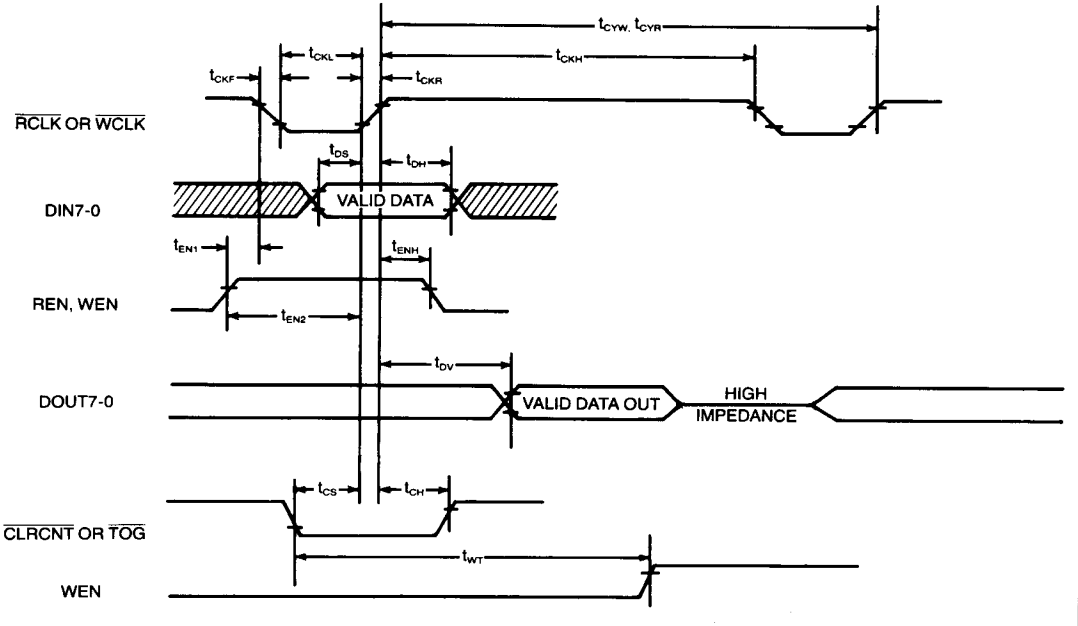


FIGURE 4: CRT 94C12 I/O TIMING

MAXIMUM GUARANTEED RATINGS

Operating Temperature Range ..... 0° to 70°C
Storage Temperature Range ..... −55°C to +150°C
Lead Temperature (soldering, 10 sec) ..... +325°C
Maximum V_{CC} ..... +7.0 V
Positive Voltage on any Pin, with respect to Ground ..... V_{CC} + 0.3 V
Negative Voltage on any Pin, with respect to Ground ..... −0.5 V

*Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied.

ELECTRICAL CHARACTERISTICS (T_A = 0°C to 70°C, V_{CC} = +5V ±5%)

PARAMETER	MIN	TYP	MAX	UNITS	COMMENTS
DC CHARACTERISTICS					
INPUT VOLTAGE LEVELS					
Low Level V_{IL}			0.8	V	
High Level V_{IH1}	2.0			V	excluding $\overline{RCLK}$; $\overline{WCLK}$
High Level V_{IH2}	4.2			V	$\overline{RCLK}$, $\overline{WCLK}$
OUTPUT VOLTAGE LEVELS					
Low Level V_{OL}			0.4	V	I_{OL} = 2mA
High Level V_{OH}	2.4			V	I_{OH} = 100 µA
INPUT LEAKAGE CURRENT					
High Leakage I_{LH1}			10	µA	excluding $\overline{OE}$
Low Leakage I_{LL1}			10	µA	excluding WEN1
High Leakage I_{LH2}			400	µA	WEN1
Low Leakage I_{LL2}			400	µA	$\overline{OE}$
INPUT CAPACITANCE					
C_{IN1}		10		pF	excluding $\overline{RCLK}$, $\overline{WCLK}$
C_{IN2}		15		pF	$\overline{RCLK}$, $\overline{WCLK}$
POWER SUPPLY CURRENT					
I_{CC}			40	mA	

PARAMETER	MIN	TYP	MAX	UNITS	COMMENTS
AC CHARACTERISTICS[1]					
t_{CYW}	250			ns	Write clock period
t_{CYR}	250			ns	Read clock period
t_{CKH}	100		DC	ns	
t_{CKL}	100			ns	
t_{CKR}			10	ns	measured from 10% to 90% points
t_{CKF}			10	ns	measured from 90% to 10% points
t_{DS}	50			ns	referenced to $\overline{WCLK}$
t_{DH}	0			ns	referenced to $\overline{WCLK}$
t_{EN1}[2]	0			ns	
t_{EN2}[2]	100			ns	
t_{ENH}[2]	0			ns	
t_{DV}			175	ns	C_L = 50 pF; referenced from $\overline{RCLK}$
t_{CS}	100			ns	
t_{CH}	0			ns	
t_{WT}[3]		$1t_{CYW}$			

1 - Reference points for all AC parameters are 2.4V high and 0.4V low.
2 - For REN, referenced from $\overline{RCLK}$; for WEN1 or WEN2 referenced to $\overline{WCLK}$.
3 - At least 1 WCLK rising edge must occur between $\overline{CLRCNT}$ or $\overline{TOG}$ (whichever occurs last) and WEN (= WEN1-WEN2).

SECTION V

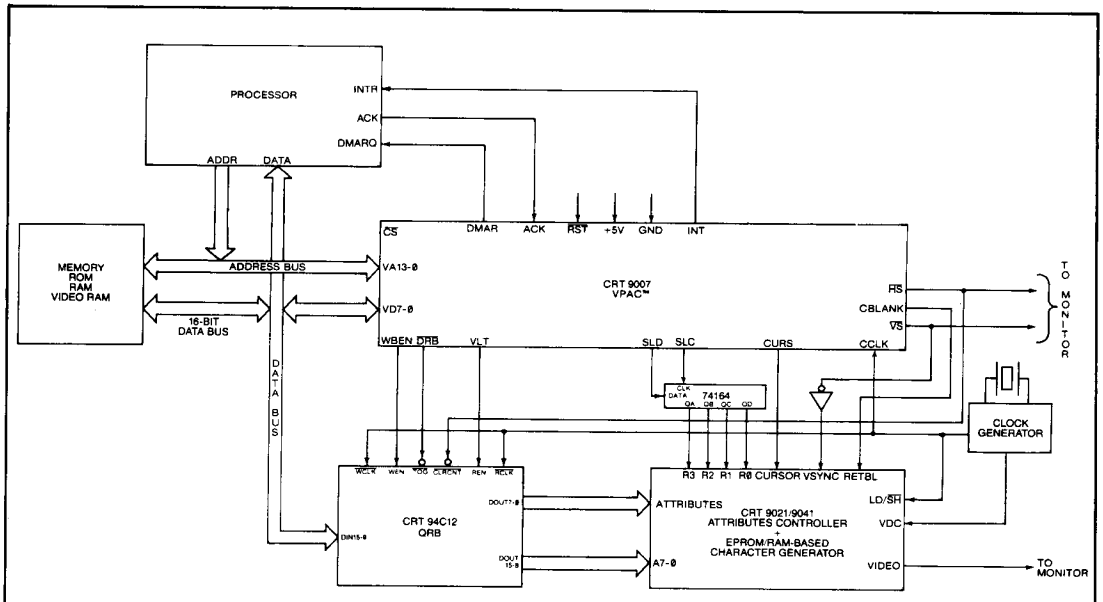


Figure 5. VPAC Configuration With Quad Row Buffer

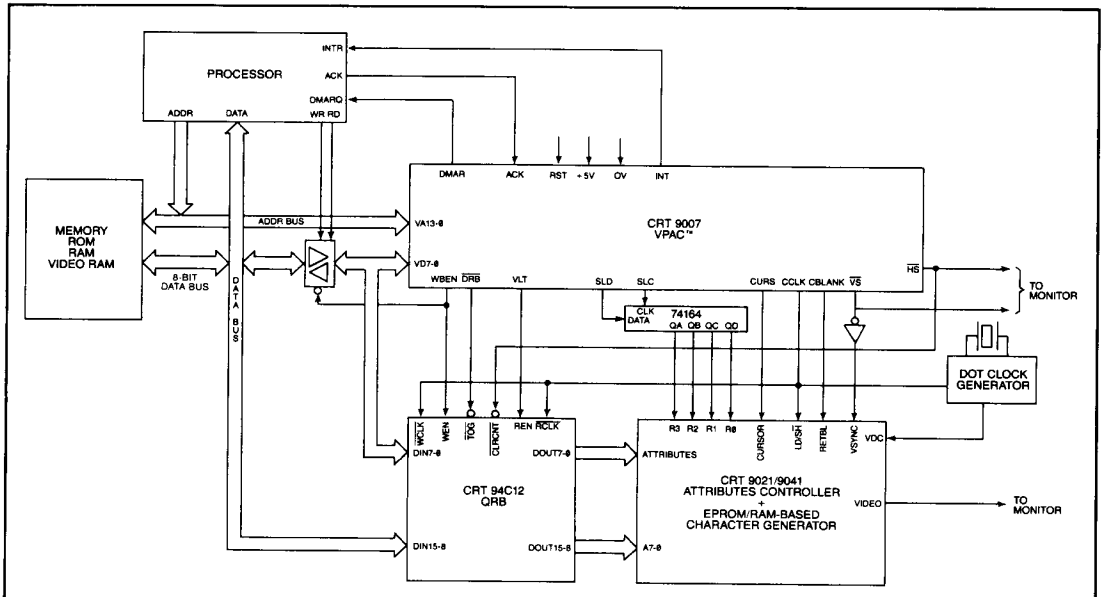


Figure 6. VPAC Configuration With Quad Row Buffer For Attribute Assembly