BCD UP/DOWN COUNTER

The HEF4510B is an edge-triggered synchronous up/down BCD counter with a clock input (CP), an up/down count control input (UP/$\overline{DN}$), an active LOW count enable input ($\overline{CE}$), an asynchronous active HIGH parallel load input (PL), four parallel inputs (P_0 to P_3), four parallel outputs (O_0 to O_3), an active LOW terminal count output ($\overline{TC}$), and an overriding asynchronous master reset input (MR).

Information on P_0 to P_3 is loaded into the counter while PL is HIGH, independent of all other input conditions except the MR input, which must be LOW. With PL LOW, the counter changes on the LOW to HIGH transition of CP if $\overline{CE}$ is LOW. UP/$\overline{DN}$ determines the direction of the count, HIGH for counting up, LOW for counting down. When counting up, $\overline{TC}$ is LOW when O_0 and O_3 are HIGH and $\overline{CE}$ is LOW. When counting down, $\overline{TC}$ is LOW when O_0 to O_3 and $\overline{CE}$ are LOW. A HIGH on MR resets the counter (O_0 to O_3 = LOW) independent of all other input conditions.

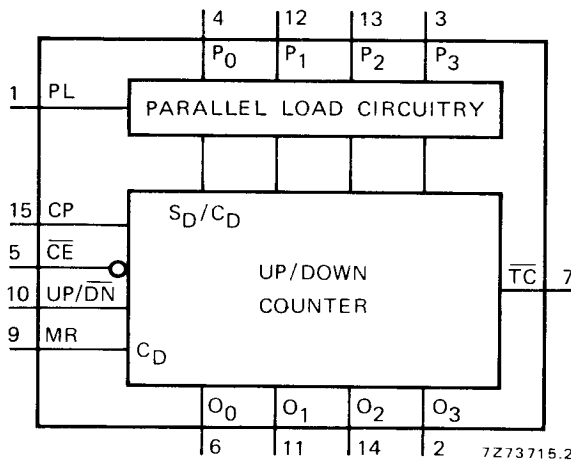
Fig. 1 Functional diagram.

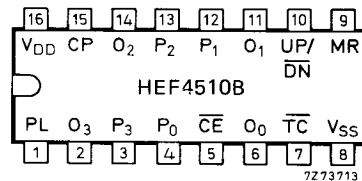
Fig. 2 Pinning diagram.

HEF4510BP : 16-lead DIL; plastic (SOT-38Z).
HEF4510BD: 16-lead DIL; ceramic (cerdip) (SOT-74).
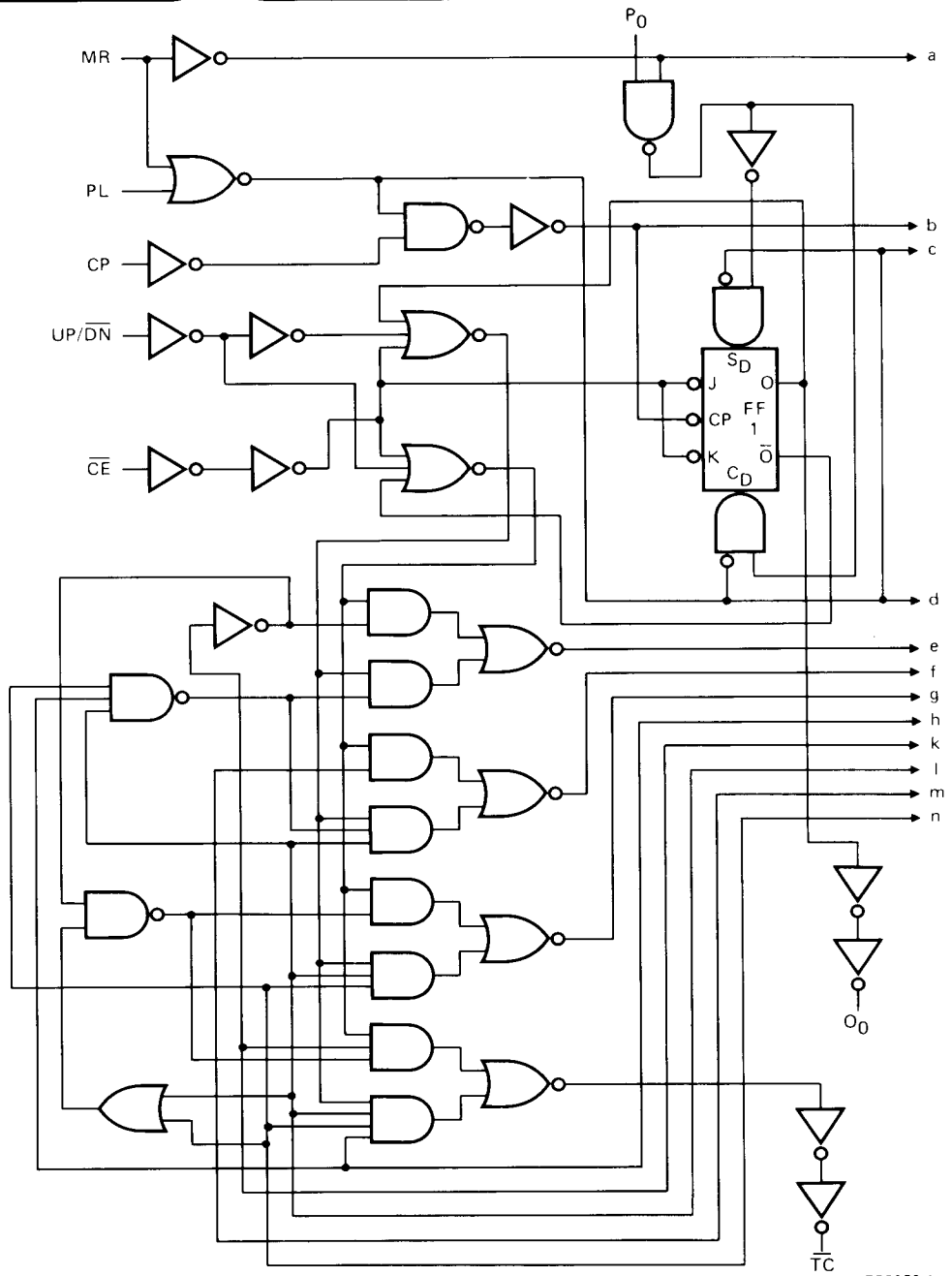HEF4510BT : 16-lead mini-pack; plastic (SO-16; SOT-109A).

PINNING

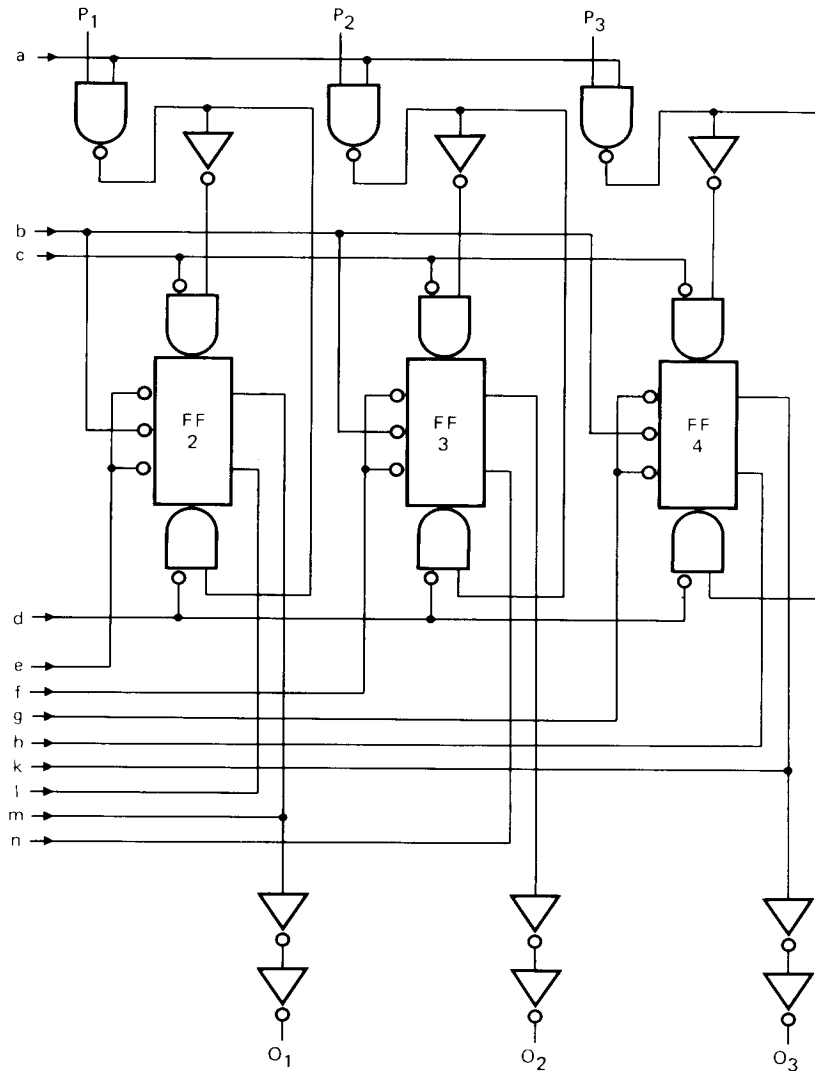|			
PL	parallel load input (active HIGH)	UP/$\overline{DN}$	up/down count control input
P_0 to P_3	parallel inputs	MR	master reset input
$\overline{CE}$	count enable input (active LOW)	$\overline{TC}$	terminal count output (active LOW)
CP	clock pulse input (LOW to HIGH, edge triggered)	O_0 to O_3	parallel outputs

FAMILY DATA

see Family Specifications

I_{DD} LIMITS category MSI

Fig. 3a Logic diagram (continued in Fig. 3b).

7Z75079.1

7Z75080.1

Fig. 3b Logic diagram (continued from Fig. 3a).

FUNCTION TABLE

MR	PL	UP/$\overline{\text{DN}}$	$\overline{\text{CE}}$	CP	mode
L	H	X	X	X	parallel load
L	L	X	H	X	no change
L	L	L	L	$\int$	count down
L	L	H	L	$\int$	count up
H	X	X	X	X	reset

H = HIGH state (the more positive voltage)
L = LOW state (the less positive voltage)
X = state is immaterial
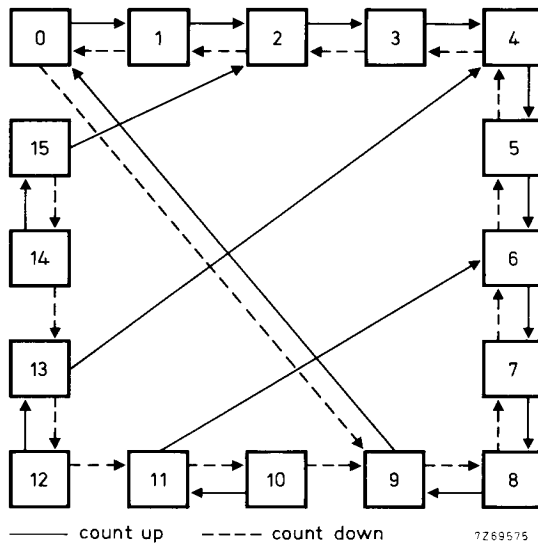$\int$ = positive-going transition

count up ————   count down - - - -   7Z69575

Fig. 4 State diagram.

Logic equation for terminal count:

$$\overline{TC} = \overline{\overline{\overline{CE}} \cdot \left\{ (UP/\overline{DN}) \cdot O_0 \cdot O_3 + \overline{(UP/\overline{DN})} \cdot \overline{O}_0 \cdot \overline{O}_1 \cdot \overline{O}_2 \cdot \overline{O}_3 \right\}}$$

A.C. CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = 25 $^{\circ}$C; input transition times $\leqslant$ 20 ns

	V_{DD} V	typical formula for P (μW)	where f_i = input freq. (MHz) f_o = output freq. (MHz) C_L = load capacitance (pF) $\Sigma(f_oC_L)$ = sum of outputs V_{DD} = supply voltage (V)
Dynamic power dissipation per package (P)	5	$1000 \, f_i + \Sigma(f_oC_L) \times V_{DD}^2$	
	10	$4500 \, f_i + \Sigma(f_oC_L) \times V_{DD}^2$	
	15	$11\,200 \, f_i + \Sigma(f_oC_L) \times V_{DD}^2$	

A.C. CHARACTERISTICS

$V_{SS} = 0$ V; $T_{amb} = 25$ °C; $C_L = 50$ pF; input transition times $\leqslant 20$ ns

	V_{DD} V	symbol	min.	typ.	max.		typical extrapolation formula
Propagation delays							
CP ⟶ O_n	5			145	290	ns	118 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}		60	120	ns	49 ns + (0,23 ns/pF) C_L
	15			45	90	ns	37 ns + (0,16 ns/pF) C_L
	5			155	310	ns	128 ns + (0,55 ns/pF) C_L
LOW to HIGH	10	t_{PLH}		65	130	ns	54 ns + (0,23 ns/pF) C_L
	15			45	90	ns	37 ns + (0,16 ns/pF) C_L
CP ⟶ $\overline{TC}$	5			260	525	ns	233 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}		105	210	ns	94 ns + (0,23 ns/pF) C_L
	15			75	150	ns	67 ns + (0,16 ns/pF) C_L
	5			180	360	ns	153 ns + (0,55 ns/pF) C_L
LOW to HIGH	10	t_{PLH}		75	150	ns	64 ns + (0,23 ns/pF) C_L
	15			55	115	ns	47 ns + (0,16 ns/pF) C_L
PL ⟶ O_n	5			125	255	ns	98 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}		55	110	ns	44 ns + (0,23 ns/pF) C_L
	15			40	85	ns	32 ns + (0,16 ns/pF) C_L
	5			170	340	ns	143 ns + (0,55 ns/pF) C_L
LOW to HIGH	10	t_{PLH}		70	140	ns	59 ns + (0,23 ns/pF) C_L
	15			50	105	ns	42 ns + (0,16 ns/pF) C_L
PL ⟶ $\overline{TC}$	5			250	500	ns	223 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}		110	220	ns	99 ns + (0,23 ns/pF) C_L
	15			80	160	ns	72 ns + (0,16 ns/pF) C_L
	5			250	500	ns	223 ns + (0,55 ns/pF) C_L
LOW to HIGH	10	t_{PLH}		110	220	ns	99 ns + (0,23 ns/pF) C_L
	15			80	160	ns	72 ns + (0,16 ns/pF) C_L
$\overline{CE}$ ⟶ $\overline{TC}$	5			165	330	ns	138 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}		65	135	ns	54 ns + (0,23 ns/pF) C_L
	15			50	100	ns	42 ns + (0,16 ns/pF) C_L
	5			145	290	ns	118 ns + (0,55 ns/pF) C_L
LOW to HIGH	10	t_{PLH}		60	125	ns	49 ns + (0,23 ns/pF) C_L
	15			45	95	ns	37 ns + (0,16 ns/pF) C_L
MR ⟶ O_n, $\overline{TC}$	5			205	405	ns	178 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}		65	130	ns	54 ns + (0,23 ns/pF) C_L
	15			45	85	ns	37 ns + (0,16 ns/pF) C_L
MR ⟶ $\overline{TC}$	5			225	450	ns	198 ns + (0,55 ns/pF) C_L
LOW to HIGH	10	t_{PLH}		75	150	ns	64 ns + (0,23 ns/pF) C_L
	15			50	100	ns	42 ns + (0,16 ns/pF) C_L

A.C. CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = 25 °C; C_L = 50 pF; input transition times ⩽ 20 ns

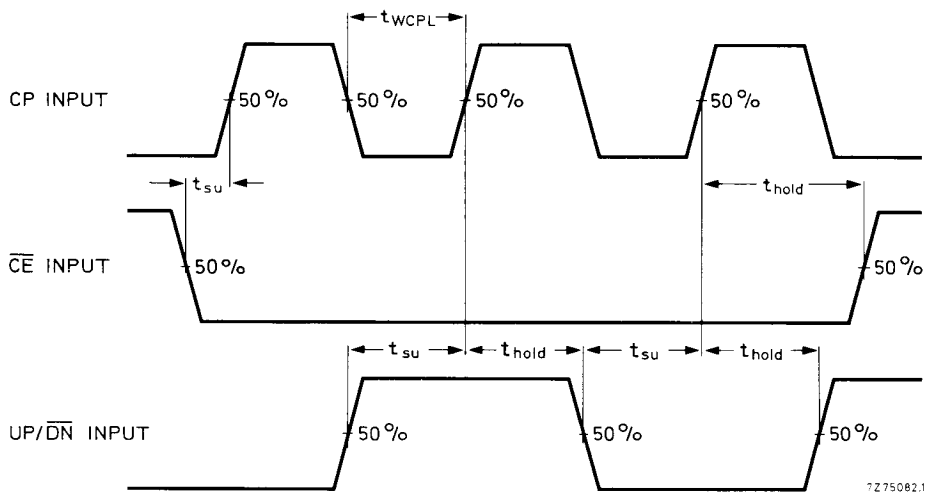|	V_{DD} V	symbol	min.	typ.	max.		typical extrapolation formula
Output transition times	5			60	120	ns	10 ns + (1,0 ns/pF) C_L
HIGH to LOW	10	t_{THL}		30	60	ns	9 ns + (0,42 ns/pF) C_L
	15			20	40	ns	6 ns + (0,28 ns/pF) C_L
	5			60	120	ns	10 ns + (1,0 ns/pF) C_L
LOW to HIGH	10	t_{TLH}		30	60	ns	9 ns + (0,42 ns/pF) C_L
	15			20	40	ns	6 ns + (0,28 ns/pF) C_L
Minimum clock	5		95	45		ns	
pulse width; LOW	10	t_{WCPL}	35	20		ns	
	15		25	15		ns	
Minimum PL	5		105	55		ns	
pulse width; HIGH	10	t_{WPLH}	45	25		ns	
	15		35	15		ns	
Minimum MR	5		120	60		ns	
pulse width; HIGH	10	t_{WMRH}	50	25		ns	
	15		40	20		ns	
Recovery time	5		130	65		ns	
for MR	10	t_{RMR}	45	20		ns	
	15		30	15		ns	
Recovery time	5		150	75		ns	
for PL	10	t_{RPL}	50	25		ns	
	15		30	15		ns	
Set-up times	5		100	50		ns	
$P_n \longrightarrow$ PL	10	t_{su}	50	25		ns	
	15		40	20		ns	see also waveforms Figs 5 and 6
	5		250	125		ns	
UP/$\overline{DN} \longrightarrow$ CP	10	t_{su}	100	50		ns	
	15		75	35		ns	
	5		120	60		ns	
$\overline{CE} \longrightarrow$ PL	10	t_{su}	40	20		ns	
	15		25	10		ns	
Hold times	5		10	−40		ns	
$P_n \longrightarrow$ PL	10	t_{hold}	5	−20		ns	
	15		0	−20		ns	
	5		35	−90		ns	
UP/$\overline{DN} \longrightarrow$ CP	10	t_{hold}	15	−35		ns	
	15		15	−25		ns	
	5		20	−40		ns	
$\overline{CE} \longrightarrow$ CP	10	t_{hold}	5	−15		ns	
	15		5	−10		ns	
Maximum clock	5		5	10		MHz	
pulse frequency	10	f_{max}	12	24		MHz	
	15		17	34		MHz	

Fig. 5 Waveforms showing minimum pulse width for CP, set-up and hold times for $\overline{CE}$ to CP and UP/$\overline{DN}$ to CP.
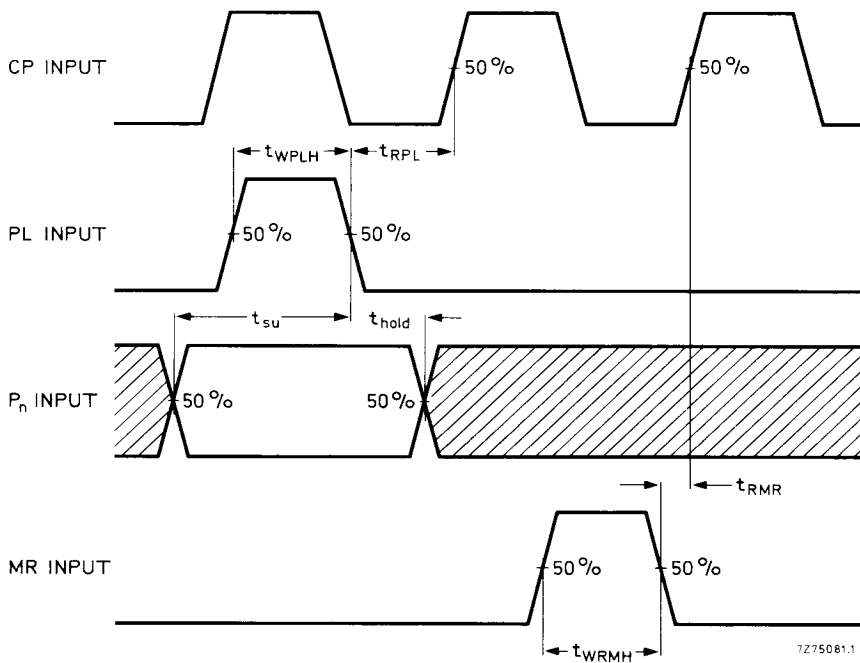

Fig. 6 Waveforms showing minimum pulse width for PL and MR, recovery time for PL and MR and set-up and hold times for P_n to PL.
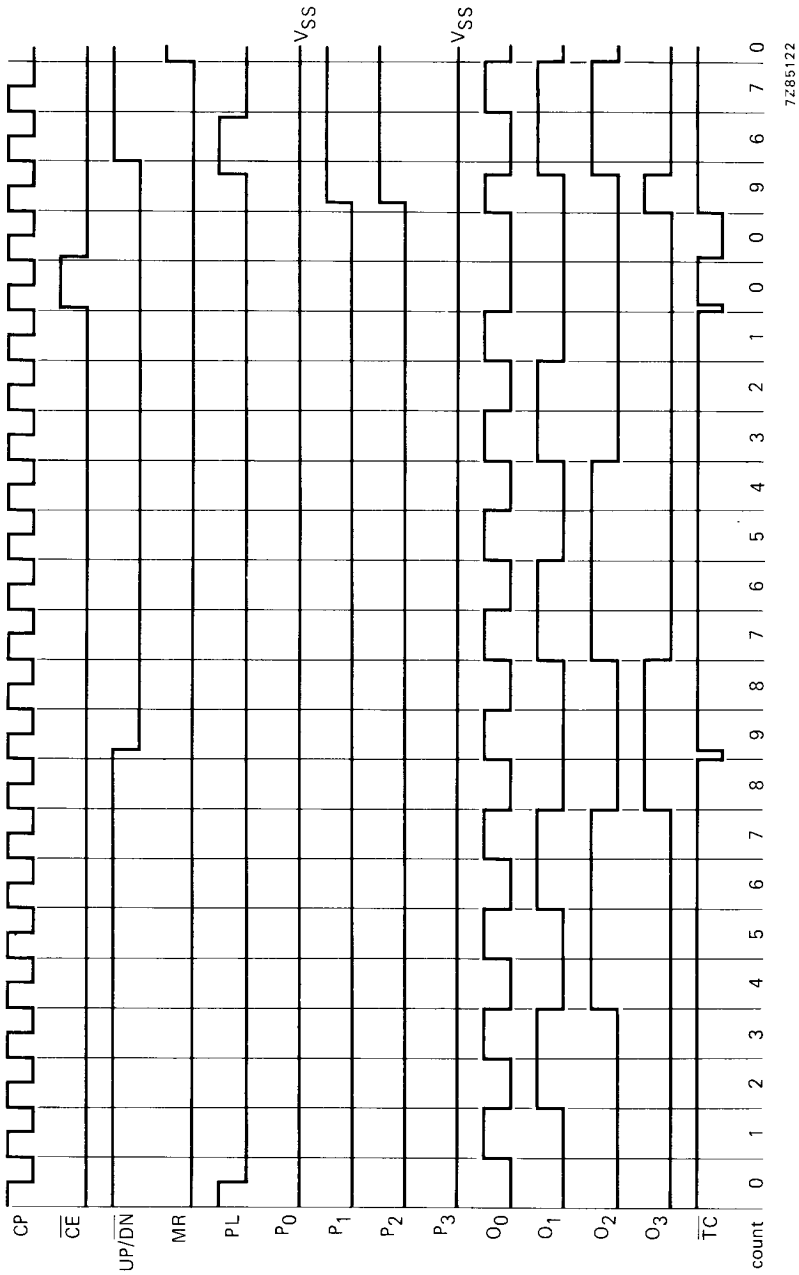
Fig. 7 Timing diagram.