Enhanced A/D Flash Type 8-Bit MCU with EEPROM and UART Interface

HT66FU60A/HT66FU70A

Revision: V1.00 Date: November 29, 2012

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Features

CPU Features

- Operating Voltage:
  - f_{SYS}=8MHz: 2.2V~5.5V
  - f_{SYS}=12MHz: 2.7V~5.5V
  - f_{SYS}=16MHz: 4.5V~5.5V
- Up to 0.25μs instruction cycle with 16MHz system clock at V_{DD}=5V
- Power down and wake-up functions to reduce power consumption
- Five oscillators
  - External Crystal − HXT
  - External 32.768kHz − LXT
  - External RC − ERC
  - Internal RC − HIRC
  - Internal 32kHz RC − LIRC
- Multi-mode operation: NORMAL, SLOW, IDLE and SLEEP
- Fully integrated internal 8MHz oscillator requires no external components
- All instructions executed in one or two instruction cycles
- Table read instructions
- 63 powerful instructions
- Up to 16-level subroutine nesting
- Bit manipulation instruction

Peripheral Features

- Flash Program Memory: 16K×16 ~ 32K×16
- Data Memory: 1024×8 ~ 2048×8
- EEPROM Memory: 128×8
- In Application Programming function
- Watchdog Timer function
- Up to 53 bidirectional I/O lines
- Software controlled 4-SCOM lines LCD driver with 1/2 bias
- Multiple pin-shared external interrupts
- Multiple Timer Module for time measure, input capture, compare match output, PWM output or single pulse output function
- Serial Interfaces Module – SIM for SPI or I^2C
- Single sefial SPI interface – SPIA
- Dual Comparator functions
- Dual Time-Base functions for generation of fixed time interrupt signals
- Multi-channel 12-bit resolution A.D converter
- Low voltage reset function
- Low voltage detect function
- Wide range of available package types
- Flash program memory can be re-programmed up to 100,000 times
- Flash program memory data retention > 10 years
- EEPROM data memory can be re-programmed up to 1,000,000 times
- EEPROM data memory data retention > 10 years

UART Module Features

- Interconnected to Holtek MCU via SPI Interface
- Full-duplex, Universal Asynchronous Receiver and Transmitter (UART) communication
  - 8-bit or 9-bit character length
  - Even, Odd or No parity options
  - One or two stop bits
  - Baud rate generator with 8-bit prescaler
  - Parity, framing, noise and overrun error detection
  - Support for interrupt on address detect
  - Address Detect Interrupt – last character bit=1
  - Transmitter and Receiver ennabled independently
  - 4-byte deep FIFO receiver data buffer
  - Transmit and Receive Multiple Interrupt Generation Sources
    - Transmitter Empty
    - Transmitter Idle
    - Receiver Full
    - Receiver Overrun
    - Address Mode Detect
  - TX pin is high impedance when the UART transmit module is disabled
  - RX pin is high impedance when the UART Receive module is disabled
- CMOS clock input, CLKI, up to 20MHz at 5V operating voltage

General Description

The HT66FU60A/HT66FU70A series of devices are Flash Memory A/D type 8-bit high performance RISC architecture microcontrollers, designed for a wide range of applications. Offering users the convenience of Flash Memory multi-programming features, these devices also include a wide range of functions and features. Other memory includes an area of RAM Data Memory as well as an area of EEPROM memory for storage of non-volatile data such as serial numbers, calibration data etc.

Analog features include a multi-channel 12-bit A/D converter and dual comparator functions. Multiple and extremely flexible Timer Modules provide timing, pulse generation and PWM generation functions. Communication with the outside world is catered for by including fully integrated SPI or I^2C interface functions, two popular interfaces which provide designers with a means of easy communication with external peripheral hardware. Protective features such as an internal Watchdog Timer, Low Voltage Reset and Low Voltage Detector coupled with excellent noise immunity and ESD protection ensure that reliable operation is maintained in hostile electrical environments. A full choice of HXT, LXT, ERC, HIRC and LIRC oscillator functions are provided including a fully integrated system oscillator which requires no external components for its implementation. The ability to operate and switch dynamically between a range of operating modes using different clock sources gives users the ability to optimise microcontroller operation and minimise power consumption.

The UART module is contained in this series of devices. It can support the applications such as data communication networks between microcontrollers, low-cost data links between PCs and peripheral devices, portable and battery operated device communication, etc.

The inclusion of flexible I/O programming features, Time-Base functions along with many other features ensure that the devices will find excellent use in applications such as electronic metering, environmental monitoring, handheld instruments, household appliances, electronically controlled tools, motor driving in addition to many others.

Selection Table

Most features are common to all devices. The main features distinguishing them are Program Memory and Data Memory capacity. The following table summarises the main features of each device.

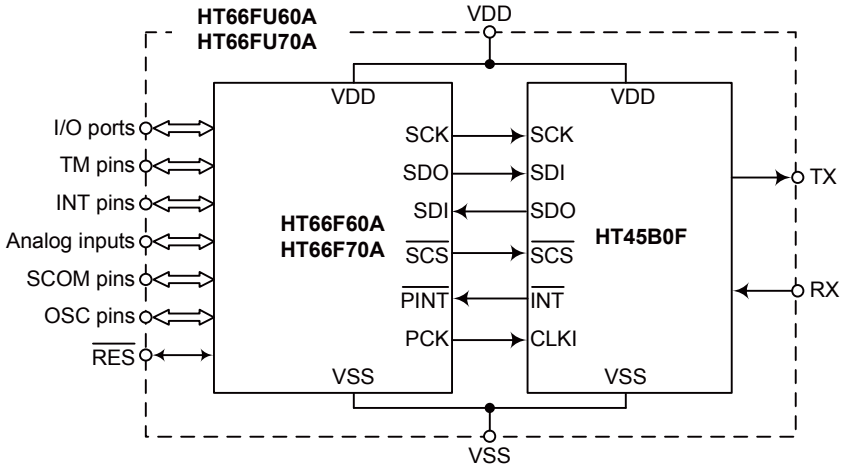
Part No.	Program Memory	Data Memory	Data EEPROM	I/O	External Interrupt	A/D Converter
HT66FU60A	16K × 16	1024 × 8	128 × 8	53	4	12-bit × 12
HT66FU70A	32K × 16	2048 × 8	128 × 8	53	4	12-bit × 12

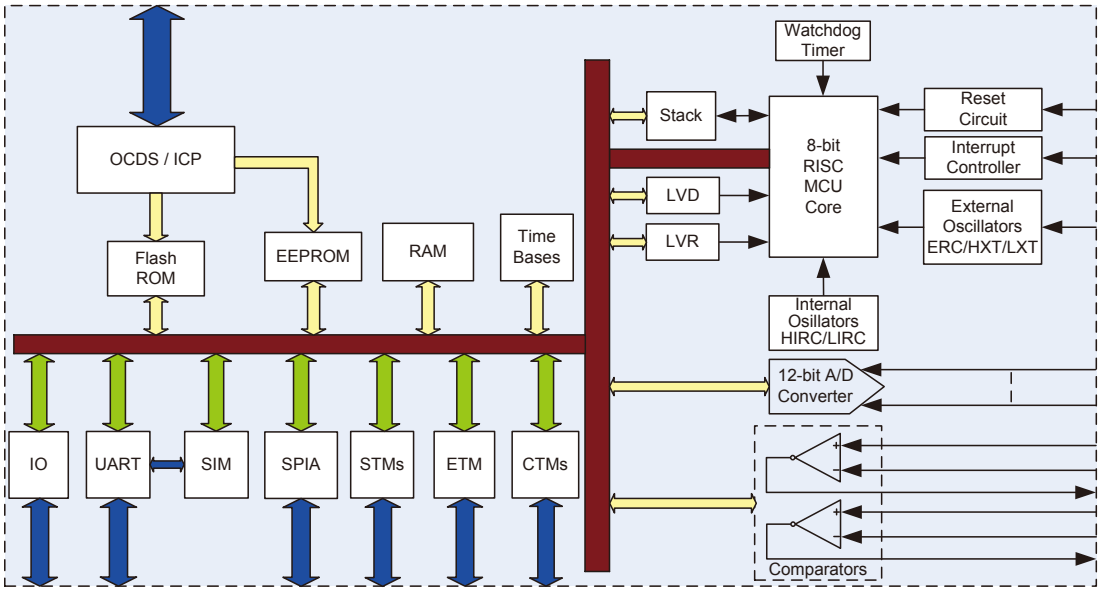
Part No.	Timer Module	SIM	SPIA	Time Base	Comparators	UART	Stacks	Package
HT66FU60A	10-bit CTM × 2 16-bit STM × 3 10-bit ETM × 1	√	√	2	2	√	16	48/64 LQFP
HT66FU70A	10-bit CTM × 2 16-bit STM × 3 10-bit ETM × 1	√	√	2	2	√	16	48/64 LQFP

Note: As devices exist in more than one package format, the table reflects the situation for the package with the most pins.

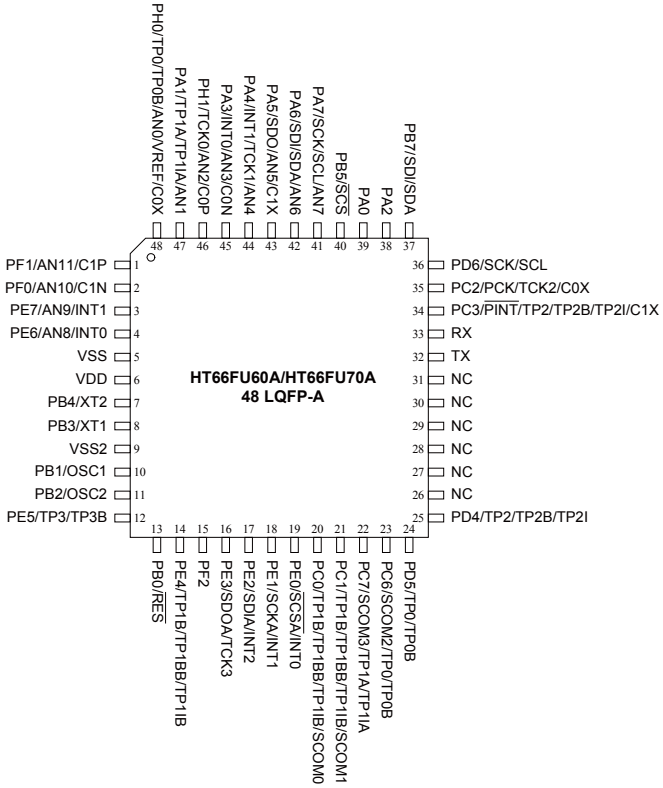
Block Diagram

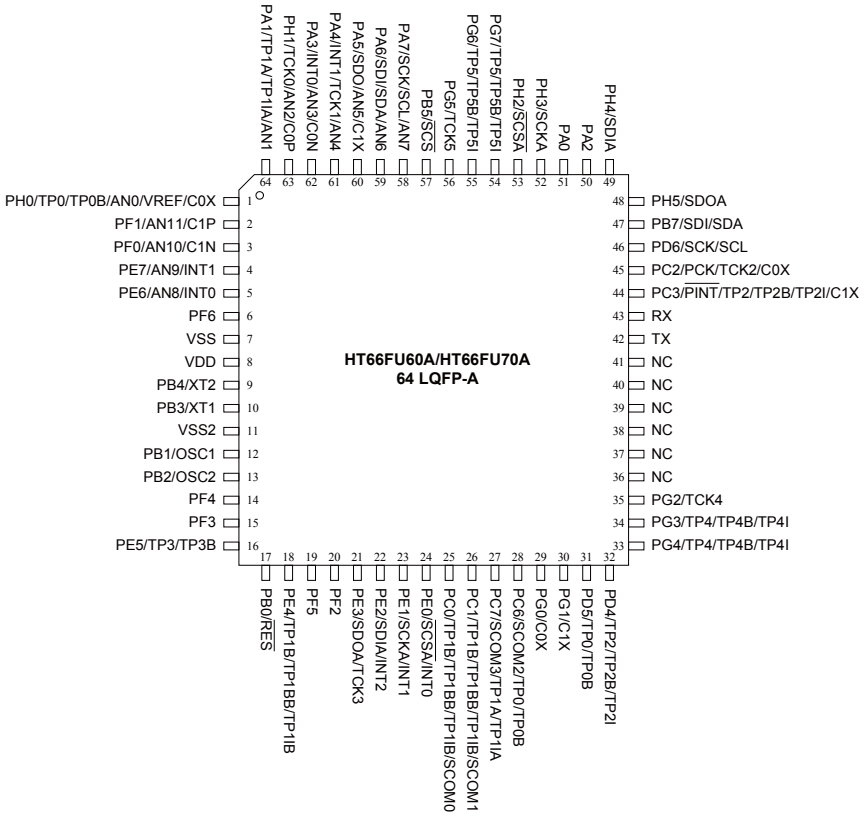
The following block diagram illustrates the dual-chip structure of the devices, where an individual MCU and SPI to UART chips are combined into a single package.

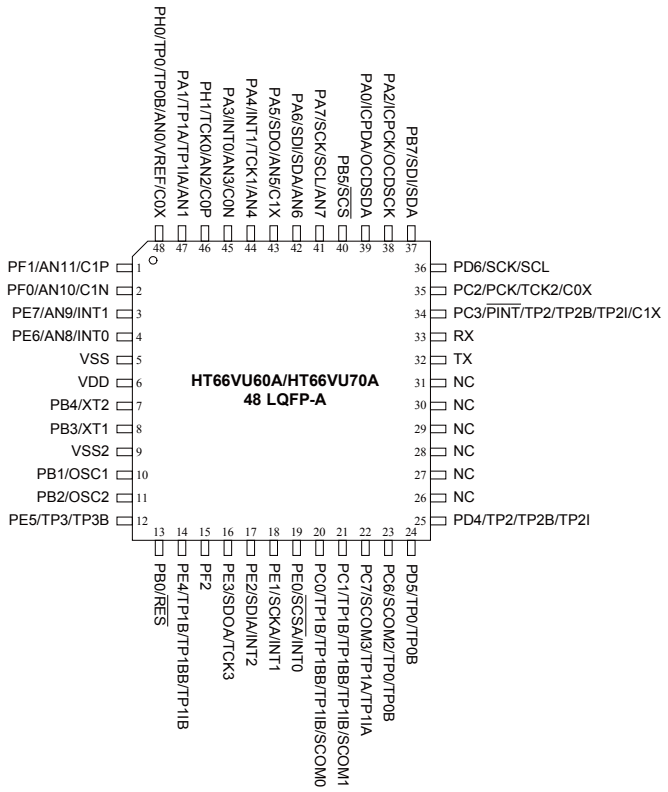


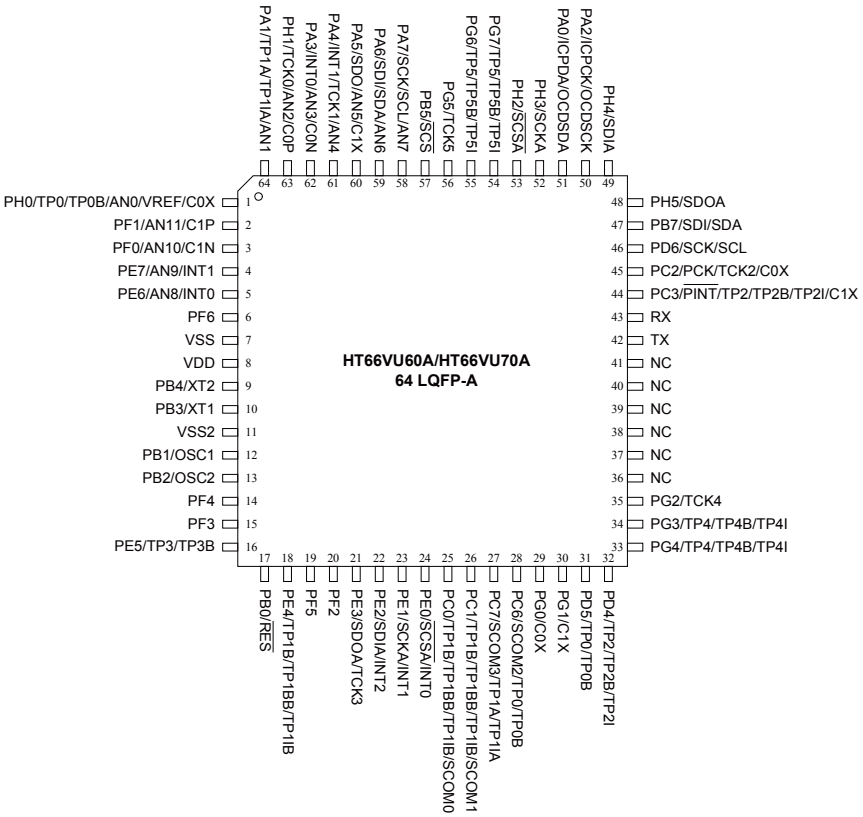


Pin Assignment




HT66FU60A/HT66FU70A
64 LQFP-A
PH0/TP0/TP0B/AN0/VREF/C0X
PF1/AN11/C1P
PF0/AN10/C1N
PE7/AN9/INT1
PE6/AN8/INT0
PF6
VSS
VDD
PB4/XT2
PB3/XT1
VSS2
PB1/OSC1
PB2/OSC2
PF4
PF3
PE5/TP3/TP3B
PA1/TP1A/TP1IA/AN1
PH1/TCK0/AN2/C0P
PA3/INT0/AN3/C0N
PA4/INT1/TCK1/AN4
PA5/SDO/AN5/C1X
PA6/SDI/SDA/AN6
PA7/SCK/SCL/AN7
PB5/SCS
PG5/TCK5
PG6/TP5/TP5B/TP5I
PG7/TP5/TP5B/TP5I
PH2/SCSA
PH3/SCKA
PA0
PA2
PH4/SDIA
PH5/SDOA
PB7/SDI/SDA
PD6/SCK/SCL
PC2/PCK/TCK2/C0X
PC3/PINT/TP2/TP2B/TP2I/C1X
RX
TX
NC
NC
NC
NC
NC
NC
PG2/TCK4
PG3/TP4/TP4B/TP4I
PG4/TP4/TP4B/TP4I
PB0/RES
PE4/TP1B/TP1BB/TP1IB
PF5
PF2
PE3/SDOA/TCK3
PE2/SDIA/INT2
PE1/SCKA/INT1
PE0/SCSA/INT0
PC0/TP1B/TP1BB/TP1IB/SCOM0
PC1/TP1B/TP1BB/TP1IB/SCOM1
PC7/SCOM3/TP1A/TP1IA
PC6/SCOM2/TP0/TP0B
PG0/C0X
PG1/C1X
PD5/TP0/TP0B
PD4/TP2/TP2B/TP2I


HT66VU60A/HT66VU70A
48 LQFP-A
PF1/AN11/C1P
PF0/AN10/C1N
PE7/AN9/INT1
PE6/AN8/INT0
VSS
VDD
PB4/XT2
PB3/XT1
VSS2
PB1/OSC1
PB2/OSC2
PE5/TP3/TP3B
PH0/TP0/TP0B/AN0/VREF/C0X
PA1/TP1A/TP1IA/AN1
PH1/TCK0/AN2/C0P
PA3/INT0/AN3/C0N
PA4/INT1/TCK1/AN4
PA5/SDO/AN5/C1X
PA6/SDI/SDA/AN6
PA7/SCK/SCL/AN7
PB5/SCS
PA0/ICPDA/OCDSDA
PA2/ICPCK/OCDSCK
PB7/SDI/SDA
PD6/SCK/SCL
PC2/PCK/TCK2/C0X
PC3/PINT/TP2/TP2B/TP2I/C1X
RX
TX
NC
NC
NC
NC
NC
NC
PD4/TP2/TP2B/TP2I
PB0/RES
PE4/TP1B/TP1BB/TP1IB
PF2
PE3/SDOA/TCK3
PE2/SDIA/INT2
PE1/SCKA/INT1
PE0/SCSA/INT0
PC0/TP1B/TP1BB/TP1IB/SCOM0
PC1/TP1B/TP1BB/TP1IB/SCOM1
PC7/SCOM3/TP1A/TP1IA
PC6/SCOM2/TP0/TP0B
PD5/TP0/TP0B



Note: 1. If the pin-shared pin functions have multiple outputs simultaneously, the pin-shared function is determined by the corresponding software control bits except the functions determined by the configuration options.

2. The HT66VU60A/HT66VU70A device is the EV chip of the HT66FU60A/HT66FU70A series of devices. It supports the "On-Chip Debug" function for debugging during development using the OCDSDA and OCDSCK pins connected to the Holtek HT-IDE development tools. Refer to the OCDS section of the MCU datasheet for more details.

Pin Description

With the exception of the power pins, all pins on these devices can be referenced by their Port name, e.g. PA.0, PA.1 etc, which refer to the digital I/O function of the pins. However these Port pins are also shared with other function such as the Analog to Digital Converter, Serial Port pins, etc. The function of each pin is listed in the following tables, however the details behind how each pin is configured is contained in individual MCU and SPI to UART chip datasheet. The important point to note here is that some I/O lines are not bonded to the external pins. Users should take special care of these I/O port lines. Refer to the Hardware Considerations section for more details.

Pad Name	Function	OPT	I/T	O/T	Description
PA0/ICPDA/OCDSDA	PA0	PAWU PAPU	ST	CMOS	General purpose I/O. Register enabled pull-up and wake-up.
	ICPDA	—	ST	CMOS	ICP Data/Address
	OCDSDA	—	ST	CMOS	OCDS Data/Address, for EV chip only.
PA1/TP1A/TP1IA/AN1	PA1	PAWU PAPU PAS0	ST	CMOS	General purpose I/O. Register enabled pull-up and wake-up.
	TP1A	PAS0	—	CMOS	TM1 A output
	TP1IA	IFS2	ST	—	TM1 A input
	AN1	PAS0	AN	—	A/D Converter analog input
PA2 /ICPCK/OCDSCK	PA2	PAWU PAPU	ST	CMOS	General purpose I/O. Register enabled pull-up and wake-up.
	ICPCK	—	ST	CMOS	ICP Clock pin
	OCDSCK	—	ST	—	OCDS Clock pin, for EV chip only.
PA3/INT0/AN3/C0N	PA3	PAWU PAPU PAS1	ST	CMOS	General purpose I/O. Register enabled pull-up and wake-up.
	INT0	INTEG INTC0 IFS0	ST	—	External Interrupt 0
	AN3	PAS1	AN	—	A/D Converter analog input
	C0N	PAS1	AN	—	Comparator 0 inverting input
PA4/INT1/TCK1/AN4	PA4	PAPU PAWU PAS2	ST	CMOS	General purpose I/O. Register enabled pull-up and wake-up.
	INT1	INTEG INTC0 IFS0	ST	—	External Interrupt 1
	TCK1	IFS1	ST	—	TM1 input
	AN4	PAS1	AN	—	A/D Converter analog input
PA5/SDO/AN5/C1X	PA5	PAWU PAPU PAS2	ST	CMOS	General purpose I/O. Register enabled pull-up and wake-up.
	SDO	PAS2	—	CMOS	SPI data output
	AN5	PAS2	AN	—	A/D Converter analog input
	C1X	PAS2	—	CMOS	Comparator 1 output

Pad Name	Function	OPT	I/T	O/T	Description
PA6/SDI/SDA/AN6	PA6	PAWU PAPU PAS3	ST	CMOS	General purpose I/O. Register enabled pull-up and wake-up.
	SDI	PAS3 IFS4	ST	—	SPI data input
	SDA	PAS3 IFS4	ST	NMOS	I^2C data line
	AN6	PAS3	AN	—	A/D Converter analog input
PA7/SCK/SCL/AN7	PA7	PAWU PAPU PAS3	ST	CMOS	General purpose I/O. Register enabled pull-up and wake-up.
	SCK	PAS3 IFS4	ST	CMOS	SPI serial clock
	SCL	PAS3 IFS4	ST	NMOS	I^2C clock line
	AN7	PAS3	AN	—	A/D Converter analog input
PB0/$\overline{RES}$	PB0	PBPU	ST	CMOS	General purpose I/O. Register enabled pull-up
	$\overline{RES}$	CO	ST	—	Reset pin
PB1/OSC1	PB1	PBPU	ST	CMOS	General purpose I/O. Register enabled pull-up
	OSC1	CO	HXT	—	HXT/ERC oscillator pin & EC mode input pin
PB2/OSC2	PB2	PBPU	ST	CMOS	General purpose I/O. Register enabled pull-up
	OSC2	CO	—	HXT	HXT oscillator pin
PB3/XT1	PB3	PBPU	ST	CMOS	General purpose I/O. Register enabled pull-up
	XT1	CO	LXT	—	LXT oscillator pin
PB4/XT2	PB4	PBPU	ST	CMOS	General purpose I/O. Register enabled pull-up
	XT2	CO	—	LXT	LXT oscillator pin
PB5/$\overline{SCS}$	PB5	PBPU PBS2	ST	CMOS	General purpose I/O. Register enabled pull-up
	$\overline{SCS}$	PBS2 IFS4	ST	CMOS	SPI slave select
PB7/SDI/SDA	PB7	PBPU PBS3	ST	CMOS	General purpose I/O. Register enabled pull-up and wake-up.
	SDI	PBS3 IFS4	ST	—	SPI data input
	SDA	PBS3 IFS4	ST	NMOS	I^2C data line
PC0/TP1B/TP1BB/TP1IB/SCOM0	PC0	PCPU PCS0	ST	CMOS	General purpose I/O. Register enabled pull-up
	TP1B	PCS0	—	CMOS	TM1 B output
	TP1BB	PCS0	—	CMOS	TM1 inverted B output
	TP1IB	IFS2	ST	—	TM1 B input
	SCOM0	PCS0	—	SCOM	LCD common output

Pad Name	Function	OPT	I/T	O/T	Description
PC1/TP1B/TP1BB/TP1IB/SCOM1	PC1	PCPU PCS0	ST	CMOS	General purpose I/O. Register enabled pull-up
	TP1B	PCS0	—	CMOS	TM1 B output
	TP1BB	PCS0	—	CMOS	TM1 inverted B output
	TP1IB	IFS2	ST	—	TM1 B input
	SCOM1	PCS0	—	SCOM	LCD common output
PC2/PCK/TCK2/C0X	PC2	PCPU PCS1	ST	CMOS	General purpose I/O. Register enabled pull-up
	PCK	PCS1	—	CMOS	Peripheral clock output
	TCK2	IFS1	ST	—	TM2 input
	C0X	PCS1	—	CMOS	Comparator 0 output
PC3/$\overline{\text{PINT}}$/TP2/TP2B/TP2I/C1X	PC3	PCPU PCS1	ST	CMOS	General purpose I/O. Register enabled pull-up
	$\overline{\text{PINT}}$	IFS0	ST	–	Peripheral interrupt
	TP2	PCS1	—	CMOS	TM2 output
	TP2B	PCS1	—	CMOS	TM2 inverted output
	TP2I	IFS2	ST	—	TM2 input
	C1X	PCS1	—	CMOS	Comparator 1 output
PC6/SCOM2/TP0/TP0B	PC6	PCPU PCS3	ST	CMOS	General purpose I/O. Register enabled pull-up
	SCOM2	PCS3	—	SCOM	LCD common output
	TP0	PCS3	—	CMOS	TM0 output
	TP0B	PCS3	—	CMOS	TM0 inverted output
PC7/SCOM3/TP1A/TP1IA	PC7	PCPU PCS3	ST	CMOS	General purpose I/O. Register enabled pull-up
	SCOM3	PCS3	—	SCOM	LCD common output
	TP1A	PCS3	—	CMOS	TM1 A output
	TP1IA	IFS2	ST	—	TM1 A input
PD4/TP2/TP2B/TP2I	PD4	PDPU PDS2	ST	CMOS	General purpose I/O. Register enabled pull-up
	TP2	PDS2	—	CMOS	TM2 output
	TP2B	PDS2	—	CMOS	TM2 inverted output
	TP2I	IFS2	ST	—	TM2 input
PD5/TP0/TP0B	PD5	PDPU PDS2	ST	CMOS	General purpose I/O. Register enabled pull-up
	TP0	PDS2	—	CMOS	TM0 output
	TP0B	PDS2	—	CMOS	TM0 inverted output
PD6/SCK/SCL	PD6	PDPU PDS3	ST	CMOS	General purpose I/O. Register enabled pull-up
	SCK	PDS3 IFS4	ST	CMOS	SPI serial clock
	SCL	PDS3 IFS4	ST	NMOS	I^2C clock line

Pad Name	Function	OPT	I/T	O/T	Description
PE0/$\overline{SCSA}$/INT0	PE0	PEPU PES0	ST	CMOS	General purpose I/O. Register enabled pull-up
	$\overline{SCSA}$	PES0 IFS5	ST	CMOS	SPIA slave select
	INT0	INTEG INTC0 IFS0	ST	—	External Interrupt 0
PE1/SCKA/INT1	PE1	PEPU PES0	ST	CMOS	General purpose I/O. Register enabled pull-up
	SCKA	PES0 IFS5	ST	CMOS	SPIA serial clock
	INT1	INTEG INTC0 IFS0	ST	—	External Interrupt 1
PE2/SDIA/INT2	PE2	PEPU PES1	ST	CMOS	General purpose I/O. Register enabled pull-up
	SDIA	IFS5	ST	CMOS	SPI serial clock
	INT2	INTEG INTC3 IFS0	ST	—	External Interrupt 2
PE3/SDOA/TCK3	PE2	PEPU PES1	ST	CMOS	General purpose I/O. Register enabled pull-up
	SDOA	PES1	ST	CMOS	SPIA serial clock
	TCK3	IFS1	ST	—	TM3 input
PE4/TP1B/TP1BB/TP1IB	PE4	PEPU PES2	ST	CMOS	General purpose I/O. Register enabled pull-up
	TP1B	PES2	—	CMOS	TM1 B output
	TP1BB	PES2	—	CMOS	TM1 inverted B output
	TP1IB	IFS2	ST	—	TM1 B input
PE5/TP3/TP3B	PE5	PEPU PES2	ST	CMOS	General purpose I/O. Register enabled pull-up
	TP3	PES2	—	CMOS	TM3 output
	TP3B	PES2	—	CMOS	TM3 inverted output
PE6/AN8/INT0	PE6	PEPU PES3	ST	CMOS	General purpose I/O. Register enabled pull-up
	AN8	PES3	AN	—	A/D Converter analog input
	INT0	INTEG INTC0 IFS0	ST	—	External Interrupt 0
PE7/AN9/INT1	PE7	PEPU PES3	ST	CMOS	General purpose I/O. Register enabled pull-up
	AN9	PES3	AN	—	A/D Converter analog input
	INT1	INTEG INTC0 IFS0	ST	—	External Interrupt 1
PF0/AN10/C1N	PF0	PFPU PFS0	ST	CMOS	General purpose I/O. Register enabled pull-up
	AN10	PFS0	AN	—	A/D Converter analog input
	C1N	PFS0	AN	—	Comparator 1 inverting input

Pad Name	Function	OPT	I/T	O/T	Description
PF1/AN11/C1P	PF1	PFPU PFS0	ST	CMOS	General purpose I/O. Register enabled pull-up
	AN11	PFS0	AN	—	A/D Converter analog input
	C1P	PFS0	AN	—	Comparator 1 non-inverting input
PF2~PF6	PFn	PFPU	ST	CMOS	General purpose I/O. Register enabled pull-up
PG0/C0X	PG0	PGPU PGS0	ST	CMOS	General purpose I/O. Register enabled pull-up
	C0X	PGS0	—	CMOS	Comparator 0 output
PG1/C1X	PG1	PGPU PGS0	ST	CMOS	General purpose I/O. Register enabled pull-up
	C1X	PGS0	—	CMOS	Comparator 1 output
PG2/TCK4	PG2	PGPU	ST	CMOS	General purpose I/O. Register enabled pull-up
	TCK4	—	ST	—	TM4 input
PG3/TP4/TP4B/TP4I	PG3	PGPU PGS1	ST	CMOS	General purpose I/O. Register enabled pull-up
	TP4	PGS1	—	CMOS	TM4 output
	TP4B	PGS1	—	CMOS	TM4 inverted output
	TP4I	IFS3	ST	—	TM4 input
PG4/TP4/TP4B/TP4I	PG4	PGPU PGS2	ST	CMOS	General purpose I/O. Register enabled pull-up
	TP4	PGS2	—	CMOS	TM4 output
	TP4B	PGS2	—	CMOS	TM4 inverted output
	TP4I	IFS3	ST	—	TM4 input
PG5/TCK5	PG5	PGPU	ST	CMOS	General purpose I/O. Register enabled pull-up
	TCK5	—	ST	—	TM5 input
PG6/TP5/TP5B/TP5I	PG6	PGPU PGS3	ST	CMOS	General purpose I/O. Register enabled pull-up
	TP5	PGS3	—	CMOS	TM5 output
	TP5B	PGS3	—	CMOS	TM5 inverted output
	TP5I	IFS3	ST	—	TM5 input
PG7/TP5/TP5B/TP5I	PG7	PGPU PGS3	ST	CMOS	General purpose I/O. Register enabled pull-up
	TP5	PGS3	—	CMOS	TM5 output
	TP5B	PGS3	—	CMOS	TM5 inverted output
	TP5I	IFS3	ST	—	TM5 input
PH0/TP0/TP0B/AN0/VREF/C0X	PH0	PHPU PHS0	ST	CMOS	General purpose I/O. Register enabled pull-up
	TP0	PHS0	—	CMOS	TM0 output
	TP0B	PHS0	—	CMOS	TM0 inverted output
	AN0	PHS0	AN	—	A/D Converter analog input
	VREF	PHS0	AN	—	A/D Converter reference input
	C0X	PHS0	—	CMOS	Comparator 0 output

Pad Name	Function	OPT	I/T	O/T	Description
PH1/TCK0/AN2/C0P	PH1	PHPU PHS0	ST	CMOS	General purpose I/O. Register enabled pull-up
	TCK0	IFS1	ST	—	TM0 input
	AN2	PHS0	AN	—	A/D Converter analog input
	C0P	PHS0	AN	—	Comparator 0 non-inverting input
PH2/$\overline{\text{SCSA}}$	PH2	PHPU PHS1	ST	CMOS	General purpose I/O. Register enabled pull-up
	$\overline{\text{SCSA}}$	PHS1 IFS5	ST	CMOS	SPIA slave select
PH3/SCKA	PH3	PHPU PHS1	ST	CMOS	General purpose I/O. Register enabled pull-up
	SCKA	PHS1 IFS5	ST	CMOS	SPIA serial clock
PH4/SDIA	PH4	PHPU	ST	CMOS	General purpose I/O. Register enabled pull-up
	SDIA	IFS5	ST	CMOS	SPIA serial data input
PH5/SDOA	PH5	PHPU PHS2	ST	CMOS	General purpose I/O. Register enabled pull-up
	SDOA	PHS2	ST	CMOS	SPIA serial data output
RX	RX	UCR1* UCR2*	ST	—	UART RX serial data input pin.
TX	TX	UCR1* UCR2*	—	CMOS	UART TX serial data output pin.
NC	NC	—	—	—	Not connected.
VDD	VDD	—	PWR	—	Positive Power supply.
VSS	VSS	—	PWR	—	Negative Power supply. Ground.
VSS2	VSS2	—	PWR	—	I/O Pad Power supply. Ground.

Legend: I/T: Input type; O/T: Output type

OPT: Optional by configuration option (CO) or register option

PWR: Power; CO: Configuration option

ST: Schmitt Trigger input; SCOM: Software controlled LCD COM;

CMOS: CMOS output; NMOS: NMOS output

HXT: High frequency crystal oscillator

LXT: Low frequency crystal oscillator

* The UCR1 and UCR2 registers are contained in the HT45B0F chip and used to configure various options of the TX and RX functions in the UART module.

Internally Connected Pins

Among the pins mentioned in the tables above several pins are not connected to external package pins. These pins are interconnection pins between the MCU and the SPI to UART chips and are listed in the following table. The description is provided from the SPI to UART chip standpoint.

SPI-to-UART Chip Pin Name	Type	Description
SDI	I	Slave SPI Serial Data In Input Signal Internally connected to the MCU Master SPI SDO output signal
SDO	O	Slave SPI Serial Data Out Output Signal Internally connected to the MCU Master SPI SDI input signal
SCK	I	Slave SPI Serial Clock Input Signal Internally connected to the MCU Master SPI SCK output signal
$\overline{SCS}$	I	Slave SPI Device Select Input Signal Internally connected to the MCU Master SPI $\overline{SCS}$ output signal – connected to pull high resistor
CLKI	I	Clock Input Signal Internally connected to the MCU Master PCK output signal
$\overline{INT}$	O	UART Interrupt Output Signal Internally connected to the MCU Master $\overline{PINT}$ input signal A UART related interrupt will generate a low pulse signal on this line

Functional Description

As these devices packages contain multiple internal chips, for a detailed functional description, users must refer to the relevant individual datasheets for both the MCU and the SPI to UART chip. The following table shows which individual devices are inside each package.

Device Part No.	Individual chips	
	MCU chip	SPI to UART chip
HT66FU60A	HT66F60A	HT45B0F
HT66FU70A	HT66F70A	

Although most of the functional description material will be located in the individual datasheets, there are some special considerations which need to be taken into account when using multi-chip devices. These points will be mentioned in the hardware and software consideration sections.

Multi-chip Hardware Considerations

As these single-package multi-chip devices are composed of an individual MCU and SPI to UART chips, using them together requires the user to take care of some special points.

Absolute Maximum Ratings

As these single-package multi-chip devices are composed of an individual MCU and SPI to UART chips, using them together requires the user to take care of some special points.

Power Supply

To calculate the power consumption for the devices, the total operating currnt is the sum of the operating current for the MCU specified in the MCU datasheet and the operating current for the SPI to UART chip listed in the HT45B0F datasheet. Similarly, the standby current is the sum of the two individual chip standby currents.

Power Down and Wake up

The MCU and SPI to UART chip are powered down independently of each other. The method of powering down the MCU is covered in the relevant MCU datasheet section. Note that the SPI to UART chip must be powered down before the MCU is poweed down.

After the device is powered down, it can also be woken up by the SPI to UART chip interrupt except by wake-up sources mentioned in the MCU datasheet. When a UART interrupt occurs on the $\overline{\text{INT}}$ line internally connected to the MCU $\overline{\text{PINT}}$ line, it will wake up the MCU if the MCU has entered a power down mode. After the MCU is woken up, the application program must set the corresponding control bits to make the device function normally.

Interrupts

When a UART interrupt occurs, a low pulse will be generated on the $\overline{\text{INT}}$ line and sent to the MCU peripheral interrupt line $\overline{\text{PINT}}$ to get the attention of the microcontroller. When the UART interrupt caused by one of the UART interrupt generation sources occurs, if the corresponding interrupt control in the host MCU is enabled and the MCU stack is not full, the program will jump to the corresponding interrupt vector where it can be serviced before returning to the main program.

For a UART interrupt to be serviced, in addition to the bits for the corresponding interrupt enable control in the SPI to UART chip being set, the global interrupt enable control and the related interrupt enable control bits in the host MCU must also be set. If these bits are not set, then the interrupt signal will only be a wake-up source and no interrupt will be serviced.

Unbonded MCU pins

Examination of the relevant MCU datasheet will reveal that not all of the MCU I/O port lines are bonded out to external pins. As a result special attention regarding initialixation procedures should be paid to these port lines. If the pins are pin-shared with the analog input pins, they will be setup as analog inputs and the corresponding analog circuits will be disabled after a reset. When these pins are set as analog input pins and the relevant circuits are disabled, they will not consume any power even if the input pin conditions are not kept as either high or low logic levels. However, if the pins are not pin-shared with analog input pins, they will be setup as input states without pull high resistors after a reset. Users should therefore ensure that these pins are setup in input states with pull high resistors or in output states with either a high or low level to avoid additional power consumption resulting from floating input pins.

Multi-chip Programming Considerations

To use the UART function, several important steps must be implemented to ensure that the SPI to UART chip operates normally.

- The SPI interface pin-shared function must be properly configured when the SPI functional pins of the microcontroller are used to control the SPI to UART chip and for transmission and reception.

  To ensure proper setup between the MCU Master SPI to the SPI to UART chip Slave SPI, the SIM pin-shared function settings together with the PCK and $\overline{\text{PINT}}$ pins in the corresponding MCU pin-shared function selection registers should be setup as shown in the following table.

  - $\overline{\text{SCS}}$ pin-shared function setup in the PDS0 Register

Register	Bit No.	Bit Name	Setting Value
PDS0	3~0	PD0S [3:0]	0010

  - SCK pin-shared function setup in the PDS0 Register

Register	Bit No.	Bit Name	Setting Value
PDS0	7~4	PD1S [3:0]	0010

  - SDI/SDA pin-shared function setup in the PDS1 and IFS4 Registers

Register	Bit No.	Bit Name	Setting Value
PDS1	3~0	PD2S [3:0]	0010
IFS4	5~4	SDIS [1:0]	10, 11

  - SDO pin-shared function setup in the PDS1 Register

Register	Bit No.	Bit Name	Setting Value
PDS1	7~4	PD3S [3:0]	0100

  - PCK pin-shared function setup in the PCS2 Register

Register	Bit No.	Bit Name	Setting Value
PCS2	7~4	PC5S [3:0]	0001

  - $\overline{\text{PINT}}$ pin-shared function setup in the PCS2 and IFS0 Registers

Register	Bit No.	Bit Name	Setting Value
PCS2	3~0	PC4S [3:0]	0000
IFS0	7~6	PINTBS [1:0]	01, 10, 11

- The SIM operating mode control bits SIM2~SIM0 in the SIMC0 register have to be configured to enable the SIM to operate in the SPI master mode with a different SPI clock frequency.
  - SIM operating mode control bits SIM2~SIM0 in the SIMC0 Register

Register	Bit	Name	Setting value
SIMC0	7~5	SIM [2:0]	000, 001, 010, 011, 100

SIM [2:0]: SIM Operating Mode Control
000: SPI master mode; SPI clock is f_{SYS}/4
001: SPI master mode; SPI clock is f_{SYS}/16
010: SPI master mode; SPI clock is f_{SYS}/64
011: SPI master mode; SPI clock is f_{SUB}
100: SPI master mode; SPI clock is TM0 CCRP match frequency/2
101~111: must not be used

- The PCK enable control bit, TB2EN, must be set to 1 to enable the PCK output as the clock source for the SPI to UART chip external clock input with various PCK output frequencies determined by the TB22, TB21 and TB20 bits in the TBC2 Register together with the peripheral clock source selection bits, CLKS11 and CLKS10, in the PSC1 register.
  - PCK output frequency selection bits PCKP1~PCKP0 in the SIMC0 Register

Register	Bit No.	Bit Name	Setting Value
TBC2	7	TB2EN	1
	2~0	TB2 [2:0]	000~111
PSC1	1~0	CLKS1 [1:0]	00~11

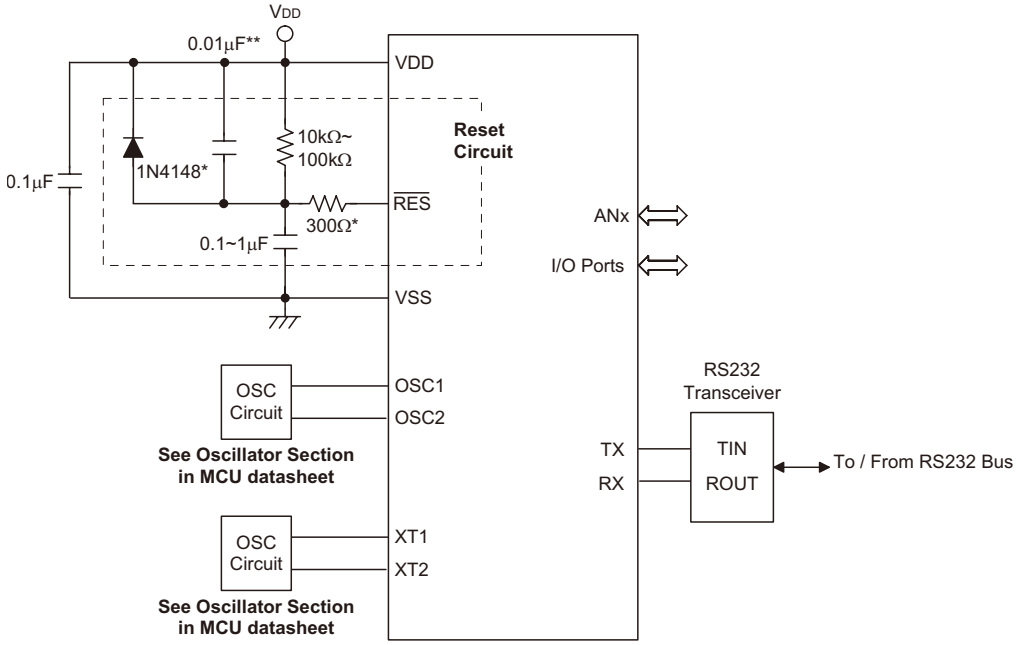
CLKS1 [1:0]: Peripheral Clock Source Selection – f_P
00: f_P is derived from f_{SYS}
01: f_P is derived from f_{SYS}/4
10: f_P is derived from f_{SUB}
11: f_P is derived from f_H

TB2 [2:0]: Peripheral Clock Output Division Selection
000: f_P
000: f_P/2
000: f_P/4
000: f_P/8
000: f_P/16
000: f_P/32
000: f_P/64
000: f_P/128

The special attention must be paid to the peripheral clock output division selection together with the clock source selection to obtain a proper clock frequency to drive the SPI to UART chip to generate certain baud rates.

After the above setup conditions have been implemented, the MCU can enable the SIM interface by setting the SIMEN bit high. The MCU can then begin communication with external UART connected appliances using its SPI interface. The detailed functional descriptions of the MCU Master SPI are provided within the Serial Interface Module section of the relevant MCU datasheet.

Application Circuits



Note: "*" It is recommended that this component is added for added ESD protection.

"**" It is recommended that this component is added in environments where power line noise is significant.

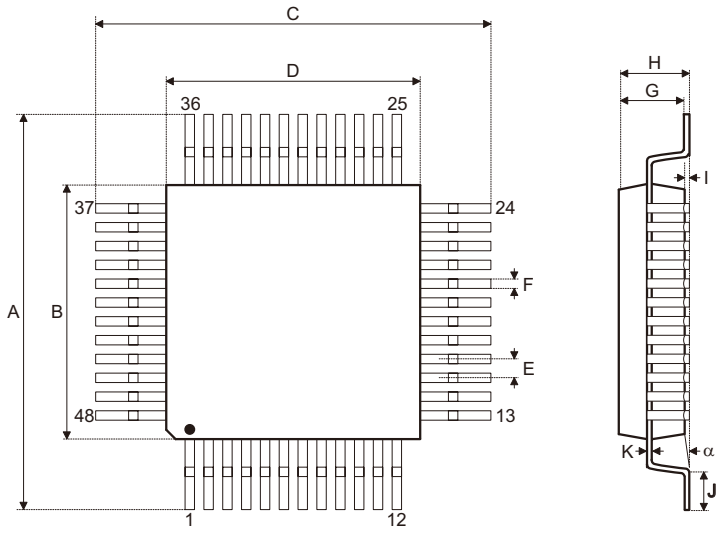
Package Information

Note that the package information provided here is for consultation purposes only. As this information may be updated at regular intervals users are reminded to consult the Holtek website for the latest version of the package information.

Additional supplementary information with regard to packaging is listed below. Click on the relevant section to be transferred to the relevant website page.

- Further Package Information (include Outline Dimensions, Product Tape and Reel Specifications)
- Packing Meterials Information
- Carton information
- PB FREE Products
- Green Packages Products

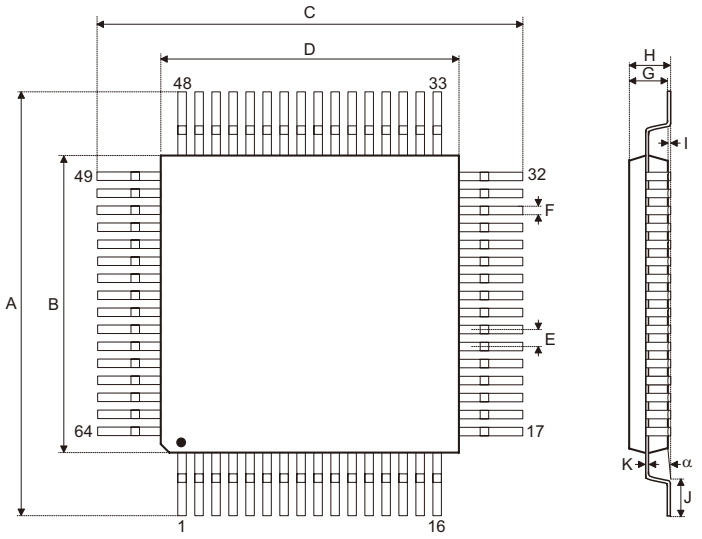
48-pin LQFP (7mm×7mm) Outline Dimensions



Symbol	Dimensions in inch		
	Min.	Nom.	Max.
A	0.350	—	0.358
B	0.272	—	0.280
C	0.350	—	0.358
D	0.272	—	0.280
E	—	0.020	—
F	—	0.008	—
G	0.053	—	0.057
H	—	—	0.063
I	—	0.004	—
J	0.018	—	0.030
K	0.004	—	0.008
α	0°	—	7°

Symbol	Dimensions in mm		
	Min.	Nom.	Max.
A	8.90	—	9.10
B	6.90	—	7.10
C	8.90	—	9.10
D	6.90	—	7.10
E	—	0.50	—
F	—	0.20	—
G	1.35	—	1.45
H	—	—	1.60
I	—	0.10	—
J	0.45	—	0.75
K	0.10	—	0.20
α	0°	—	7°

64-pin LQFP (7mm×7mm) Outline Dimensions



Symbol	Dimensions in inch		
	Min.	Nom.	Max.
A	0.350	—	0.358
B	0.272	—	0.280
C	0.350	—	0.358
D	0.272	—	0.280
E	—	0.016	—
F	0.005	—	0.009
G	0.053	—	0.057
H	—	—	0.063
I	0.002	—	0.006
J	0.018	—	0.030
K	0.004	—	0.008
α	0°	—	7°

Symbol	Dimensions in mm		
	Min.	Nom.	Max.
A	8.90	—	9.10
B	6.90	—	7.10
C	8.90	—	9.10
D	6.90	—	7.10
E	—	0.40	—
F	0.13	—	0.23
G	1.35	—	1.45
H	—	—	1.60
I	0.05	—	0.15
J	0.45	—	0.75
K	0.09	—	0.20
α	0°	—	7°

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