MOTOROLA

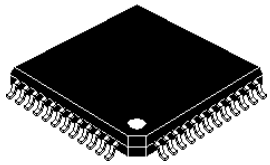
*Advance Information*

# NTSC Digital Video Encoder

## HCMOS Technology

**MC44722**
**MC44723**

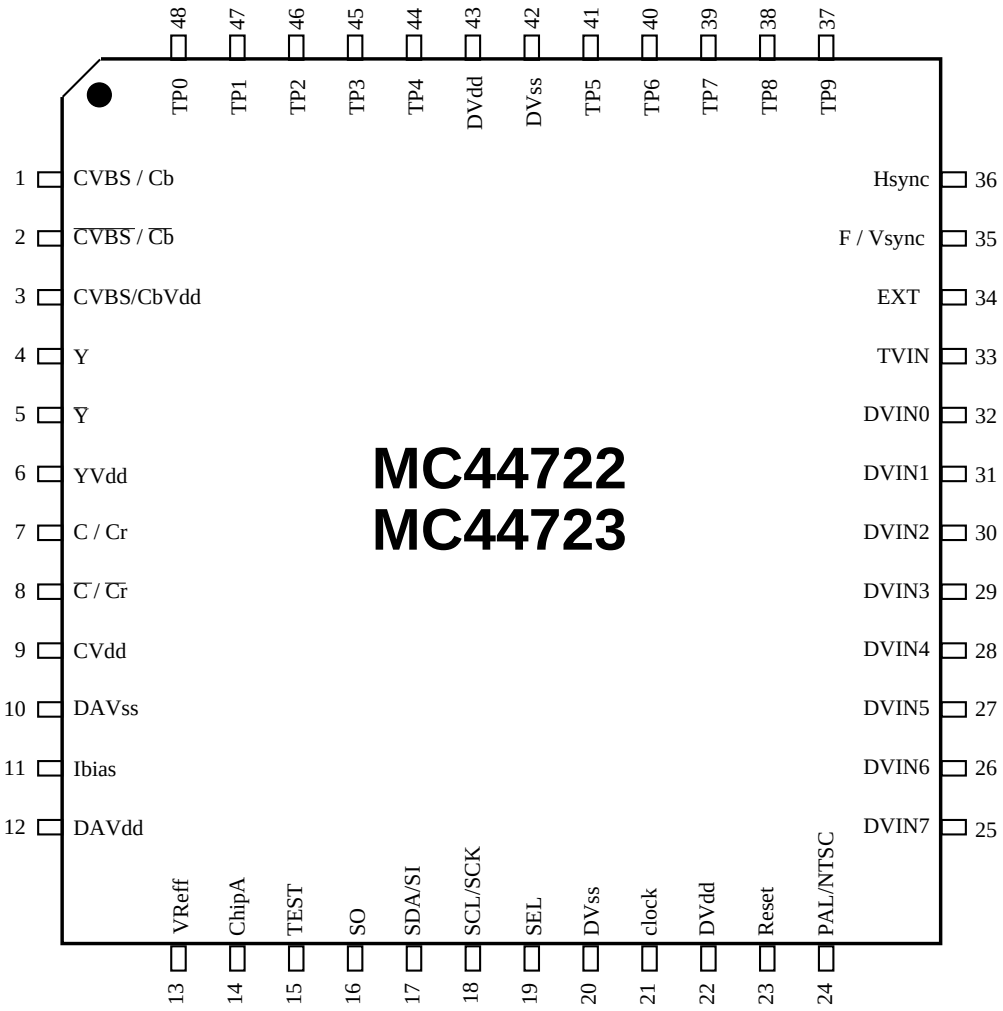
The MC44722 and MC44723 are Digital Video Encoders (DVE). They convert ITU-601/656 standard 4:2:2 Bit-Paralellel data into analog composite video, S-Video or Y/Cb/Cr in PAL and NTSC formats. They accept the multiplexed ((CB,Y,CR)Y) signals from digital sources such as MPEG decoders and can act as a sync generator master. All video processing is done digitally and requires no external adjustment.
Specifically designed for digital satellite, digital cable decoders and multimedia terminals.



FT SUFFIX
48 QFP
(0.8mm Pitch)

- World Wide Operation (PAL-BDGHI, PAL-N,PAL-M, NTSC-M)
- SMPTE **170M** / ITU - **R 624** composite video output
- Programmable Color Sub-carrier Frequencies
- **Analog Horizontal**, **Vertical**, **Frame** or **Composite** Sync Outputs
- Sync Extraction From Digital Input Data (SAV, EAV)
- Sync Polarity and Horizontal Phase Control
- Master or Slave Sync (**H/Vsync, H/Fsync, ITU-R656 slave**) Operation
- Interlaced or Non-Interlaced Support
- 625/50 or 525/60 ITU-601/656 **8-bit** ((CB,Y,CR)Y) Digital Input
- Luma 2X / Chroma 4X Oversampling Filtering
- **External VBI Information Data Input** (such as TeleText Information Data)
- **CVBS / YS / CS** or **Y / Cb / Cr** Analog Outputs Through **10-bit** DACs
- Easily programmed via Serial Bus ( **I2C** or **SPI** Bus)
- **2 Hardware I2C Chip Addresses**
- **Closed-Caption** and **CGMS** Information data Insertion
- **MACROVISION ver. 7.01** Anti-Copy Signal Insertion
  **(MC44722 Only support NTSC mode)**
- On Chip **Color - bar** Generator
- **+3.3V** Power Supply or **+3.3V**(Digital)/**+5V**(Analog) Power Supply
- Pin Compatible with **MC44720FT**

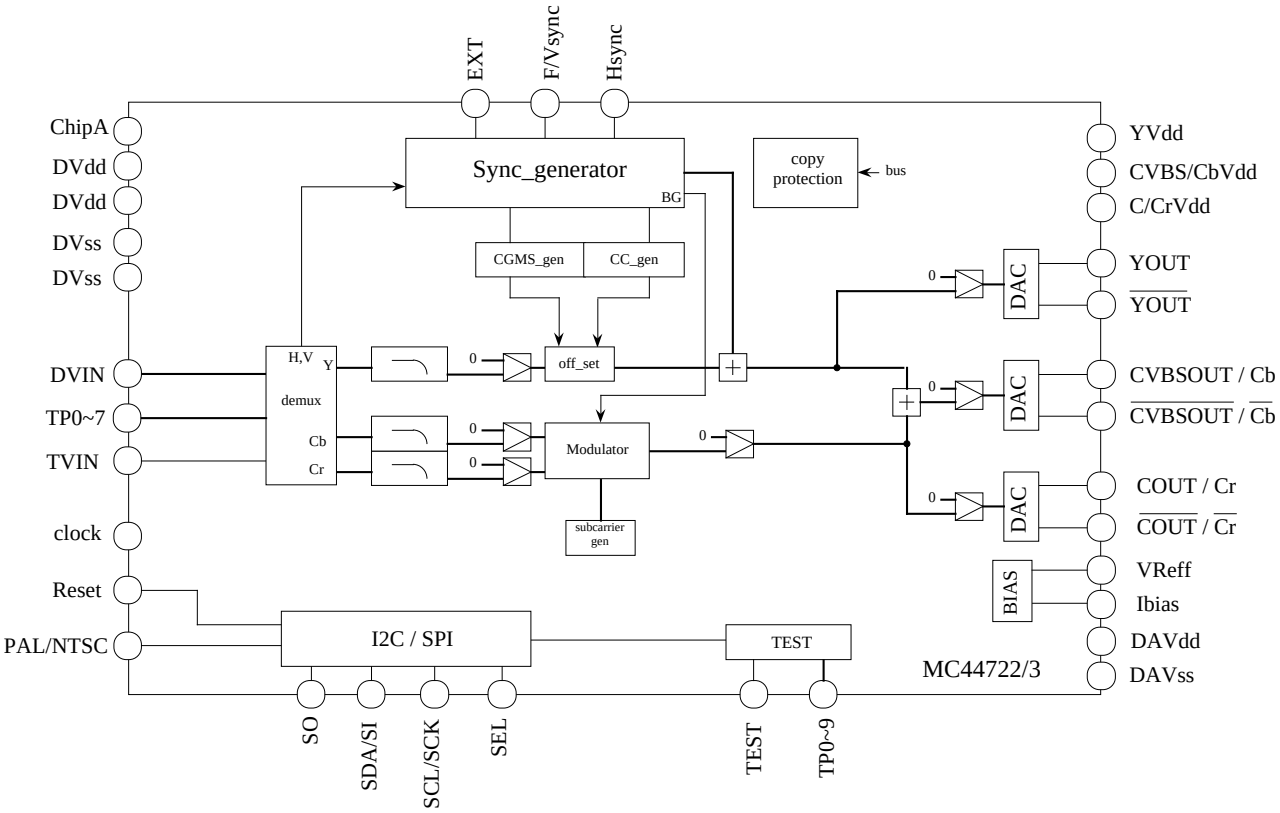
## *[Pin Assignment]*



## *[Pin Descriptions]*

| PIN | NAME | I/O | DESCRIPTIONS |
|---|---|---|---|
| 1 | CVBS / Cb | O | Analog composite video signal output or Cb signal output current drive(positive) |
| 2 | $\overline{\text{CVBS}}$ /$\overline{\text{Cb}}$ | O | Analog composite video signal output or Cb signal output current drive(negative) |
| 3 | CVBS/CbVdd | | Power Supply for CVBS / Cb DAC circuit |
| 4 | Y | O | Analog luminance signal output current drive(positive) |
| 5 | $\overline{\text{Y}}$ | O | Analog luminance signal output current drive(negative) |
| 6 | YVdd | | Power Supply for Y DAC circuit |
| 7 | C/Cr | O | Analog chrominance signal output or Cr signal output current drive(positive) |
| 8 | $\overline{\text{C}}$/$\overline{\text{Cr}}$ | O | Analog chrominance signal output or Cr signal output current drive(negative) |
| 9 | C/CrVdd | | Power Supply for C / Cr DAC circuit |
| 10 | DAVss | | Ground for DAC circuit |
| 11 | Ibias | O | Reference current for the 3 DACs |
| 12 | DAVdd | | Power Supply for DAC circuit |
| 13 | VReff | | Reference full scale voltage for the 3 DACs |
| 14 | ChipA | | I2C chip address select { 0 : 42(hex)/43(hex) 1 : 1C(hex )/1D(hex) } |
| 15 | TEST | I | TEST pin(Ground) |
| 16 | SO | z(O) | If SPI mode, serial data output / If I2C mode, connect to Ground |
| 17 | SDA/SI | I/O(I) | Serial data input, Open drain output / If SPI mode, serial data input |
| 18 | SCL/SCK | I | Serial clock |
| 19 | SEL | (I) | Connect to Ground / If SPI mode, this pin is chip select |
| 20 | DVss | | Ground for Digital circuit |
| 21 | CLOCK | I | 27MHz clock input |
| 22 | DVdd | | Power Supply for Digital circuit |
| 23 | Reset | I | Reset signal, active LOW |
| 24 | PAL/NTSC | I | NTSC/PAL select . This pin active only Reset time. (NTSC : Low PAL : High ) |
| 25~32 | DVIN7~0 | I | 8-bit Multiplexed Y/Cr/Cb 4:2:2 data(CCIR Rec656) input(1) |
| 33 | TVIN | I | TEST data input |
| 34 | EXT | I/O | Csync/Frame sync output or external VBI information input |
| 35 | F/Vsync | I/O | Frame sync or Vertical sync input/output |
| 36 | Hsync | I/O | Horizontal sync input/output |
| 37 | TP9 | I/O | for D/A converter test |
| 38 | TP8 | I/O | MUX switch in 8-bit Multiplexed Y/Cr/Cb 4:2:2 data(CCIR Rec656) input mode, or |
| | | | Test data input/output |
| 39~41 | TP7~5 | I/O | 8-bit Multiplexed 4:2:2 data(CCIR Rec656/601) input(2), or Multiplexed Cr/Cb data |
| | | | (CCIR Rec656/601) input in 16-bit input mode (MSB : TP7), or Test data input/output |
| 42 | DVss | | Ground for Digital circuit |
| 43 | DVdd | | Power Supply for Digital circuit |
| 44~48 | TP4~0 | I/O | 8-bit Multiplexed 4:2:2 data(CCIR Rec656/601) input(2), or Multiplexed Cr/Cb data |
| | | | (CCIR Rec656/601) input in 16-bit input mode (LSB : TP0), or Test data input/output |

## *[Block Diagram]*




I2C/SPI chip-address 42/43(hex)
1C/1D(hex)

## *[Function Descriptions]*

### Clock

27.0Mhz is necessary. This signal on the clock pin needs to be active before the reset pin is de-asserted.
( see figures 1 and 2 )

### Reset Procedure

RESET is a level sensitive input pin. Driving the RESET pin low causes a DVE reset. The 27Mhz DVE clock signal must be active before RESET is released. De-asserting reset will latch the status of the PAL/ NTSC, TVIN and SEL pins.
The PAL/NTSC pin determines the default values for the DVE control registers. The default register values have been chosen so that standard PAL or NTSC video will appear at the DAC outputs immediately when a valid input digital video data stream is present.
The value on the SEL pins determine the default serial communication mode. If Low, the DVE use I2C bus operation. If High, the DVE use 4-wire SPI operation.

After reset, the VBI signals (Closed-Caption and CGMS) are disabled.

(see page --- for sub-address register descriptions.)

**Fig 1 : DVIN Data Input Timing**

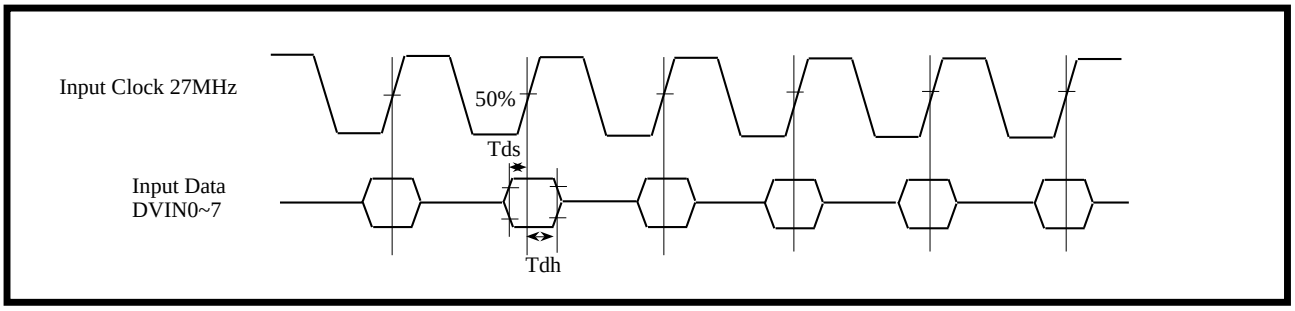
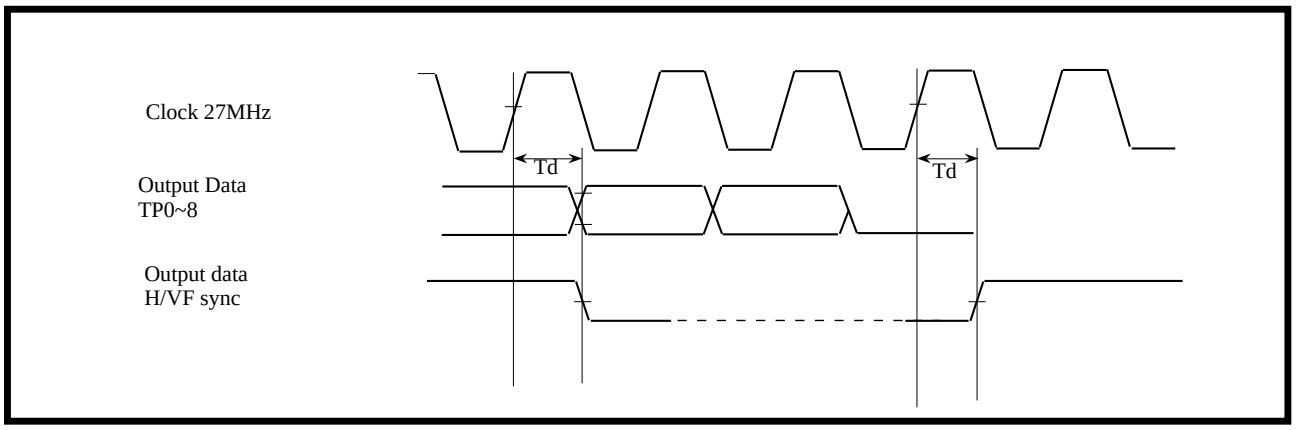



**Fig 2 : Sync Data Output Timing**



## Input Data Format

The input digital video is in accord with the ITU-R Rec.656 and SMPTE 125M standards. It is two 8-bit or 16-bit multiplexed 4:2:2 ((CB,Y,CR)Y) data stream. Samples are latched on the rising edge of the clock signal. Data is input on pins **DVIN[ 7 : 0 ]** and TP[ 8 : 1 ]
(see figures 3 and 4 for sub-address register descriptions.)

## Video Timing / Sync Generator

The DVE outputs PAL-B,D,G,H,I, PAL-N, PAL-M or NTSC-M standard video signals.
The DVE sync generator can be operated in two modes, master or slave.
In master mode, the DVE generates all the correct Horizontal and Vertical or Frame sync signals internally, or it is output Csync signal through the EXT pin(C/Fsync).
In slave mode, the DVE derives the sync signals from the Bit-Parallel input data stream Start Active Video (SAV) and End Active Video (EAV) data packet information. Sync signals are output on the Hsync and F/Vsync or EXT pins and can be programmed for positive or negative polarity. The phase of Hsync can also be controlled.
Also, the DVE allows more two slave modes. One is H/Vsync slave, and the aother is H/Fsync slave mode.
Vertical Blanking corresponds to the following lines.

625/50 624-22 311-335 ITU-R line numbering
525/60 1-19 264-282 SMPTE line numbering

(see figures 3,4,5,6,7,8,9,10, and 11 for sub-address register descriptions.)

**Fig 3 : Digital Input Timing(525/60 system) in Master Mode** 70(hex){[1:0]=01}

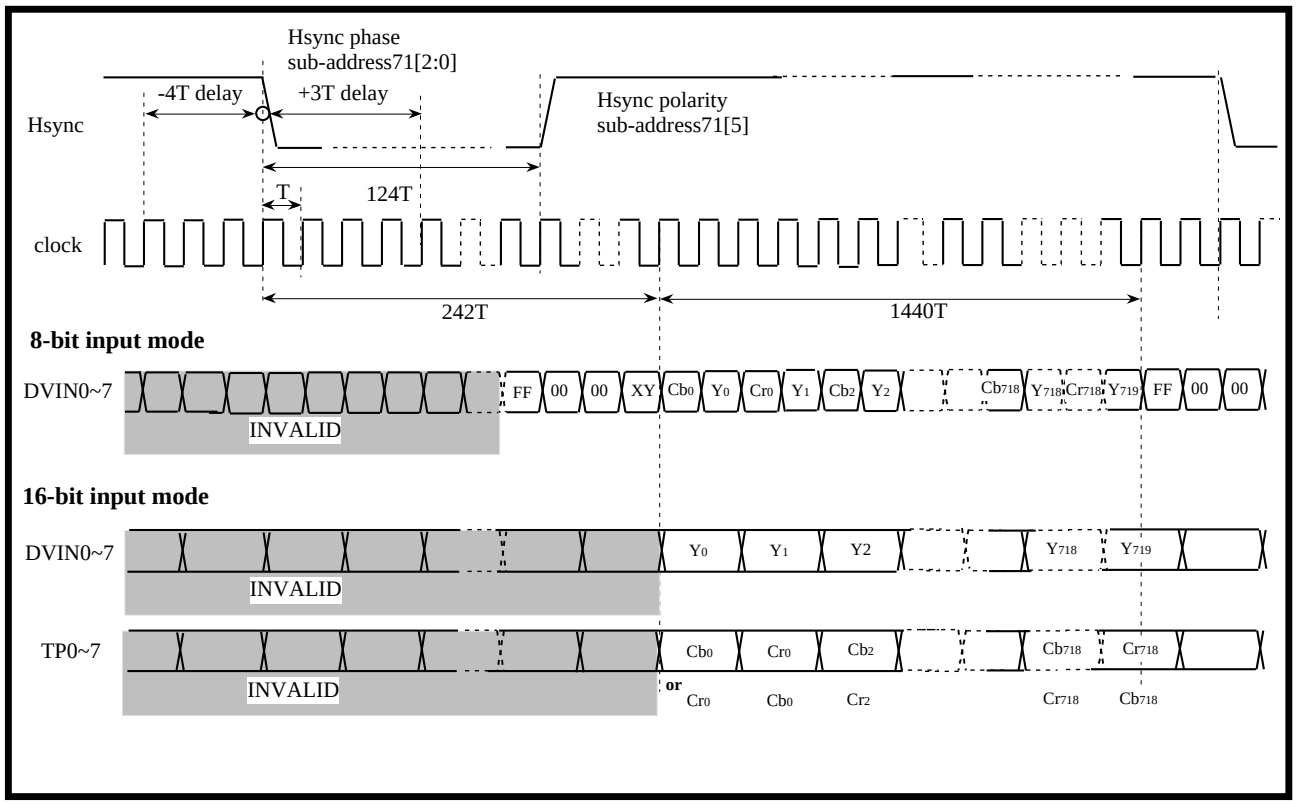


**Fig 4 : Digital Input Timing(625/50 system) in Master Mode** 70(hex){[1:0]=01}

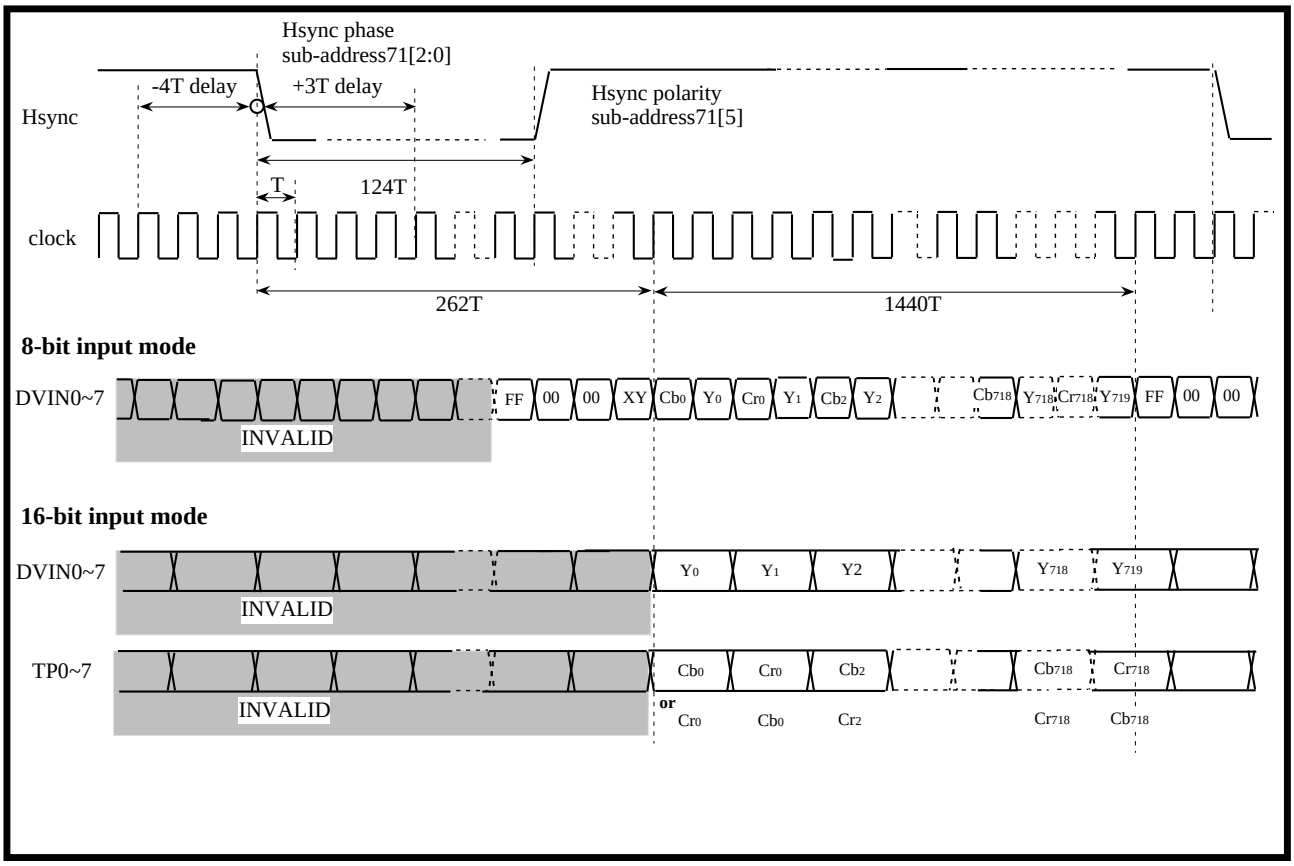



**Fig 5 : Sync Timing::525/60 Interlaced System in Master Mode** sub-address71[7] =0

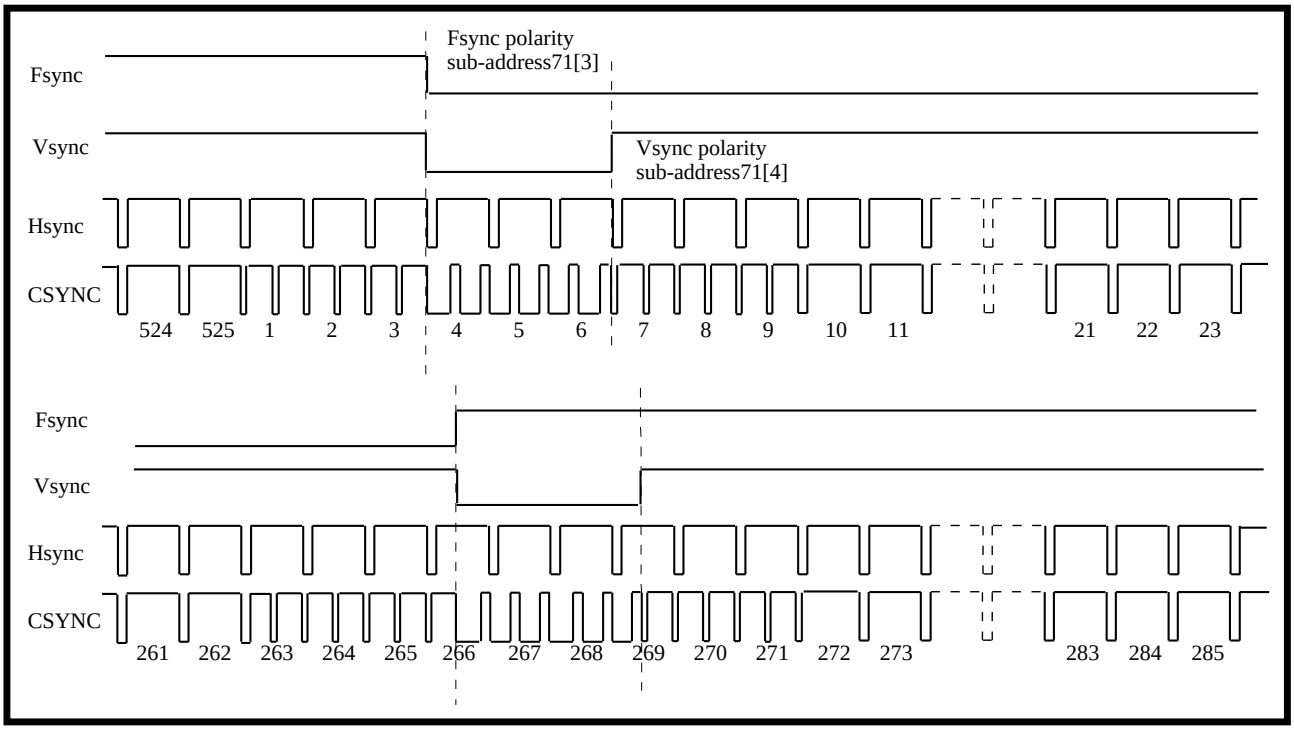


**Fig 6 : Sync Timing::625/50 Interlaced System in Master Mode** sub-address71[7] =0

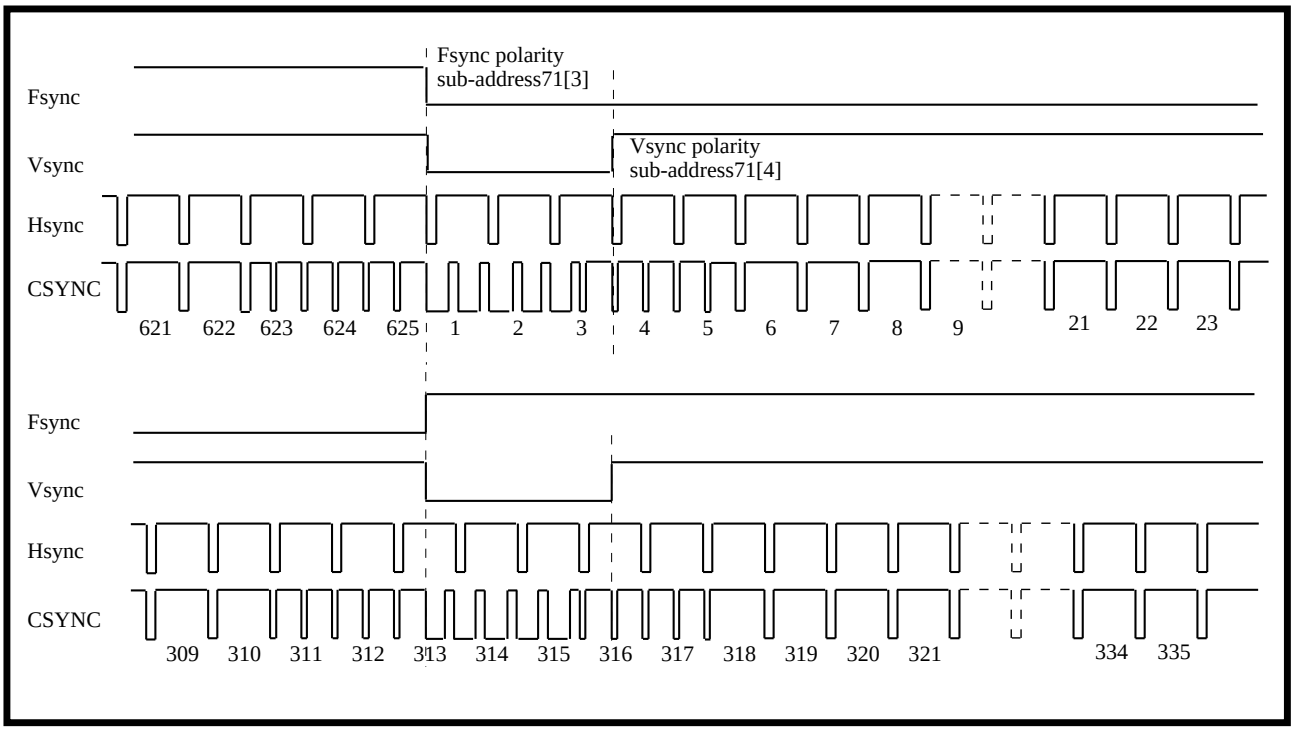



**Fig 7 : Sync Timing::525/60 Non-interlaced System in Master Mode** sub-address71[7] =1

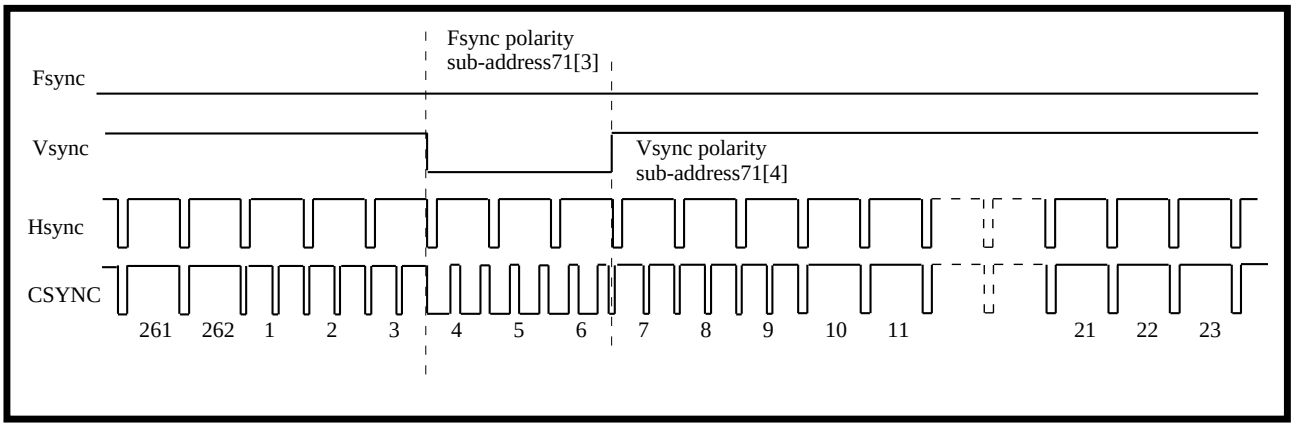



**Fig 8 : Sync Timing::625/50 Non-interlaced System in Master Mode** sub-address71[7] =1

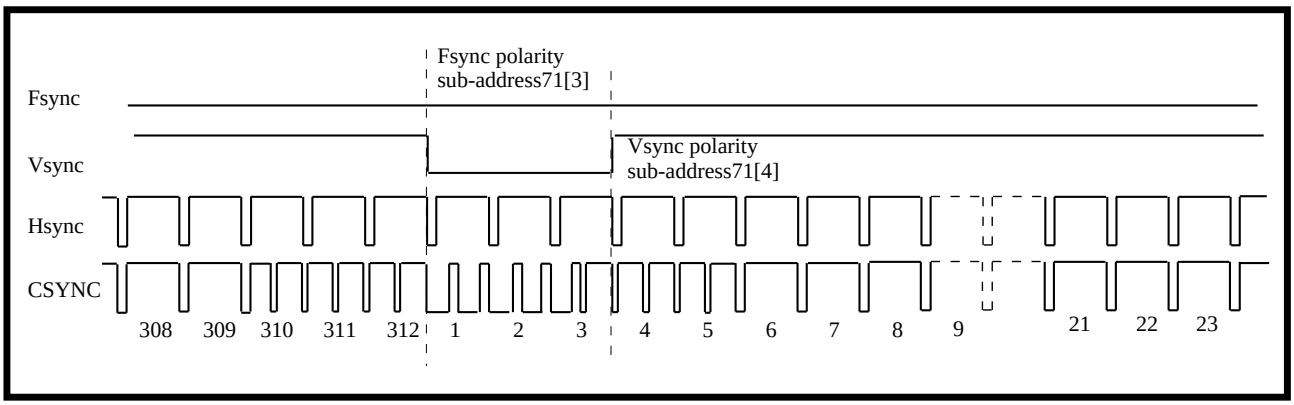


**Fig 9 : Analog Sync Timing::Rise and fall**

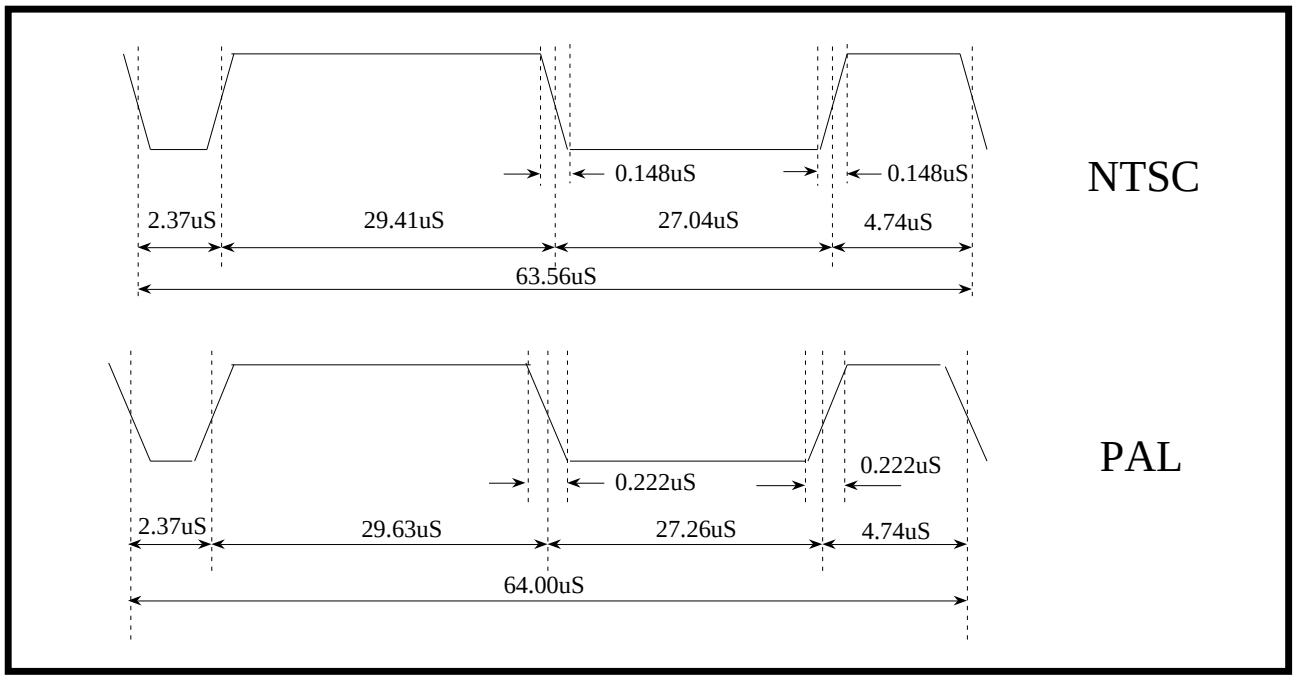



**Fig 10 : Sync Timing::525/60 Interlaced System in Slave Mode** sub-address71[1:0] =10, 11

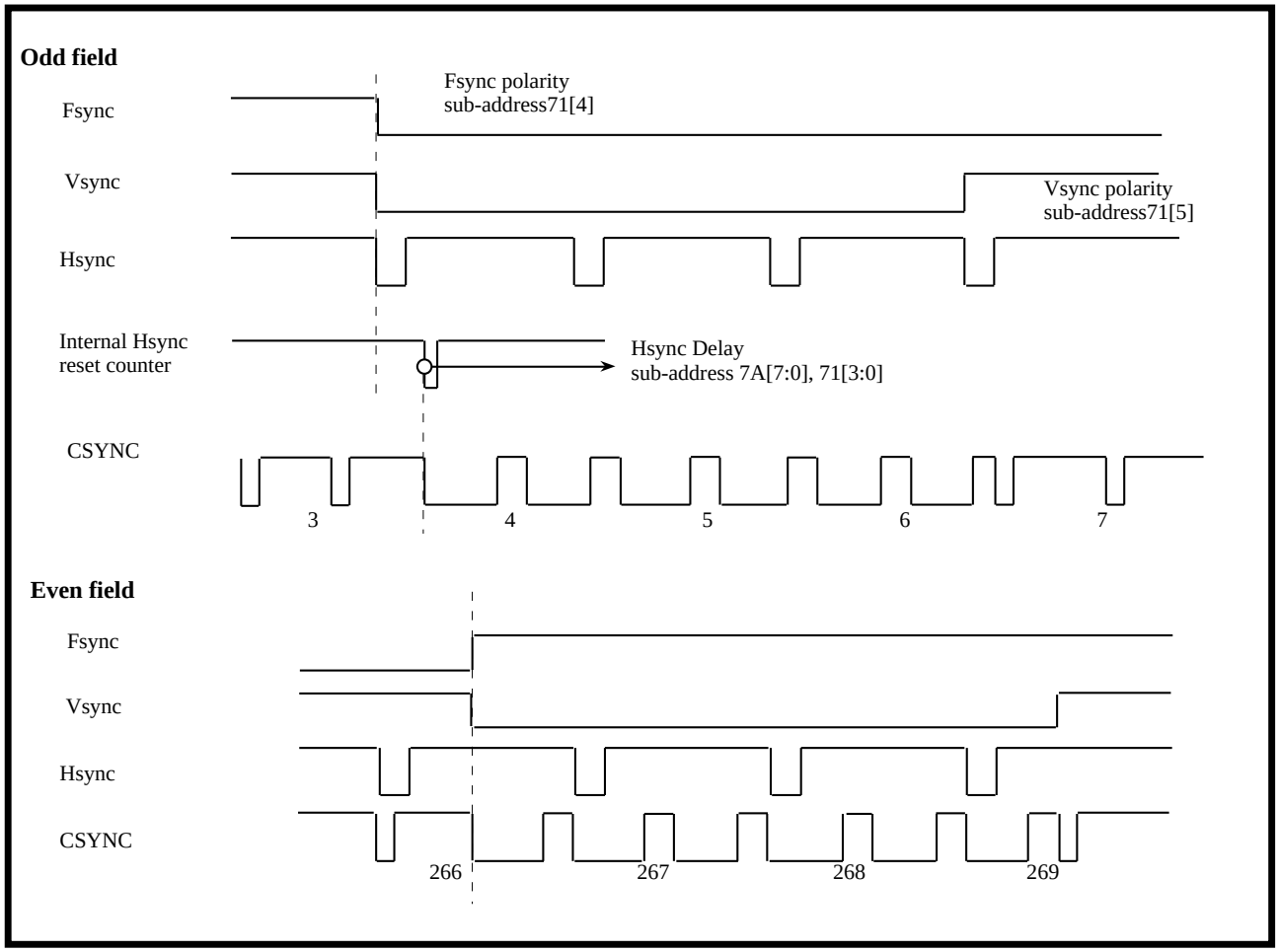
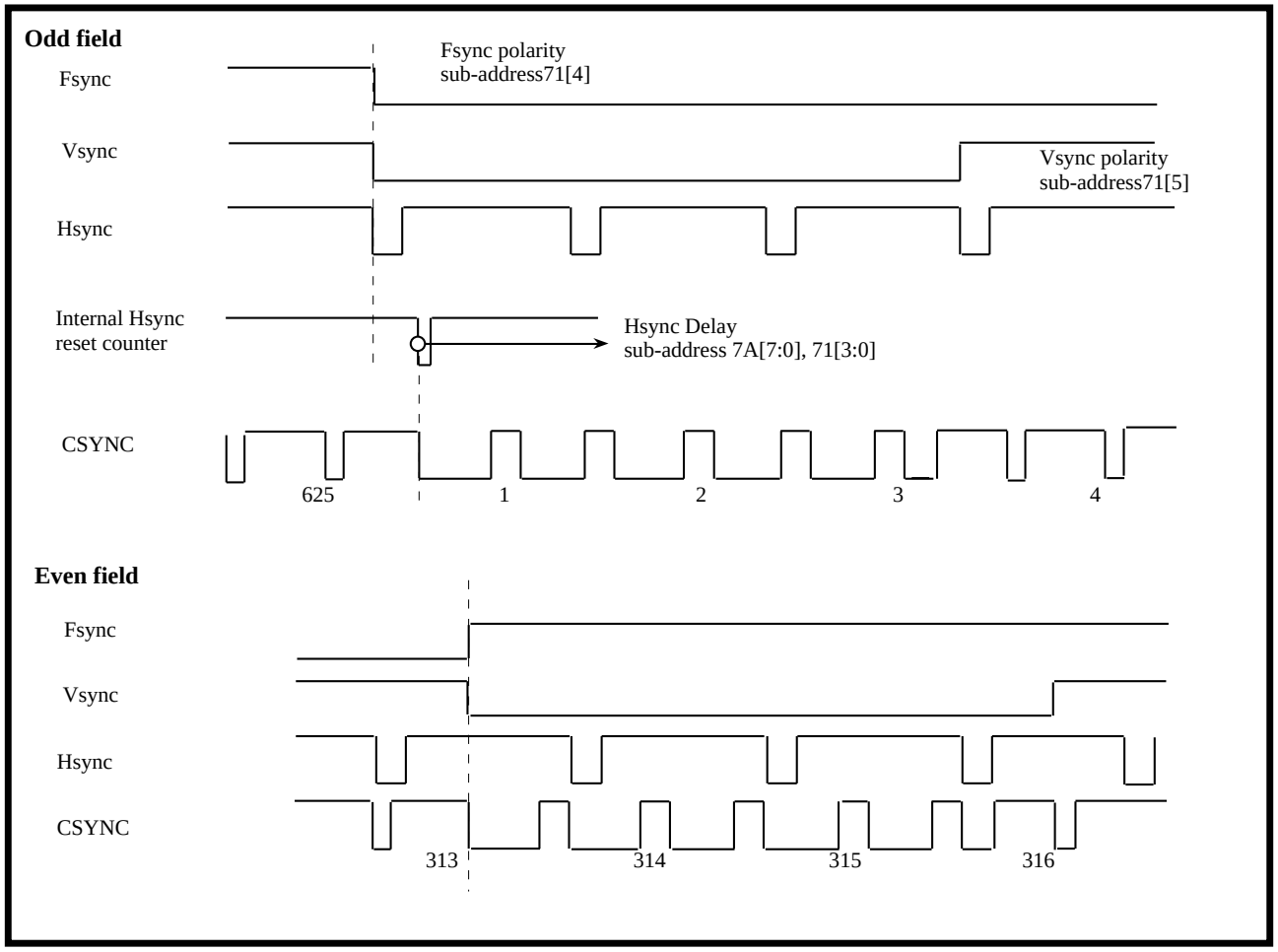


**Fig 11 : Sync Timing::625/50 Interlaced System in Slave Mode** sub-address71[1:0] =10, 11



## Chroma / Luma Encoding

The DVE de-multiplexes the 4:2:2 digital video data stream.

The de-multiplexed Y or Luma samples are interpolated (2X oversampled) at the clock rate. Offset compensation is then added, next any VBI signals consisting of Closed-Caption and VID are added to the appropriate lines, then finally composite sync pulses are added to the Luma signal. (see figure 12.)

De-multiplexed component color CB and CR samples are interpolated (4X oversampled) at the clock rate. Interpolating simplifies the output filter and allows more accurate encoding. The DVE generates the necessary subcarrier color frequency for PAL or NTSC encoding from the 27Mhz system clock. This color subcarrier is then modulated by the base band component color CB and CR signals to create the video Chroma signal. (see figure 13.)

A 7.5 IRE pedestal is added for the 60Hz field rate. This can be added for the 50Hz field rate through serial bus control. (see sub-address register descriptions)

## CVBS and S-VIDEO or YCbCr Outputs

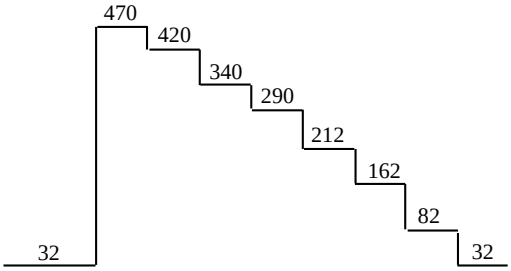
The internal digital video signals drive 10-bit D/A converters. Converter outputs are bi-directional current sources where the current is proportional to the digital data with reference to the IBIAS reference current. The pins CVBS/Cb, Y and C/Cr are the respective composite, Luma and Chroma or Y/Cb/Cr signal current source pins. Also, each DACs can drive **75ohm** load register.

(see "Application Diagram" and "sub-address register descriptions".)

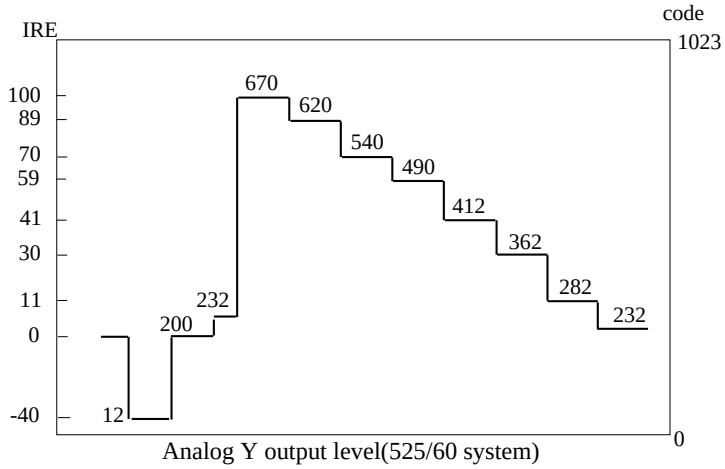
Bias Current Gain

DACs can be switched off through serial bus control to reduce power consumption. Both outputs of unused DACs should be connected to ground through a resister to avoid charge buildup.

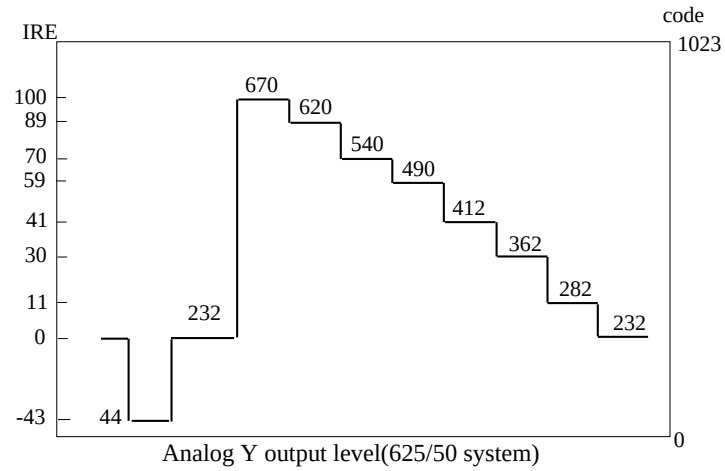
**Fig 12 : Luminance Output Range**




Digital Y input code(16~235)
525/60 and 625/50 system
100%amplitude,100%saturation color bar

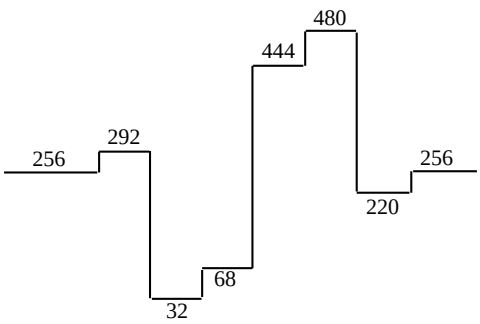



Analog Y output level(525/60 system)
100%amplitude,100%saturation color bar

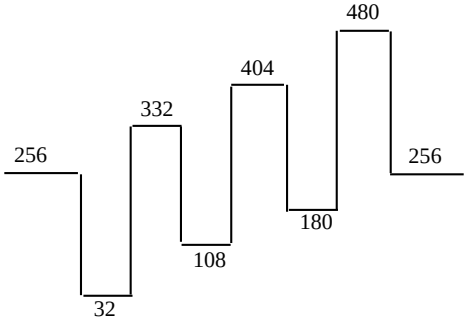



Analog Y output level(625/50 system)
100%amplitude,100%saturation color bar

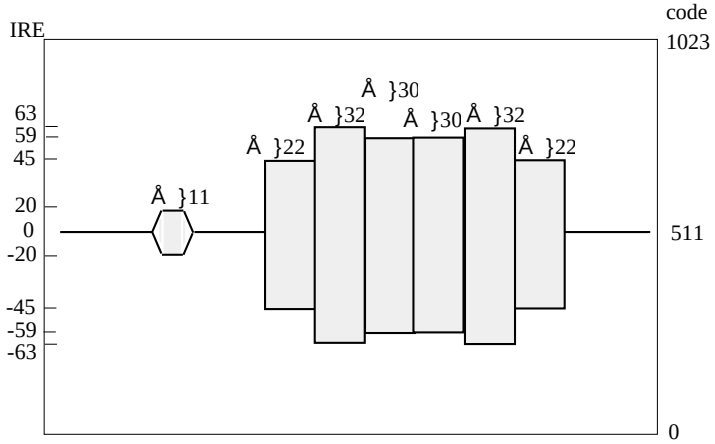
**Fig 13 : Chrominance Output Range**



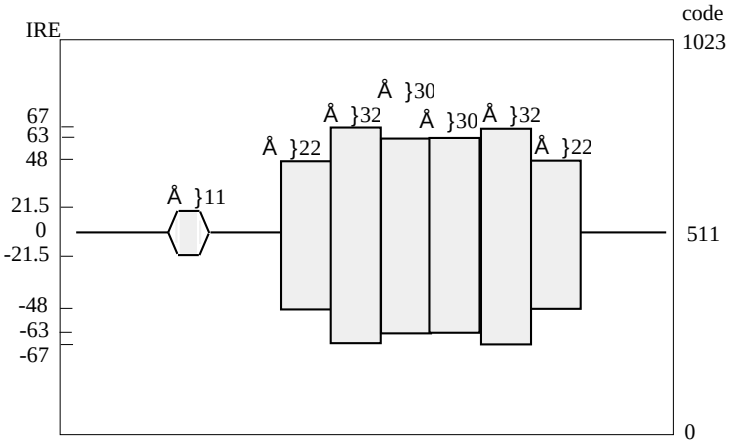

Digital Cr-input code(16~240)
525/60 and 625/50 system
100%amplitude,100%saturation color bar




Digital Cb-input code(16~240)
525/60 and 625/50 system
100%amplitude,100%saturation color bar




Analog C output level(525/60 system)
100%amplitude,100%saturation color bar




Analog C output level(625/50 system)
100%amplitude,100%saturation color bar

## Copy Generation Managment System (CGMS) Encoding

CGMS signals can be encoded by the DVE onto output video line 20 (525 / 60 for Japan).
CGMS identification signals also identify and control the TV screen presentation mode - wide screen, letterbox and or normal -16:9 or 4:3.

(see figures 16 for sub-address register descriptions.)

## Closed-Caption Encoding

Closed-Captioned or Extended Data Service signals can be encoded by the DVE onto output video line 21/284 (NTSC) and line 22/335 (PAL). The CC data is input through the serial bus interface. Two 8-bit byte data pairs are encoded for each field. There are four registers for holding the data - two bytes per field. The serial data is 7bit US-ASCII MSB first, proceeded by an odd parity bit. Total 8-bits. (P-7-6-5-4-3-2-1-0)
The DVE automatically generates the required clock run in and start bit for CC encoding. (see figure 16.)
When Closed-Captioning is enabled, the system micro processor (uP) should update the CC data once each frame. The system uP should also write NULL characters when there is no CC data to encode. It is also recommended to write CC data only to the inactive frame. Field1 and Field2 data are double-buffered by the Frame sync falling edge of previous Frame, updating Frame 2 data during Frame1 display and Frame1 data during Frame2 display.

(see figures 18 for sub-address register descriptions.)

## Serial Control Bus

Control of the DVE device is accomplished through the I2C-Bus or SPI serial bus.
In I2C mode, pins SDA and SCL are the respective data and clock signals. Device address can be 42(hex)/43(hex) or 1C(hex)/1D(hex) . Slave address is chosen at reset by the state of the ChipA pin signal { 0 : 42(hex)/43(hex), 1 : 1C(hex)/1D(hex) }
Sub-address register read and write operations are documented in the following section.

In SPI mode, pins SO, SI, SCK and SEL are the respective data input, output, serial clock and chip select signals. Register read and write operations are documented in the following section.

## MACROVISION™ Copy Protection

When the MC44722 is enabled this features in **NTSC mode**, the Luma and Chroma signals are modified according to the MACROVISION™ copy protection process for Pay Per View (PPV) applications revision 7.01 dated Sep 6th , 1996.
But this feature is **NOT supported in PAL mode**, so please do **NOT** use this features in PAL mode.

Enabling and control is through the serial control bus.

No parts will be sent to the customer until the customer provides MOTOROLA with written confirmation of a license, non-disclosure or waiver from MACROVISION™.

If your customer does NOT use this features, please recommend to use the MC44723 no-supported the copy-guard features.

**Fig 14-a : I2C-BUS Interface Write operation Timing**

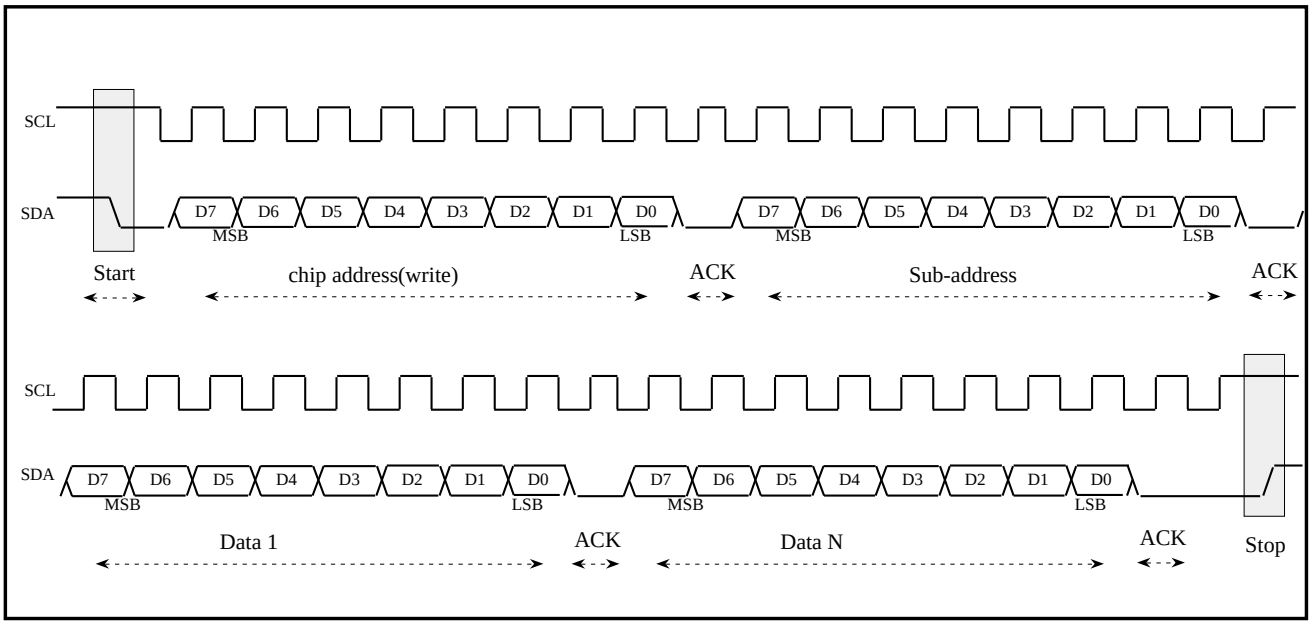



**Fig 14-b : I2C-BUS Interface Read operation Timing**

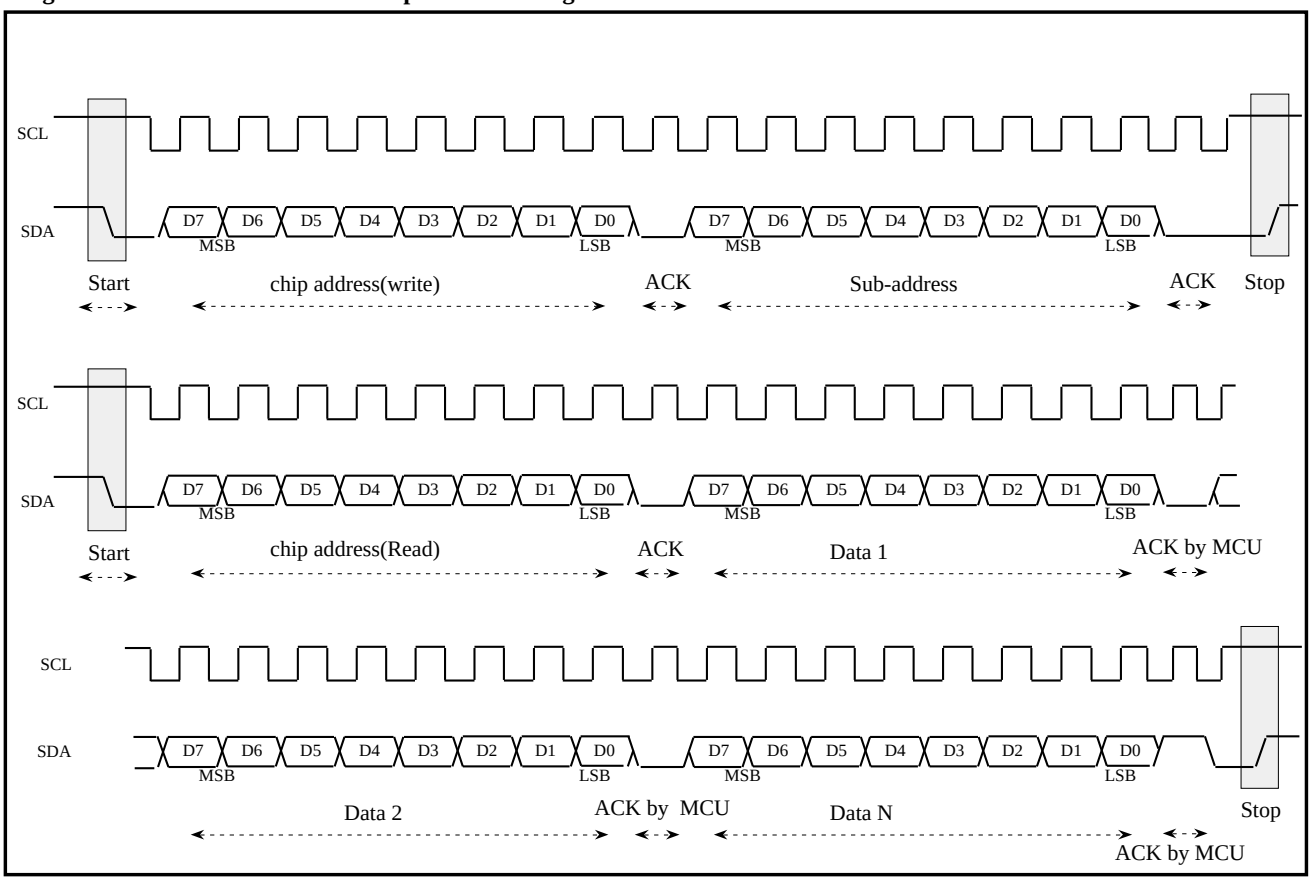


**Fig 15-a : SPI-BUS Interface Write operation Timing**

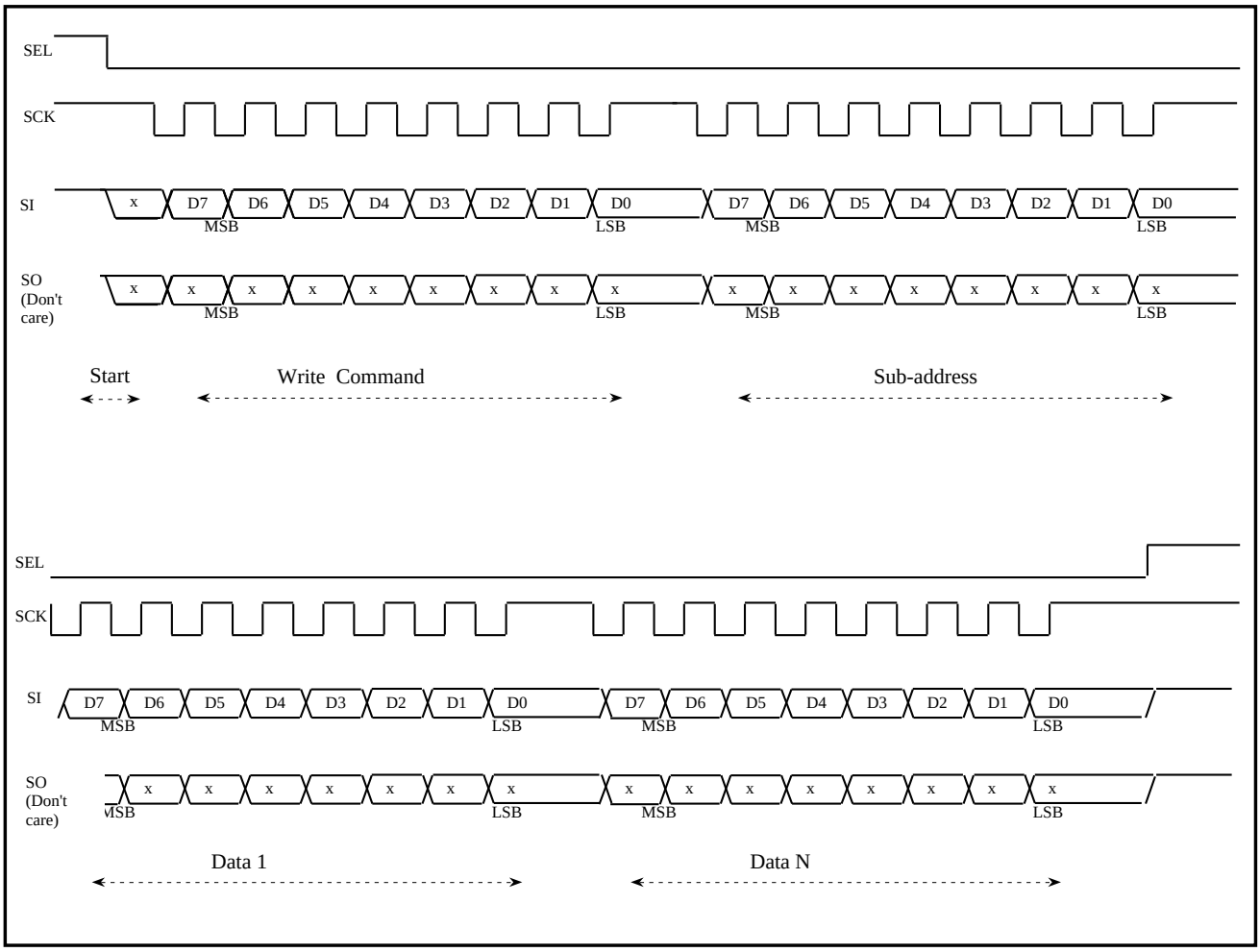
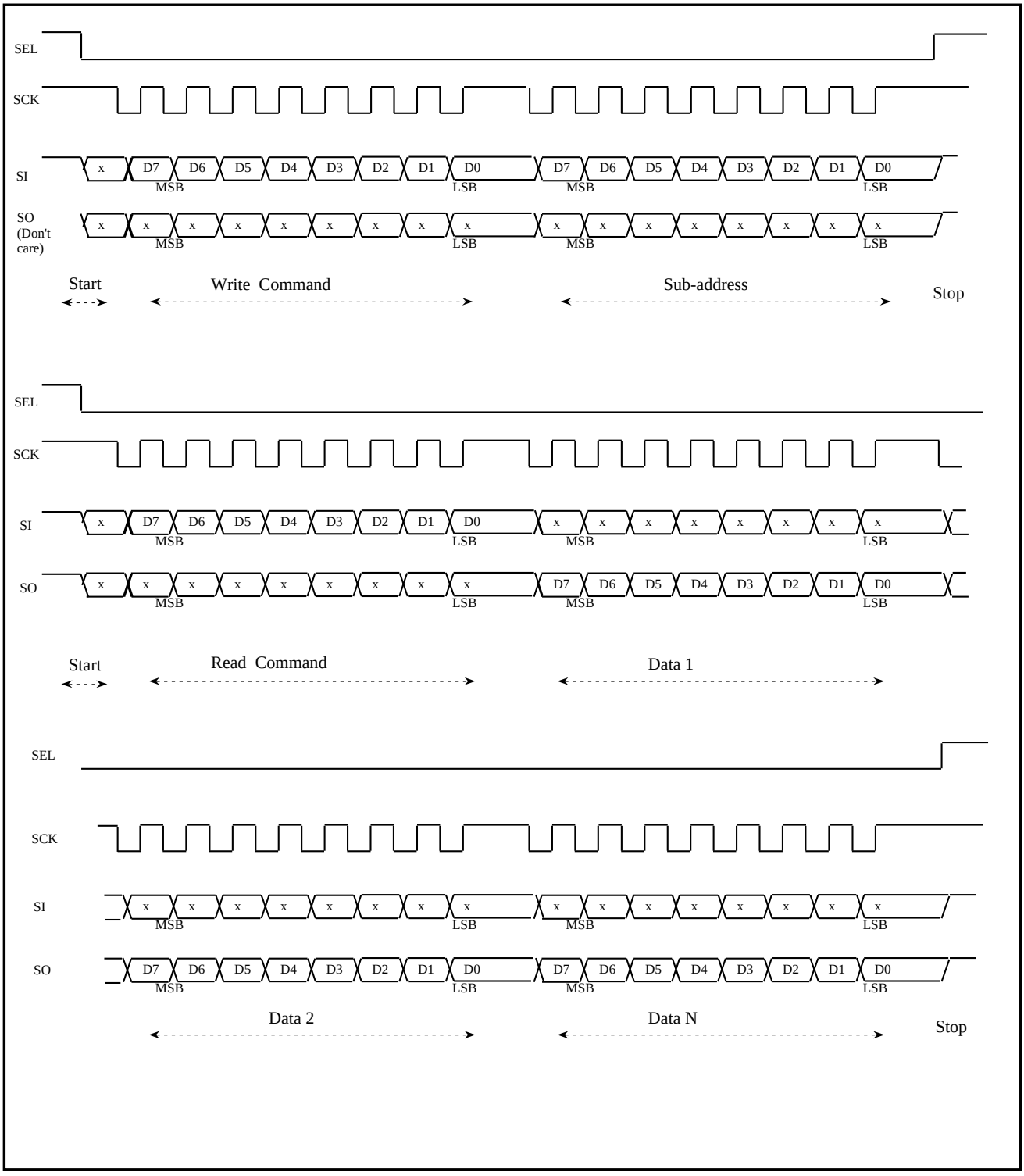


**Fig 15-b : SPI-BUS Interface Read operation Timing**



## *[Specifications]*

*Maximum Ratings*

| | | | |
|---|---|---|---|
| DC Supply Voltage | Vdd | -0.5 ~ +7.0 | V |
| Input Voltage, All Inputs | Vin | -1.5 ~ Vdd+1.5 | V |
| Output Voltage, All Outputs | Vout | -0.5 ~ Vdd+1.5 | V |
| DC Output Current, per Pin | Iout | 25 | mA |
| Power Dissipation | Pd | 750 | mW |
| Storage Temperature | Tstg | -65 ~ +150 | Å é |

*Electrical Characteristics*

| Characteristic | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Power Supply Voltage(Analog Blocks)<br>DAVDD | AVDD | 3.1<br>4.75 | 3.3<br>5.0 | 3.5<br>5.25 | V |
| Power Supply Voltage(Digital Blocks)<br>DVDD | DVDD | 3.1 | 3.3 | 3.5 | V |
| Supply Current(Analog Blocks) | AIcc | - | 30 | - | mA |
| Supply Current(Digital Blocks) | DIcc | - | 170 | - | mA |
| Operating Temperature | Ta | 0 | - | 70 | Å é |

*DAC Blocks Characteristics(Power Supply 3.3V,Ta=25Å é Å }3Å é )*

| Characteristics | Symbol | Min | Typ | Max | Unit | Other |
|---|---|---|---|---|---|---|
| Resolution | - | - | - | 10 | Bit | |
| Integral Non-Linearity | INL | - | - | Å }4.0 | LSB | Vref = 1.1V |
| Differential Non-Linearity | DNL | - | - | Å }2.0 | LSB | Vref = 1.1V |
| Analog Output Voltage | Vyo | 0.85 | 1.00 | 1.15 | Vp-p | Vref = 1.5V |
| Full Scale Output Voltage | Vyfs | 0.85 | 1.00 | 1.15 | V | |
| Zero Scale Output Voltage | Vyzs | - | 0.0 | 0.1 | V | |
| External Load Resistance | RL | 75 | 120 | - | É ∂ | |

*DAC Blocks Characteristics(Power Supply 5.0V,Ta=25Å é Å }3Å é )*

| Characteristics | Symbol | Min | Typ | Max | Unit | Other |
|---|---|---|---|---|---|---|
| Resolution | - | - | - | 10 | Bit | |
| Integral Non-Linearity | INL | - | - | Å }4.0 | LSB | Vref = 1.5V |
| Differential Non-Linearity | DNL | - | - | Å }2.0 | LSB | Vref = 1.5V |
| Analog Output Voltage | Vyo | - | 1.5 | 2.0 | Vp-p | Vref = 2V |
| Full Scale Output Voltage | Vyfs | - | 1.5 | 2.0 | V | Vref = 2V |
| Zero Scale Output Voltage | Vyzs | - | 0.0 | 0.1 | V | |
| External Load Resistance | RL | 75 | 240 | - | É ∂ | |

## *[Specifications]*

*Clock Blocks Characteristics*

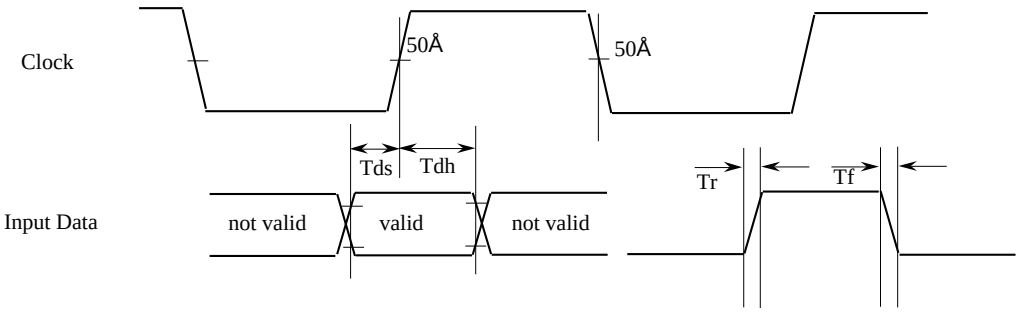
| Characteristic | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Clock Rate | fc | - | 27.0 | - | MHz |
| Clock Duty Cycle | Dty | 40 | 50 | 60 | Å ì |

*Digital Blocks Electrical Characteristics(Power Supply 3.3V,Ta=25Å é Å }3Å é )*

| Characteristics | | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Input Voltage | HIGH | ViH | 2.0 | - | - | V |
| | LOW | ViL | - | - | 0.8 | V |
| Output Voltage | HIGH | VoH | 2.4 | - | - | V |
| (2.0mA) | LOW | VoL | - | - | 0.5 | V |
| Input Leakage Current | | Iin | - | Å }2.5 | - | É A |
| Hi-Z Leakage Current | | Ioz | - | Å }20 | - | É A |
| Input Capacitance | | Cin | - | - | 20 | pF |
| Load Capacitance | | $C_L$ | - | - | 20 | pF |
| Data Setup Time | | Tds | 4 | - | - | nS |
| Data Hold Time | | Tdh | 5 | - | - | nS |
| Input Rise Time | | Tr | - | - | 5 | nS |
| Input Fall Time | | Tf | - | - | 5 | nS |
| Data delay | | Td | - | - | 27 | nS |

*IIC/SPI-BUS Blocks Characteristics(Power Supply 3.3V,Ta=25Å é Å }3Å é )*

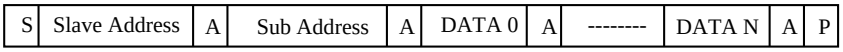
| Characteristics | Symbol Å @Min | | | Typ | Max | Uni |
|---|---|---|---|---|---|---|
| Input Voltage LOW | $V_{ILM}$ | - | - | 0.8 | V | |
| Input Voltage High | $V_{IHM}$ | 2.3 | - | - | V | |
| Input Current | $V_{IM}$ | - | - | Å }10 | É A | |
| SDA Output Voltage ($I_{OM}$=3mA) | $V_{OM}$ | - | - | 0.4 | V | |
| Output Current (during acknowledge) | $I_{OM}$ | 3 | - | - | mA | |



## *[I2C-BUS Slave Address 42(hex)/43(hex) or 1C(hex)/1D(hex)]*

### <I2C-Bus Format>

WRITE MODE

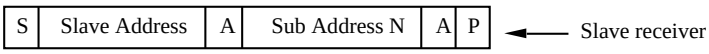



42(hex) or 1C(hex)

if more than 1byte DATA is transmitted,
then auto-increment of the Sub Address is performed

| | |
|---|---|
| S | Start condition |
| Slave Address | 42(hex) or 1C(hex) |
| A | Acknowledge, generated by the slave |
| Sub Address | Sub address byte |
| DATA 0 | First data byte |
| DATA N | continued data byte(Sub Address is auto increment) |
| P | Stop condition |

READ MODE




42(hex) or 1C(hex)

then


43(hex) or 1D(hex)

| | |
|---|---|
| S | Start condition |
| Slave Address | Slave receiver is act transmitter is ad |
| A | Acknowledge, generated by the slave |
| Sub Address N | Sub Address byte |
| DATA N | DATA byte of Register N |
| DATA N + 1 | DATA byte of Register N + 1 (address auto-increment) |
| AM | Acknowledge, generated by the micro controller |
| P | Stop condition (When Last AM must be '1' ) |

## *[SPI-BUS]*

### <SPI-Bus Format>

WRITE MODE

| S | Write Command | Sub Address | DATA 0 | -------- | DATA N | P |
|---|---|---|---|---|---|---|

42(hex) or 1C(hex)

if more than 1byte DATA is transmitted,
then auto-increment of the Sub Address is performed

| | |
|---|---|
| S | Chip select on ( Hi to Lo) |
| Write Command | 42(hex) or 1C(hex) |
| Sub Address | Sub address byte |
| DATA 0 | First data byte |
| DATA N | continued data byte(Sub Address is auto increment) |
| P | Chip select off (Lo to Hi) |

READ MODE

| S | Write Command | Sub Address N | P |
|---|---|---|---|

← Slave receiver

42(hex) or 1C(hex)

then

| S | Read Command | DATA N | DATA N + 1 | --------- | P |
|---|---|---|---|---|---|

← Slave transmitter

43(hex) or 1D(hex)

| | |
|---|---|
| S | Chip select on (Hi to Lo) |
| Sub Address N | Sub Address byte set |
| Read Command | 43(hex) or 1D(hex) |
| DATA N | DATA byte of Register N |
| DATA N + 1 | DATA byte of Register N + 1 (address auto-increment) |
| P | Chip select off (Lo to Hi) |

## *[Register Mapping and Description]*

Sub-address 70 : Variable I/O Switch (write/read)

| | MSB | | | | | | | LSB |
|---|---|---|---|---|---|---|---|---|
| Register 70 | bs-off | self-SW | color bar select | VBLK SW | EXTsync SW | F/Vsync SW | M/S mode1 | M/S mode0 |

default : 0000_0001(bin)

bs - off : color burst control switch On/Off
- 0 : color burst ON (default)
- 1 : color burst OFF

self - SW : internal self H/V counter reset switch On / Off
- 0 : self counter reset OFF (default)
- 1 : self counter reset ON

Note : this mode is ONLY valid at when 70h[1: 0] is "10(bin)" or "11(bin)".

color bar select : color bar select

| | Luma | Chroma |
|---|---|---|
| 0 : color bar | 100% | 100% |
| 1 : color bar | 100% | 75% |

VBLK SW : Vertical Blanking Mask Enabale switch On-Off
- 0 : reject VBI information data in vertical blanking period (default)
- 1 : through VBI information data in vertical blanking period

EXTsync SW : Composite sync/Flame sync output switch
- 0 : Frame sync output (default)
- 1 : compsite sync output

F/Vsync SW : Flame sync /Vertical sync output switch
- 0 : Vertical sync output (default)
- 1 : Frame sync output

M/S sync mode1 : Master or Slave sync mode
M/S sync mode0
- 00 : 656 slave or H/V master mode
- 01 : 656 slave mode(no H/Vsync output) (defalt)
- 10 : Fsync/Hsync slave mode
- 11 : Vsync/Hsync slave mode

Sub-address 71 : Sync control (write/read)

| | MSB | | | | | | | LSB |
|---|---|---|---|---|---|---|---|---|
| Register 71 | non-inter | VBI SW | h-polarity | v-polarity | f-polarity | h- delay2 | h-delay1 | h-delay0 |

default : 0000_0100(bin)

non-inter : non-interlaced mode select
- 0 : interlace mode (default)
- 1 : non-interlace mode

VBI SW : vertical blanking information signal input control switch on EXT pin
- 0 : VBI input Off (default)
- 1 : VBI input On

h-polarity : polarity of Hsync
- 0 : negative (default)
- 1 : positive

v-polarity : polarity of Vsync
- 0 : negative (default)
- 1 : positive

f-polarity : polarity of Fsync
- 0 : field1 (odd) = low level (default)
- 1 : field1 (odd) = high level

h-delay2
h-delay1
h-delay0 : delay on Hsync with referance to DVIN data in Master mode
- 000: + 4 clock delay
- 001: + 3 clock delay
- 010: + 2 clock delay
- 011: + 1 clock delay
- 100: + 0 clock delay
- 101: - 1 clock delay
- 110: - 2 clock delay
- 111: - 3 clock delay

Note : this h-delay can be also related with 7A[7:0] register and can delay totally +2023 clock delay in H/V or H/Fsynnc slave mode.

Sub-address 72 : PAL/NTSC setup (write / read)

| | MSB | | | | | | | LSB |
|---|---|---|---|---|---|---|---|---|
| Register 72 | phase-set | TEST | EXT I/O SW | color bar | setup75 | 625/525 | PAL/ NTSC2 | PAL/ NTSC1 |

default : 0000_1000(bin) NTSC (If "PAL/NTSC" pin is LOW level)
0000_0101(bin) PAL

phase-set : color sub-currier phase syncronization
0 : free running (default)
1 : 1 phase reset/8 field and 1 phase reset/4 flam

TSET : for test, should be "0"

EXT I/O SW : Input/Output switch on EXT pin
0 : VBI input(default)
1 : Csync or Flame sync output

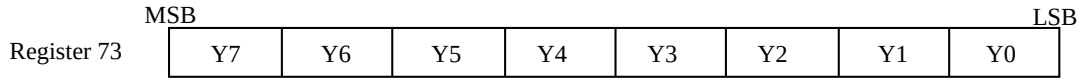
color bar : internal color bar genarator control
0 : nomal operation (default)
1 : color bar genarator On
(need to set color bar mode on sub-address 70[5]. )

setup75 : Setup level for Luminance
0 : setup level for luminunce = 0IRE
1 : setup level for luminunce = 7.5IRE

625/525 : control line mode
0 : 525 lines / 60 Hz mode
1 : 625 lines / 50 Hz mode

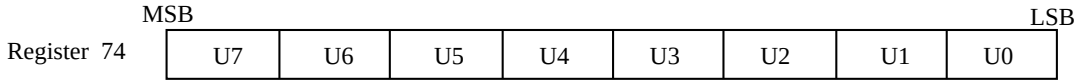
PAL/NTSC2 : subcarrier control
PAL/NTSC1
00 : NTSC(M)
01 : PAL (BDGHI)
10 : PAL (M)
11 : PAL (N)

Sub-address 73: Vertical Blanking Information Luma (Y) Level (write only)




default : 1000_0000(bin)

Sub-address 74: Vertical Blanking Information Chroma (U) Level (write only)




default : 79(dec) (NTSC)
157(dec) (PAL)

Sub-address 75: Vertical Blanking Information Chroma (V) Level (write only)


default : 128(dec) (NTSC)
107(dec) (PAL)

Sub-address 76 : signal control 1(write only)

| | MSB | | | | | | | LSB |
|---|---|---|---|---|---|---|---|---|
| Register 76 | Cr | Cb | Luma | CVBS dac | C dac | Y dac | dac sw1 | dac sw0 |

default : 0000_0000(bin)

Cr : Cr/Cb signal control
Cb
0 : Cr, Cb On (default)
1 : chrominance Off

Luma : luminance control
0 : luminance On (default)
1 : luminance Off

CVBSdac : D/A converter output On-Off control
Cdac
Ydac
0 : CVBS/CbDAC, C/CrDAC, YDAC output On (default)
1 : CVBS/CbDAC, C/CrDAC, YDAC output Off

dac sw1 : 1~9-pin's D/A converter output signal control
dac sw0
10 : Y/Cr/Cb output On
00 : Y/C/CVBS output On

Sub-address 77 : signal control 2 (write only )

| | MSB | | | | | | | LSB |
|---|---|---|---|---|---|---|---|---|
| Register 77 | - | - | - | - | - | - | dac sw4 | dac sw3 |

default : 0000_0001(bin)

dac sw4 : D/A converter output signal control
dac sw3
10 : Y/Cr/Cb output On
00 : Y/C/CVBS output On

Sub-address 78~79 : Sub-carrier phase control (write only)

| | MSB | | | | | | | LSB |
|---|---|---|---|---|---|---|---|---|
| Register 78 | sc-ph9 | sc-ph8 | sc-ph7 | sc-ph6 | sc-ph5 | sc-ph4 | sc-ph3 | sc-ph2 |

default : 0000_0000(bin)

| | MSB | | | | | | | LSB |
|---|---|---|---|---|---|---|---|---|
| Register 79 | - | - | - | - | - | - | sc-ph1 | sc-ph0 |

default : 0000_0000(bin)

sc-ph9 : sub-currier phase control
sc-ph8 0000_0000 : sub-currier phase 0 degree (default)
sc-ph7 to
sc-ph6 1111_1111 : sub-currier phase 359 degree
sc-ph5
sc-ph4
sc-ph3
sc-ph2
sc-ph1
sc-ph0

Sub-address 7A : Hsync delay control (write only)

| | MSB | | | | | | | LSB |
|---|---|---|---|---|---|---|---|---|
| Register 7A | H-dela10 | H-delay9 | H-delay8 | H-delay7 | H-delay6 | H-delay5 | H-delay4 | H-delay3 |

default : 0000_0000(bin)

h-delay10 : delay on Hsync with reference to DVIN data
h-delay9 0000_0000_000 : Hsync delay 0 delay
h-delay8 to
h-delay7 1111_1111_000 : Hsync delay +255 delay
h-delay6
h-delay5
h-delay4
h-delay3

Note : this h-delay can be also related with 71[3:0] register and can delay totally +2023 delay(1111_1111_111) in H/V or H/ Fsync slave mode.

Sub-address 7B : Digital Video Input Select Control (write only)

| | MSB | | | | | | | LSB |
|---|---|---|---|---|---|---|---|---|
| Register 7B | - | - | Cr_tmg 2 | Cr_tmg1 | Cb_tmg 2 | Cb_tmg1 | Y_tmg | 16-bit input mode |

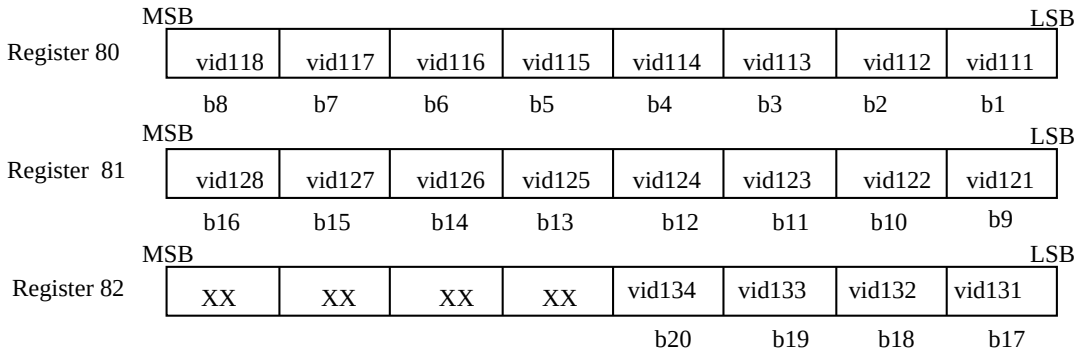
default : 0000_0000(bin)

Cr/Cb_tmg2 : Cr/Cb clock timing delay in 16-bit Digital Input Mode
Cr/Cb_tmg1
00 : Cr clock delay 0 clock (default)
01 : Cr clock delay +1 clock
10 : Cr clock delay +2 clock
11 : Cr clock delay +3 clock

Y_tmg : Y clock timing delay in 16-bit Digital Input Mode
0 : Y clock delay 0 clock (default)
1 : Y clock delay +1 clock

16-bit input mode : 16-bit Multiplexed CbYCrY Digital Video Inout mode
0 : 8-bit CbYCrY Digital Video Input mode (default)
1 : 16-bit CbYCrY Digital Video Input mode

Sub-address 80~82: CGMS characters for Field1(Line20)/Field2(Line283) (write only) NTSC only



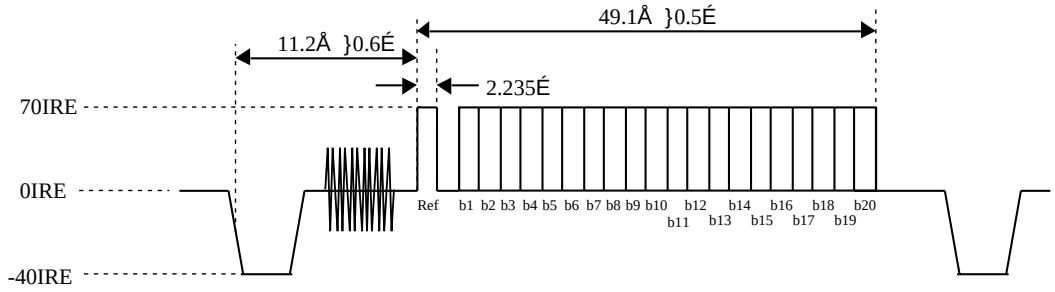




**Fig 16 : CGMS wave form**

Sub-address 83~84 :closed caption characters/extended data for Field1(Line21) (write only)

default 1000_0000

First byte to Encode

| | MSB | | | | | | | LSB |
|---|---|---|---|---|---|---|---|---|
| Register 83 | ccp118 | ccb117 | ccb116 | ccb115 | ccb114 | ccb113 | ccb112 | ccb111 |
| | parity | b7 | b6 | b5 | b4 | b3 | b2 | b1 |

Second byte to Encode

| | MSB | | | | | | | LSB |
|---|---|---|---|---|---|---|---|---|
| Register 84 | ccp128 | ccb127 | ccb126 | ccb125 | ccb124 | ccb123 | ccb122 | ccb121 |
| | parity | b7 | b6 | b5 | b4 | b3 | b2 | b1 |

Sub-address 85~86 :closed cation character/extended data for Field2(Line284)

First byte to Encode

| | MSB | | | | | | | LSB |
|---|---|---|---|---|---|---|---|---|
| Register 85 | ccp218 | ccb217 | ccb216 | ccb215 | ccb214 | ccb213 | ccb212 | ccb211 |
| | parity | b7 | b6 | b5 | b4 | b3 | b2 | b1 |

Second byte to Encode

| | MSB | | | | | | | LSB |
|---|---|---|---|---|---|---|---|---|
| Register 86 | ccp228 | ccb227 | ccb226 | ccb225 | ccb224 | ccb223 | ccb222 | ccb221 |
| | parity | b7 | b6 | b5 | b4 | b3 | b2 | b1 |

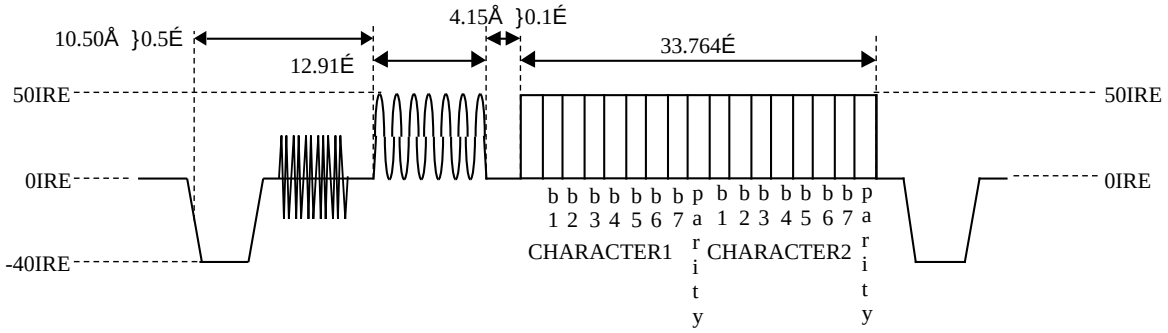



**Fig 17 : Closed caption wave form**

sub-address 83 & 84 and 85 & 86 (previous frame data)
are double-buffered by Flame sync falling edge

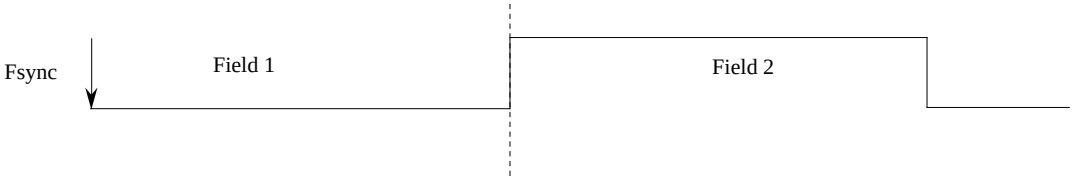



**Fig 18 : Closed caption data update timing**

Sub-address 87 :Closed caption/CGMS

| | MSB | | | | | | | LSB |
|---|---|---|---|---|---|---|---|---|
| Register 87 | - | - | - | - | - | VBI | CC2 | CC1 |

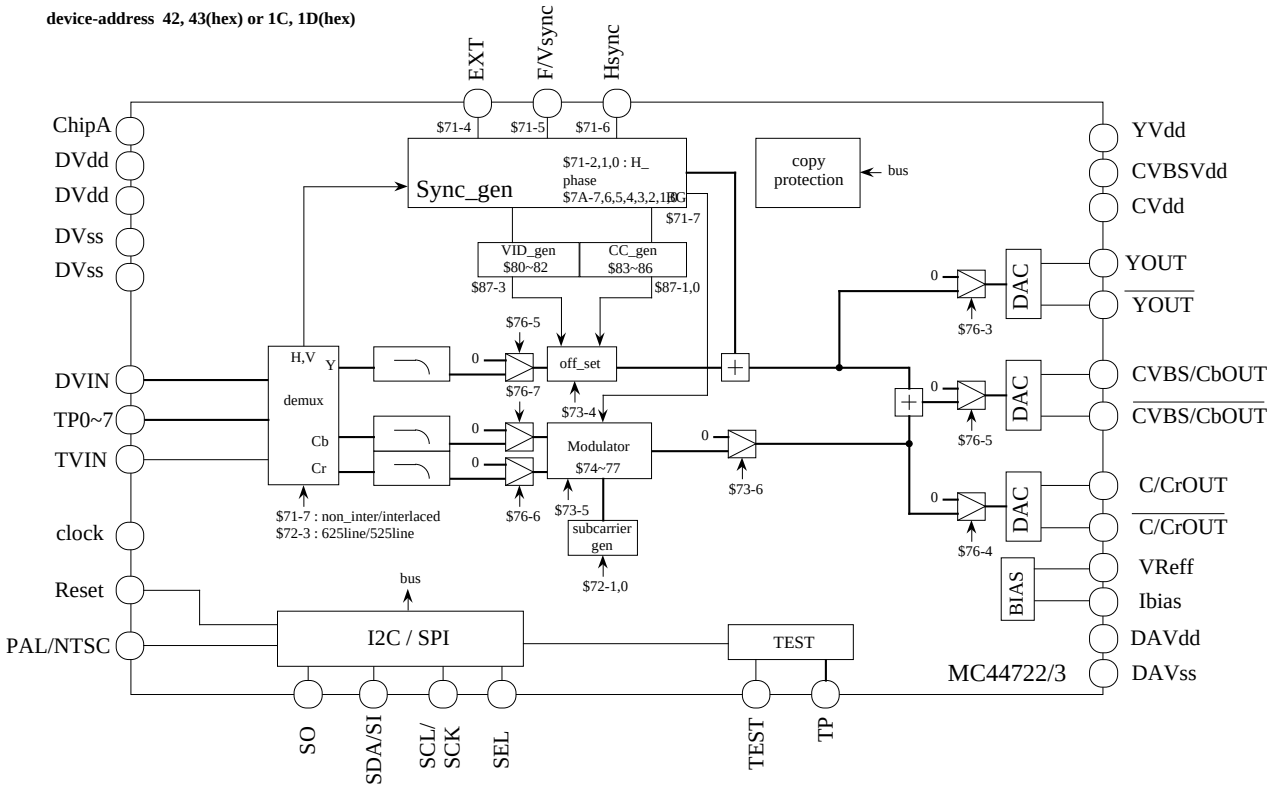
default 000

VBI : CGMS information data insertion On-Off
0 : CGMS information data insertion Off
1 : CGMS information data insertion On

CC2 : closed caption/extended data for field2 encoding On-Off
0 : closed caption/extended data for field2 encoding Off
1 : closed caption/extended data for field2 encoding On

CC1 : closed caption/extended data for field1 encoding
0 : closed caption/extended data for field1 encoding Off
1 : closed caption/extended data for field1 encoding On

**device-address 42, 43(hex) or 1C, 1D(hex)**




%% I2C-BUS Slave Receiver Sub-address map %%

| | | |
|---|---|---|
| 70h:[7] | | burst control (default 0:on) |
| | [6] | self counter reset switch (default 0:off) |
| | [5] | color bar select (defalut 0:Luma 100% Chroma 100%) |
| | [4] | vertical blanking switch(default 0:off) |
| | [3] | EXT pin output mode select (Csync:1, Flame sync:0) |
| | [2] | F/Vsync select(default 0:Vsync) |
| | [1:0] | Master/Slave mode select(default 01:656_slave) |
| 71h:[7] | | interlaced / non-interlaced<br>(default 0:interlaced) |
| | [6] | VBI input control on EXT pin (default 0:off) |
| | [5] | horizontal sync polarity (default 0) |
| | [4] | vertical sync polarity (default 0) |
| | [3] | flame sync polarity (default 0) |
| | [2:0] | hsync delay control (default 100:0 clock delay)<br>(In slave mode can use with 7A[7:0]) |
| 72h:[7] | | sub-currier phase syncronaiation(default 0) |
| | [6] | Test mode (default 0:off) |
| | [5] | EXT I/O switch(defalt 1:cysnc output) |
| | [4] | color bar generate(default 0:off) |
| | [3] | setup level control(default 1:7.5IRE) |
| | [2] | 625lines50Hz/525Lines60Hz<br>(default set PAL/NTSC pin) |
| | [1:0] | PAL/NTSC (default set PAL/NTSC pin)<br>00:NTSC/M<br>01:PAL/BGHL<br>(10:PAL/M) (11:PAL/N) |
| 73h[7:0] | | Y_register(default 80h) |
| 74h[7:0] | | U_register(default 79d:ntsc/157d:PAL) |
| 75h[7:0] | | V_register(default 128d:ntsc/107d:PAL) |
| 76h[7] | | Cr on/off (default 0:on) |
| | [6] | Cb on/off (default 0:on) |
| | [5] | Luma on/off(default 0:on)<br>(default 0: on) |
| | [4] | CVBS/Cb DAC on/off(default 0: on) |
| | [3] | C/Cr DAC on/off(default 0: on) |
| | [2] | C/Cr DAC on/off(default 0: on) |
| | [1] | CBVS/Y/C Y/Cr/Cb output control swith<br>(default 0 : CBVS/Y/C output) |
| | [0] | reserved |
| 77h[7:0] | | n.a |
| 78h[7:0] | | sub-currier phase control(default 00h) |
| 79h[1:0] | | sub-currier phase control(default 00) |
| 79h:[7:2] | | n.a. |
| 7A[7:0] | | hsync-delay control<br>(In slave mode, is valid with 71h[2:] register) |
| 7B[7:6] | | n.a |
| 7B[5:4] | | Cr clock timing delay in 16-bit digital input mode |
| 7B[3:2] | | Cb clock timing delay in 16-bit digital input mode |
| 7B[1] | | Y clock timing delay in 16-bit digital input mode |
| 7B[0] | | 16-bit multiplexed CbYCrY digital input mode<br>(default 0: 8-bit multiplexed CbYCrY mode) |
| 80~82h: | | Video ID characters for field1(line20)/field2(line283) |
| 83h[7:0] | | CC character1(line21) (default 'h80) |
| 84h[7:0] | | CC character2(line21) (default 'h80) |
| 85h[7:0] | | CC character1(line284) (default 'h80) |
| 86h[7:0] | | CC character2(line284) (default 'h80) |
| 87h[7:3] | | n.a. |
| | [2] | CGMS on/off (default 0: off) |
| | [1] | CC closed caption/extended data for field2 encoding<br>(default 0: off) |
| | [0] | CC closed caption/extended data for field1 encoding<br>(default 0: off) |

<<<<<<<< M-BUS Format >>>>>>

** WRITE MODE **

S | Slave_address(W) | A | Sub_address | A | Data0 | A | ... | DataN | A | P

| | |
|---|---|
| S | Start condition |
| Slave_address | 42(hex) or 1C(hex) |
| A | Acknowledge generated by me |
| Sub_address | Sub_address register |
| Data0 | First data |
| DataN | Continued data(address is auto incremented) |
| P | Stop condition |

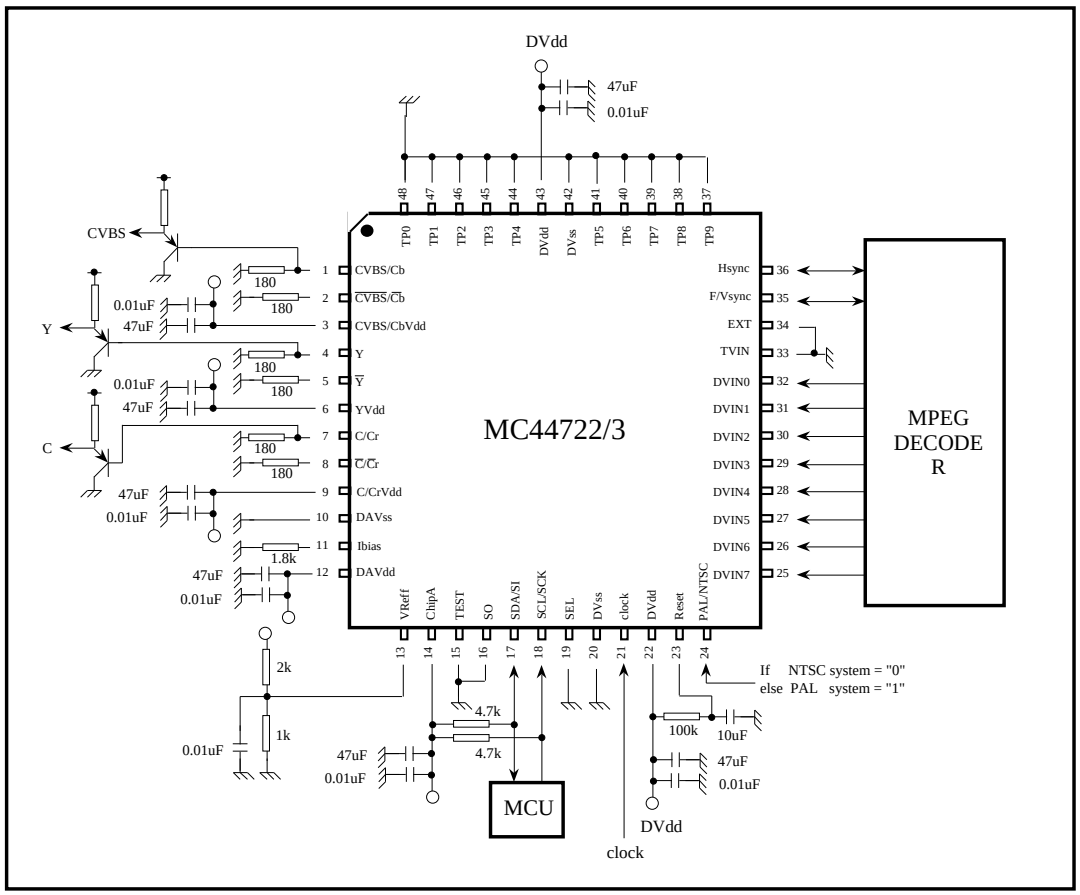
<<<<<<<< SPI-Bus Format >>>>>>

** WRITE MODE **

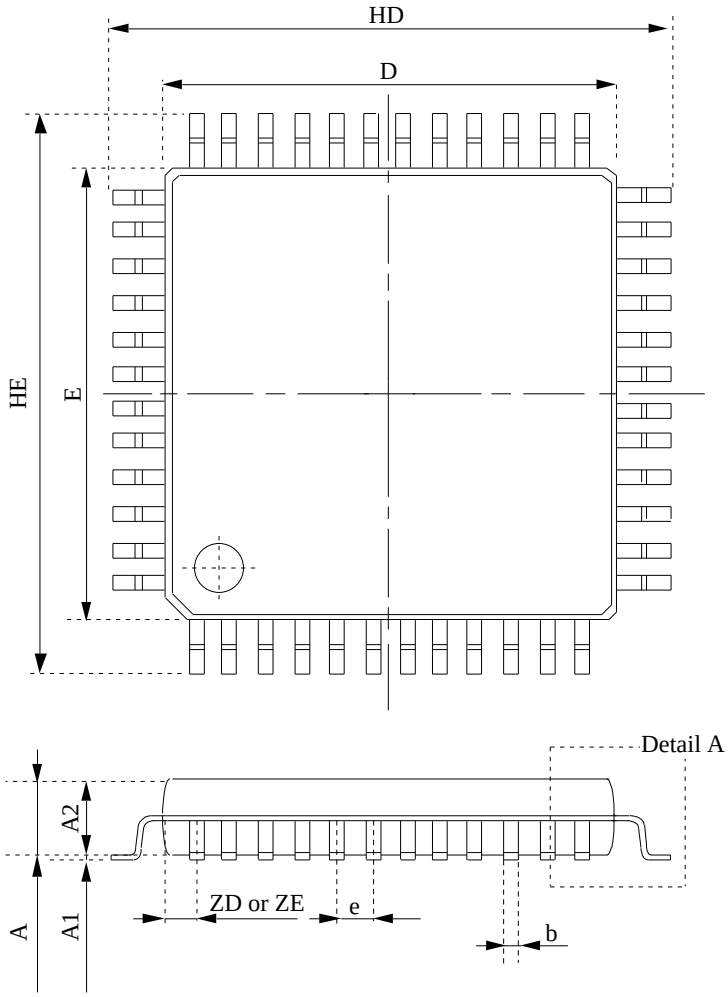
S | Write Command | Sub_address | Data0 | ... | DataN | P

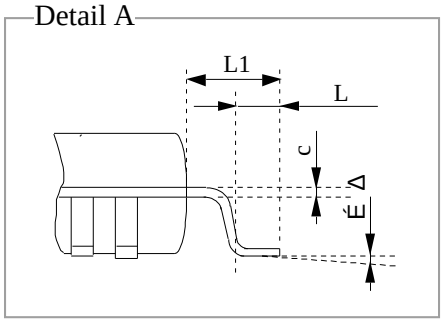
| | |
|---|---|
| S | Chip select on (High to Low) |
| Write Command | 42(hex) or 1C(hex) |
| Sub_address | Sub_address byte |
| Data0 | First data |
| DataN | Continued data byte(address is auto incremented) |
| P | Chip select off (Low to High) |

## *[ Appication Diagram ]*



Package




| | min | max |
|---|---|---|
| A | - | 1.70 |
| A1 | 0.05 | 0.15 |
| A2 | 1.40TYP | |
| b | 0.3 | 0.45 |
| c | 0.10 | 0.20 |
| D | 11.90 | 12.10 |
| E | 11.90 | 12.10 |
| e | 0.80 | |
| HD | 13.80 | 14.20 |
| HE | 13.80 | 14.20 |
| L | 0.30 | 0.70 |
| L1 | 0.80 | 1.20 |
| É | 0 | 10 |
| y | - | 0.10 |
| ZD | 1.60 | |
| ZE | 1.60 | |

unit : mm