Advanced Power Electronics Corp.

AP6920GMT-HF

Dual N-CHANNEL ENHANCEMENT

MODE POWER MOSFET

▼ **Simple Drive Requirement**

▼ **Easy for Synchronous Buck**

   **Converter Application**

▼ **RoHS Compliant & Halogen-Free**
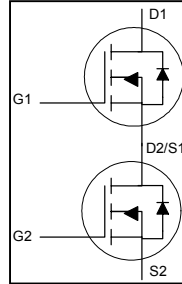
CH-1	BV_{DSS}	30V
	$R_{DS(ON)}$	8.5mΩ
	I_D	48A
CH-2	BV_{DSS}	30V
	$R_{DS(ON)}$	3.8mΩ
	I_D	87A

Description

Advanced Power MOSFETs from APEC provide the designer with the best combination of fast switching, ruggedized device design, low on-resistance and cost-effectiveness.

The control MOSFET (CH-1) and synchronous MOSFET (CH-2) co-package for synchronous buck converters.
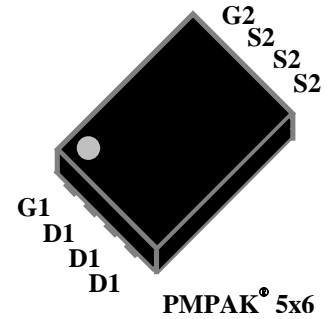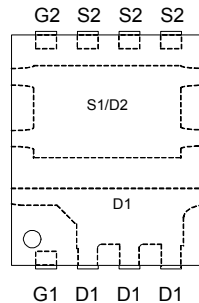
PMPAK® 5x6

Absolute Maximum Ratings

Symbol	Parameter	Rating CH-1	Rating CH-2	Units
V_{DS}	Drain-Source Voltage	30	30	V
V_{GS}	Gate-Source Voltage	$\pm$20	$\pm$12	V
I_D@T_C=25℃	Continuous Drain Current (Chip Limited)	48	87	A
I_D@T_A=25℃	Continuous Drain Current[3]	15	25.7	A
I_D@T_A=70℃	Continuous Drain Current[3]	12	20.5	A
I_{DM}	Pulsed Drain Current[1]	40	60	A
P_D@T_A=25℃	Total Power Dissipation	3.13	3.9	W
T_{STG}	Storage Temperature Range	-55 to 150		℃
T_J	Operating Junction Temperature Range	-55 to 150		℃

Thermal Data

Symbol	Parameter	Rating CH-1	Rating CH-2	Units
Rthj-c	Maximum Thermal Resistance, Junction-case	4	2.8	℃/W
Rthj-a	Maximum Thermal Resistance, Junction-ambient[3]	40	32	℃/W
Rthj-a	Maximum Thermal Resistance, Junction-ambient[4]	70	60	℃/W

CH-1 Electrical Characteristics@T$_j$=25°C(unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
BV$_{DSS}$	Drain-Source Breakdown Voltage	V$_{GS}$=0V, I$_D$=250uA	30	-	-	V
R$_{DS(ON)}$	Static Drain-Source On-Resistance[2]	V$_{GS}$=10V, I$_D$=12A	-	6.5	8.5	mΩ
		V$_{GS}$=4.5V, I$_D$=8A	-	9.3	12	mΩ
V$_{GS(th)}$	Gate Threshold Voltage	V$_{DS}$=V$_{GS}$, I$_D$=250uA	1	1.32	3	V
g$_{fs}$	Forward Transconductance	V$_{DS}$=10V, I$_D$=12A	-	36	-	S
I$_{DSS}$	Drain-Source Leakage Current	V$_{DS}$=24V, V$_{GS}$=0V	-	-	10	uA
I$_{GSS}$	Gate-Source Leakage	V$_{GS}$=±20V, V$_{DS}$=0V	-	-	±100	nA
Q$_g$	Total Gate Charge	I$_D$=12A	-	6.5	10.4	nC
Q$_{gs}$	Gate-Source Charge	V$_{DS}$=15V	-	1.5	-	nC
Q$_{gd}$	Gate-Drain ("Miller") Charge	V$_{GS}$=4.5V	-	3	-	nC
t$_{d(on)}$	Turn-on Delay Time	V$_{DS}$=15V	-	7.5	-	ns
t$_r$	Rise Time	I$_D$=1A	-	5	-	ns
t$_{d(off)}$	Turn-off Delay Time	R$_G$=3.3Ω	-	18	-	ns
t$_f$	Fall Time	V$_{GS}$=10V	-	7	-	ns
C$_{iss}$	Input Capacitance	V$_{GS}$=0V	-	600	960	pF
C$_{oss}$	Output Capacitance	V$_{DS}$=15V	-	220	-	pF
C$_{rss}$	Reverse Transfer Capacitance	f=1.0MHz	-	100	-	pF
R$_g$	Gate Resistance	f=1.0MHz	-	2.7	5.4	Ω

Source-Drain Diode

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
V$_{SD}$	Forward On Voltage[2]	I$_S$=12A, V$_{GS}$=0V	-	-	1.2	V
t$_{rr}$	Reverse Recovery Time	I$_S$=12A, V$_{GS}$=0V,	-	20	-	ns
Q$_{rr}$	Reverse Recovery Charge	dI/dt=100A/μs	-	10	-	nC

CH-2 Electrical Characteristics@T_j=25°C(unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS}=0V, I_D=250uA	30	-	-	V
$R_{DS(ON)}$	Static Drain-Source On-Resistance[2]	V_{GS}=10V, I_D=20A	-	2.9	3.8	mΩ
		V_{GS}=4.5V, I_D=12A	-	4	5.2	mΩ
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}=V_{GS}, I_D=250uA	1	1.5	3	V
g_{fs}	Forward Transconductance	V_{DS}=10V, I_D=20A	-	60	-	S
I_{DSS}	Drain-Source Leakage Current	V_{DS}=24V, V_{GS}=0V	-	-	10	uA
I_{GSS}	Gate-Source Leakage	V_{GS}=±12V, V_{DS}=0V	-	-	±100	nA
Q_g	Total Gate Charge	I_D=20A	-	36	57	nC
Q_{gs}	Gate-Source Charge	V_{DS}=15V	-	9	-	nC
Q_{gd}	Gate-Drain ("Miller") Charge	V_{GS}=4.5V	-	19	-	nC
$t_{d(on)}$	Turn-on Delay Time	V_{DS}=15V	-	14	-	ns
t_r	Rise Time	I_D=1A	-	11	-	ns
$t_{d(off)}$	Turn-off Delay Time	R_G=3.3Ω	-	65	-	ns
t_f	Fall Time	V_{GS}=10V	-	26	-	ns
C_{iss}	Input Capacitance	V_{GS}=0V	-	3800	6080	pF
C_{oss}	Output Capacitance	V_{DS}=15V	-	430	-	pF
C_{rss}	Reverse Transfer Capacitance	f=1.0MHz	-	380	-	pF
R_g	Gate Resistance	f=1.0MHz	-	1.6	3.2	Ω

Source-Drain Diode

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
V_{SD}	Forward On Voltage[2]	I_S=20A, V_{GS}=0V	-	-	1.2	V
t_{rr}	Reverse Recovery Time	I_S=10A, V_{GS}=0V,	-	29	-	ns
Q_{rr}	Reverse Recovery Charge	dI/dt=100A/µs	-	22	-	nC

Notes:

1.Pulse width limited by Max. junction temperature.

2.Pulse test

3.Surface mounted on 1 in^2 copper pad of FR4 board, t ≤10sec.

4.Surface mounted on 1 in^2 copper pad of FR4 board, on steady-state

Channel-1

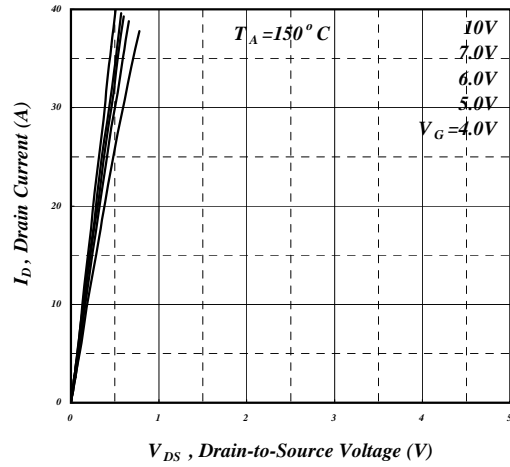Fig 1. Typical Output Characteristics

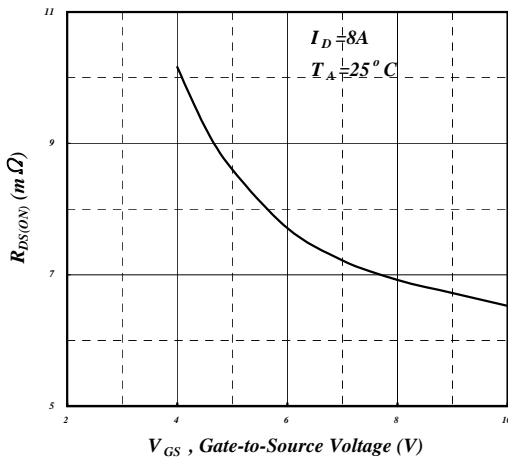Fig 2. Typical Output Characteristics
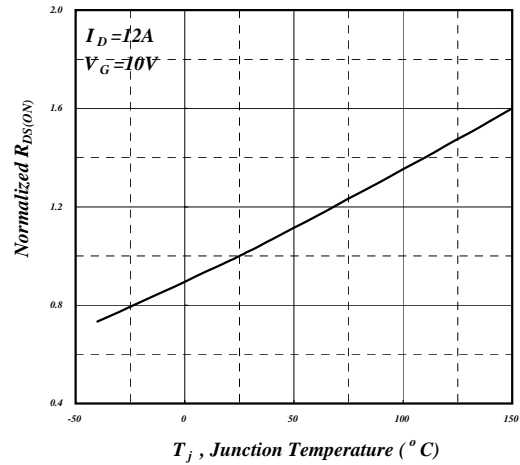

Fig 3. On-Resistance v.s. Gate Voltage

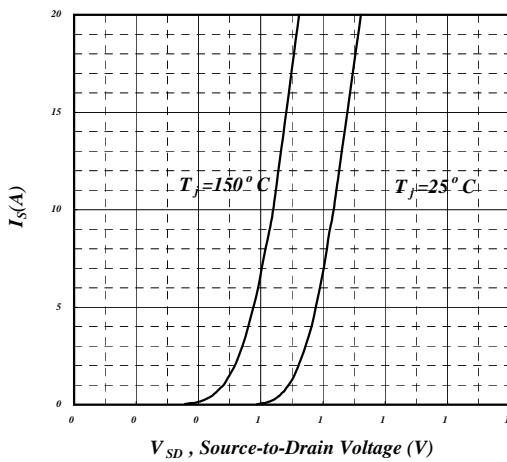Fig 4. Normalized On-Resistance
v.s. Junction Temperature

Fig 5. Forward Characteristic of
Reverse Diode
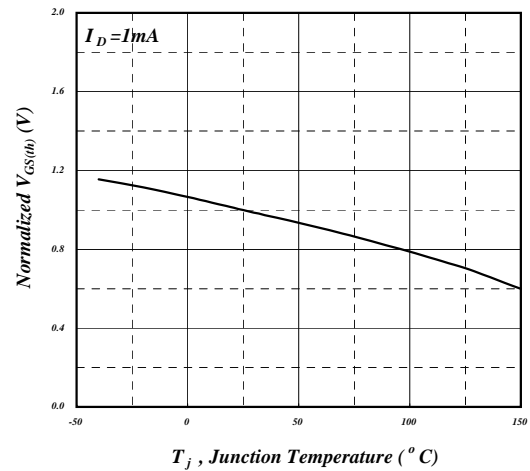

Fig 6. Gate Threshold Voltage v.s.
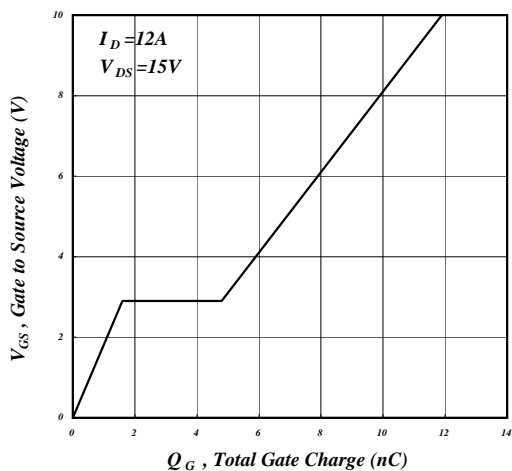Junction Temperature

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Channel-1
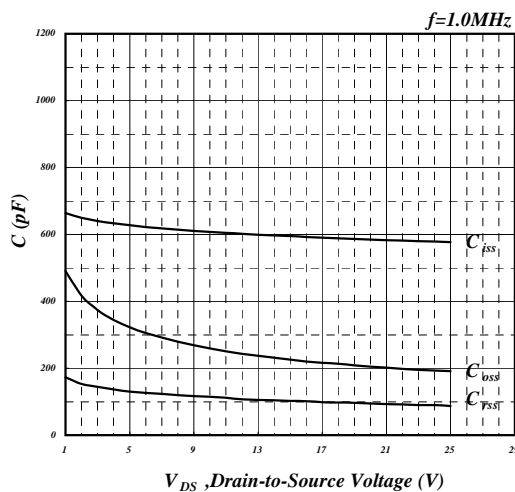

Fig 7. Gate Charge Characteristics
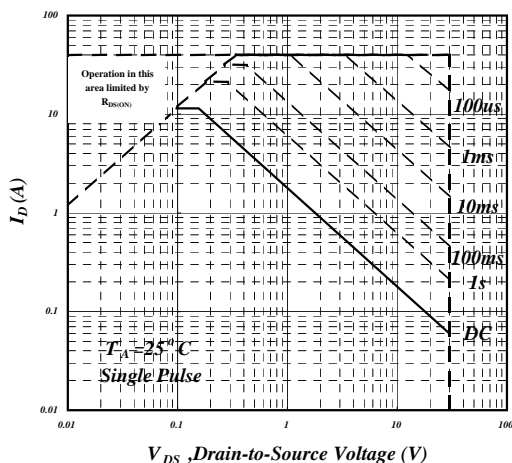

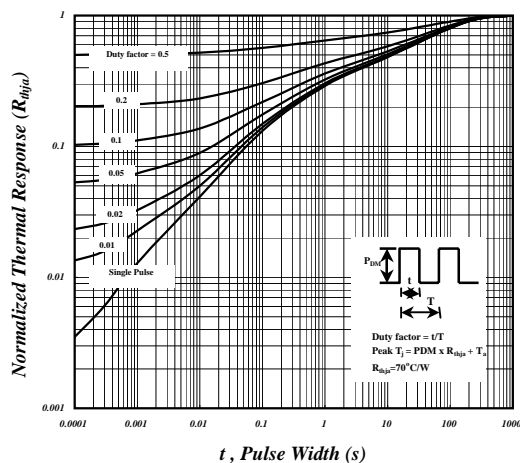Fig 8. Typical Capacitance Characteristics
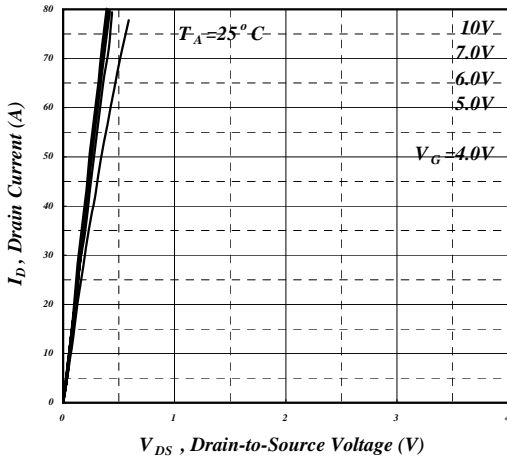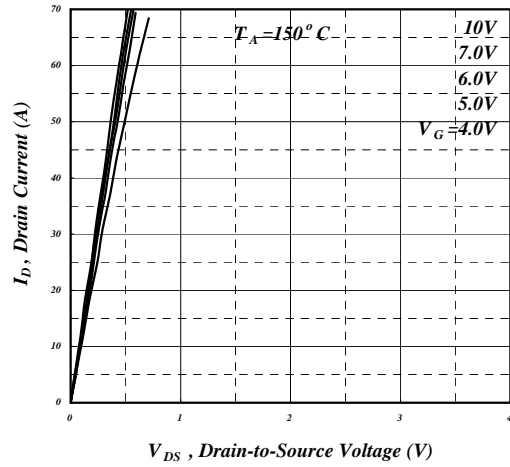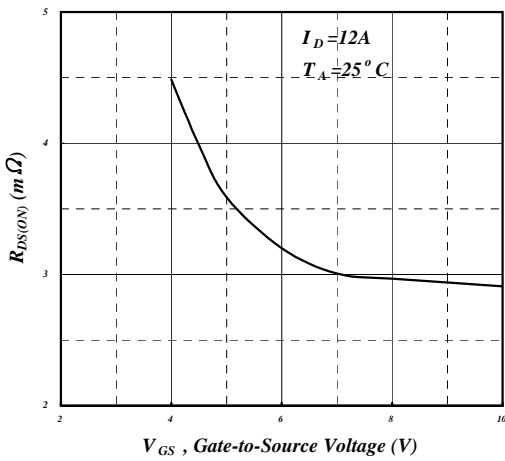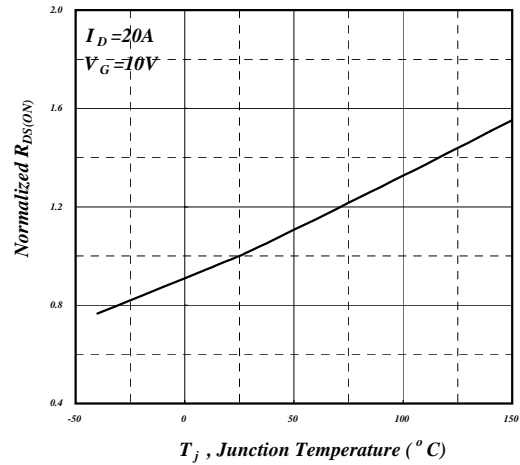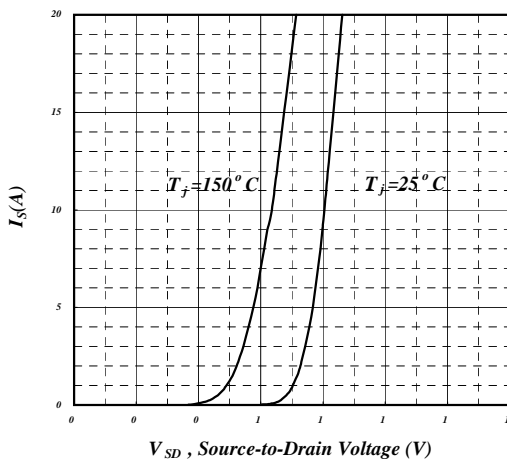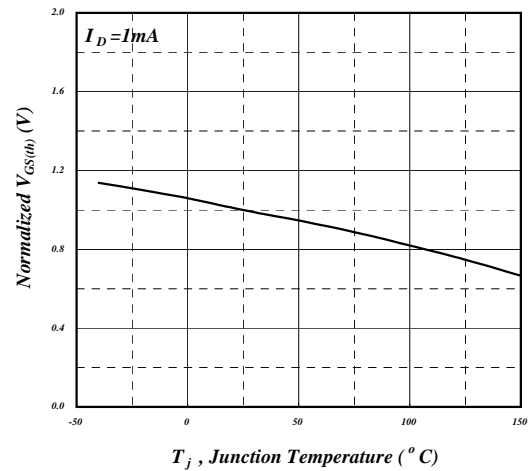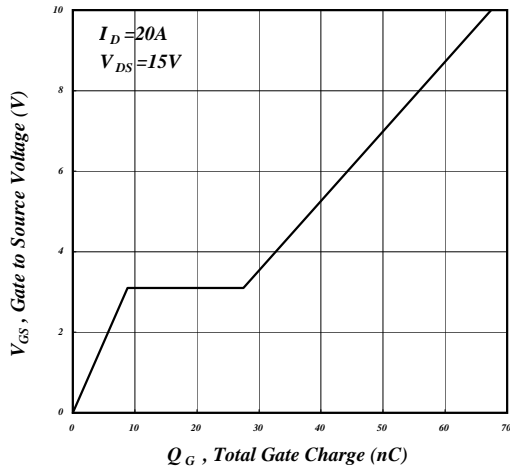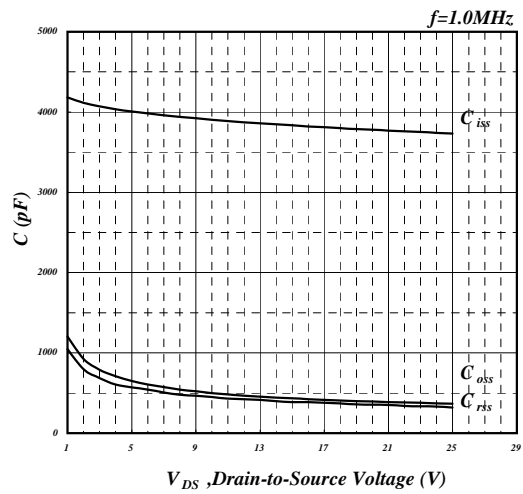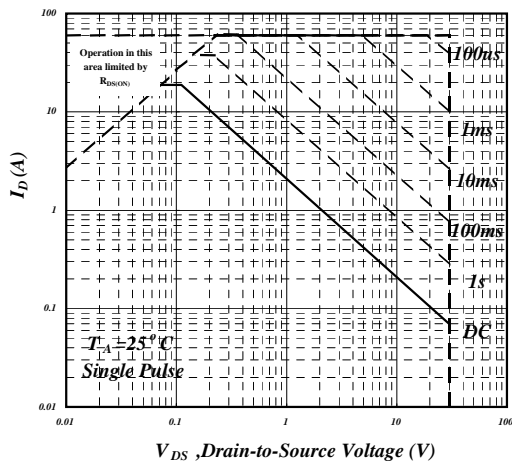
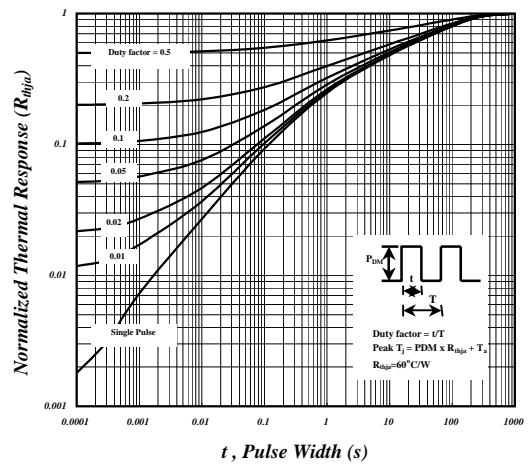

Fig 9. Maximum Safe Operating Area

Fig 10. Effective Transient Thermal Impedance
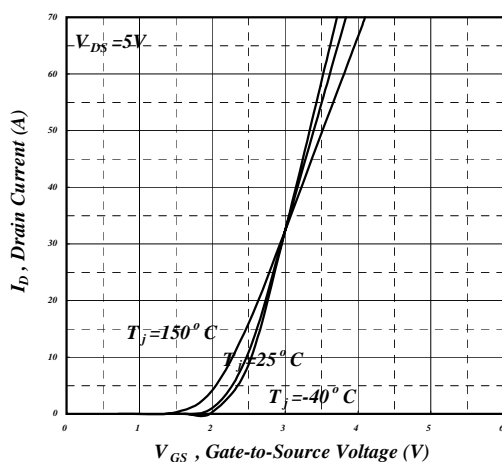
Fig 11. Transfer Characteristics
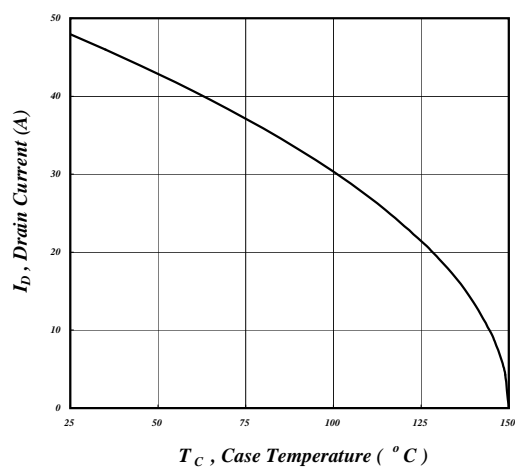
Fig 12. Maximum Continuous Drain Current
v.s. Case Temperature

Channel-2

Fig 1. Typical Output Characteristics

Fig 2. Typical Output Characteristics

Fig 3. On-Resistance v.s. Gate Voltage

Fig 4. Normalized On-Resistance
v.s. Junction Temperature

Fig 5. Forward Characteristic of
Reverse Diode

Fig 6. Gate Threshold Voltage v.s.
Junction Temperature

Channel-2

Fig 7. Gate Charge Characteristics

Fig 8. Typical Capacitance Characteristics

Fig 9. Maximum Safe Operating Area

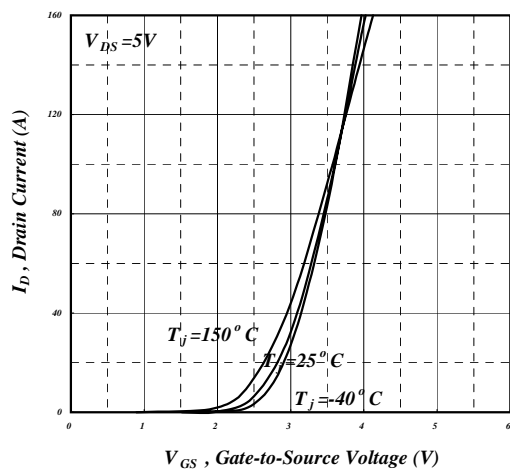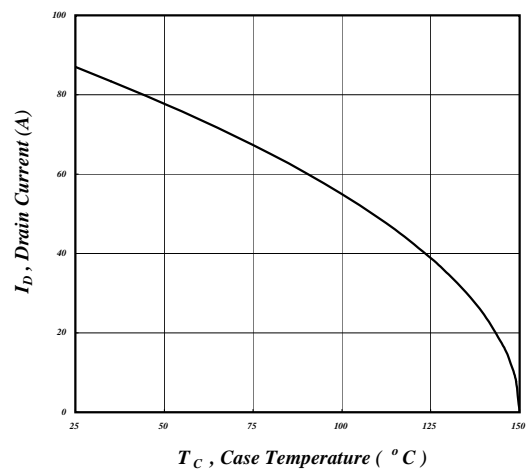**Fig 10. Effective Transient Thermal Impedance**

Fig 11. Transfer Characteristics

**Fig 12. Maximum Continuous Drain Current
v.s. Case Temperature**