Low Parts Compression Amplifier

GB512/LD512 DATA SHEET

FEATURES

- **44 dB typical preamplifier gain**
- **14 dB typical output stage gain**
- **compression function ratio 1:1 to 2:1 to ∞:1**
- **automatic setting of transducer current**
- **operation down to 1.1 VDC**
- **greater than 40 dB volume control range**

STANDARD PACKAGING

- 8 pin MICROPAC
- 8 pin PLID
- 8 pin SLT ®
- Chip (61 x 61 mils)
  Au Bump

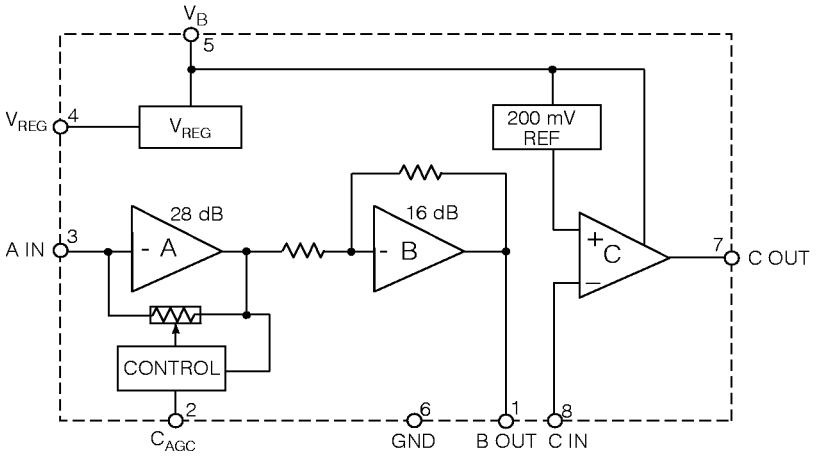
DESCRIPTION

The GB512 and LD512 are 8 pin stand-alone input compression amplifiers requiring minimal external parts. Each consists of a voltage regulator for the electret microphone providing a high power supply rejection ratio (PSRR), a compression stage which has a 2:1 compression ratio, and an auto-biasing, class A, voltage drive output stage.

The auto-bias output stage can drive a variety of impedances ranging from 500 Ω to 5 kΩ without adding any external resistors to set the bias.

The GB512 and LD512 are recommended for low to medium gain/output ITE and ITC type hearing aids.

The GB512 is tested to tighter test limits.



BLOCK DIAGRAM

Revision Date April 1998

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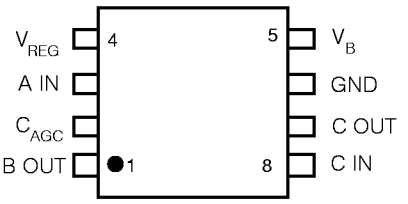
ABSOLUTE MAXIMUM RATINGS

PARAMETER	VALUE/UNITS
Supply Voltage	5 V DC
Power Dissipation	25mW
Operating Temperature Range	-10°C to 40°C
Storage Temperature Range	-20°C to 70°C

CAUTION
CLASS 1 ESD SENSITIVITY

PIN CONNECTION

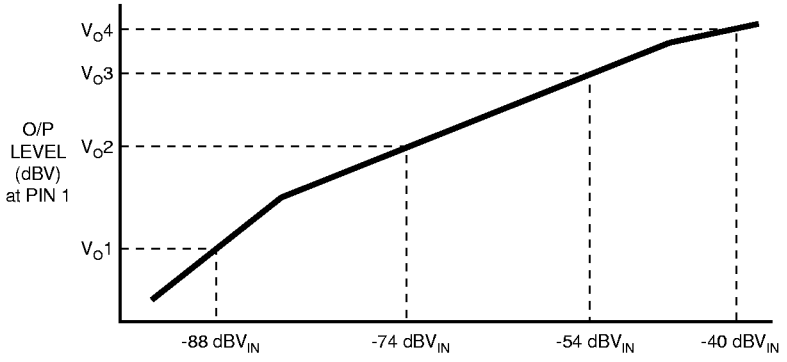


ELECTRICAL CHARACTERISTICS

Conditions : Temperature 25°C, Frequency 1 kHz, Supply Voltage 1.3 VDC.

			GB512			LD512			
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
Amplifier Current	I_{AMP}		110	200	290	110	200	290	µA
Regulator Voltage	V_{REG}		0.88	0.93	0.98	0.88	0.93	0.98	V_{DC}
Output Level	V_{O1}	V_{IN} = -88 dBV	-47	-44	-41	-48	-44	-40	dBV
Output Level	V_{O2}	V_{IN} = -74 dBV	V_{O1} + 7	V_{O1} + 9	V_{O1} + 11	-	-	-	dB
Output Level	V_{O3}	V_{IN} = -54 dBV	V_{O2} + 8	V_{O2}+10	V_{O2}+12	V_{O2} + 7	V_{O2}+10	V_{O2}+13	dB
Output Level	V_{O4}	V_{IN} = -40 dBV	-23	-20	-18	-23.5	-20	-17.5	dBV
Input Referred Noise	IRN	NFB 0.2-10kHz at 12dB/oct	-	1	3	-	1	3	μV_{RMS}
Total Harmonic Distortion	THD	V_{IN} = -54 dBV	-	2	4	-	2	4	%
Receiver Bias Voltage	V_{BIAS}	Note 3	100	200	300	160	200	240	mVDC
Current Sinking Capability	I_{SINK}	Note 4	3	8	-	3	8	-	mA
Release Time Factor	T_{REL}		-	100	-	-	100	-	ms/µF
Attack Time Factor	T_{ATT}		-	5	-	-	5	-	ms/µF

All parameters and switches remain as shown in the Test Circuit unless stated in CONDITIONS column.
V_{PX} - actual voltage measured on the pin at given condition (X is pin number).



Notes:

1. V_O and Distortion measurements are taken at pin 1.
2. Output stage gain = 20 log (R_F / R_S). A gain of 14 dB is recommended for optimal stability. Stability is dependent upon the ratio of the receiver impedance (Z_L) and the battery impedance to R_F & R_S. (R_F / R_S) < (Z_L/R_B)
3. V_{BIAS} = V_{P5} - V_{P7}
4. Measured at pin 7

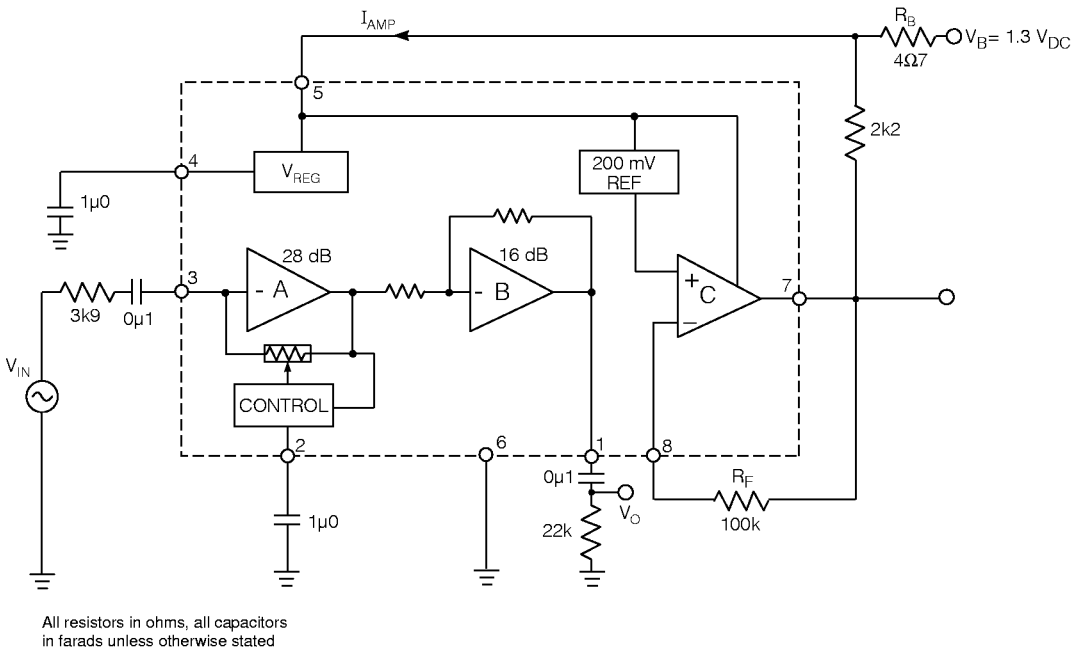


Fig. 1 Test Circuit

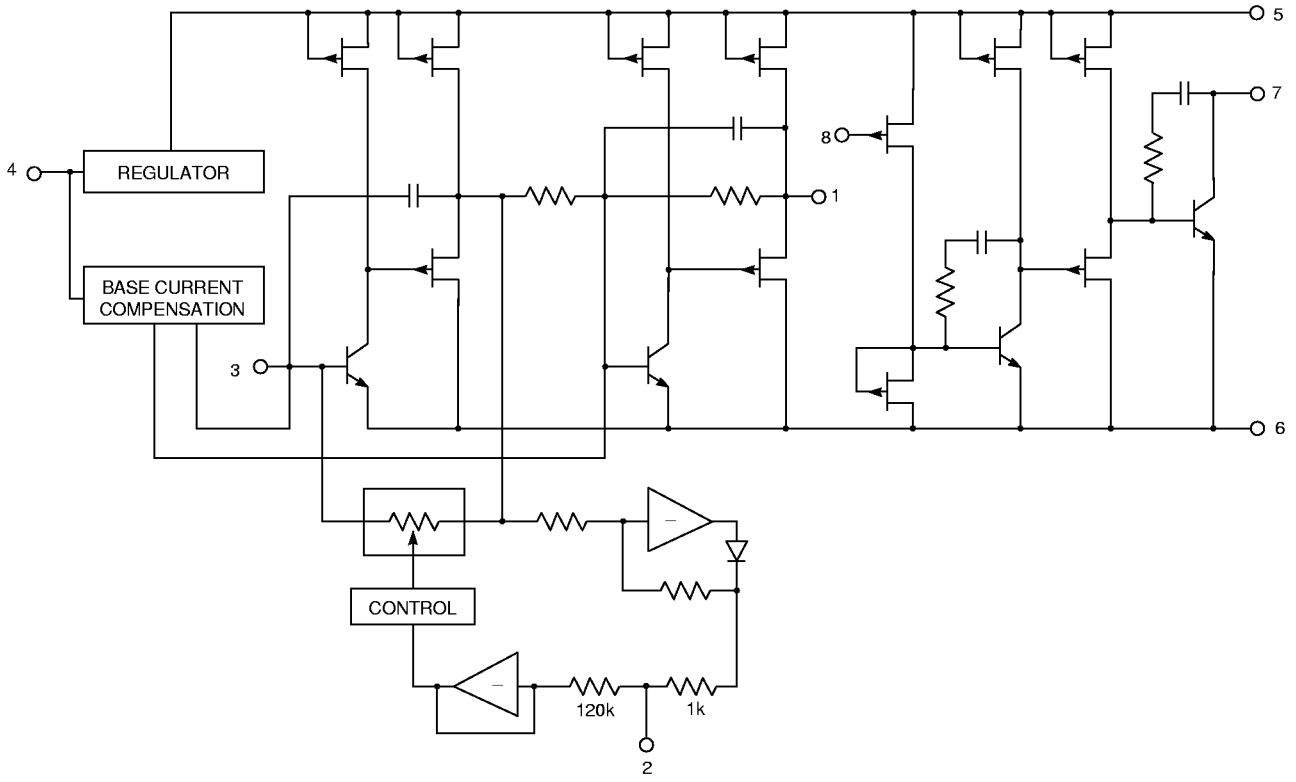


Fig. 2 Functional Schematic

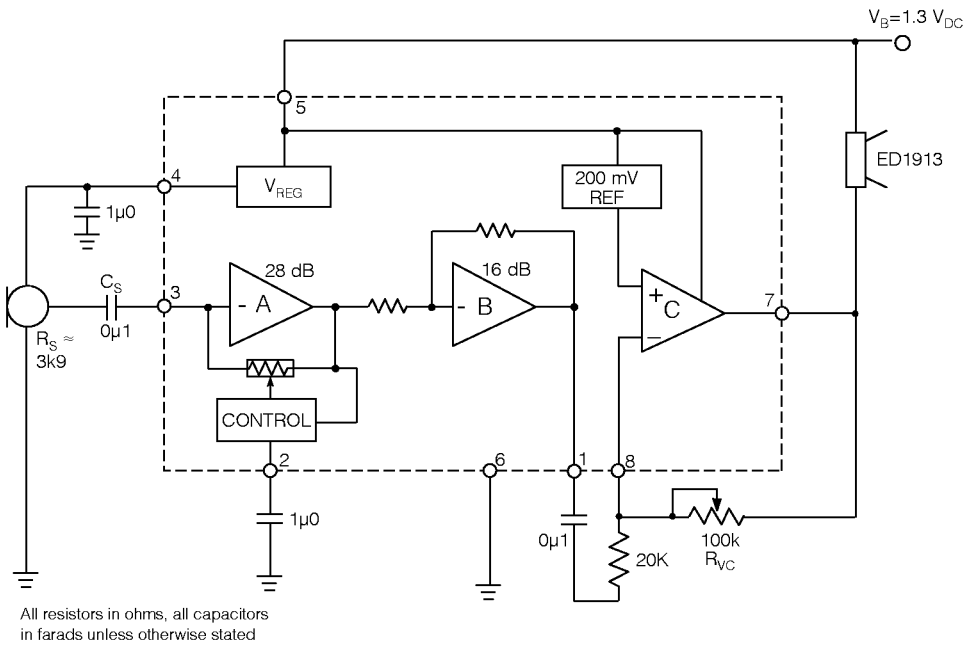


Fig. 3 Typical Hearing Aid Application

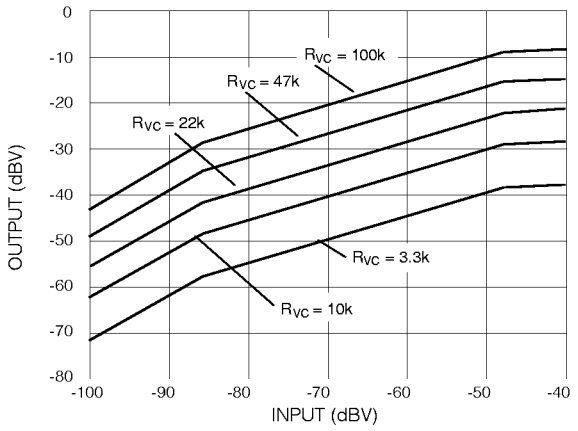


Fig. 4 I/O Characteristics at Various R_{VC} Values (Pin 7)

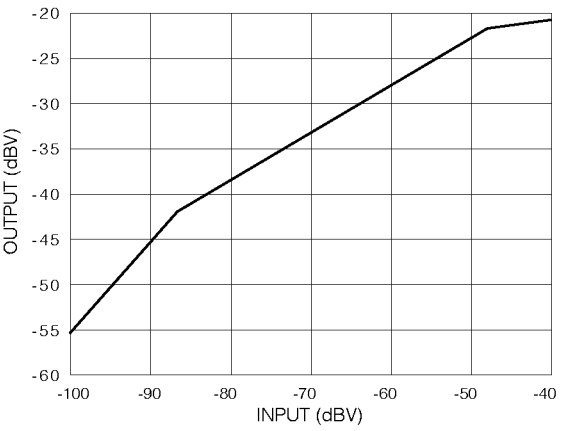


Fig. 5 I/O Characteristics at Pin 1

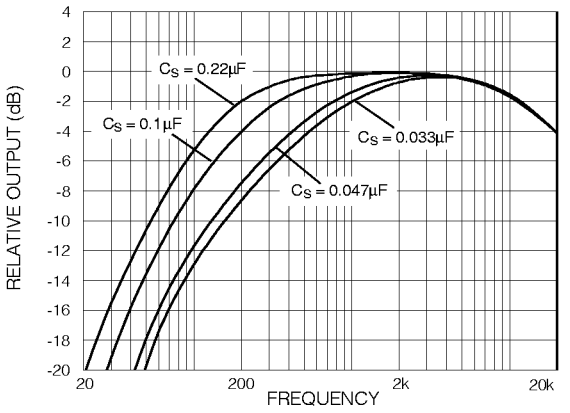


Fig. 6 Closed Loop Frequency Response at Various C_S Values

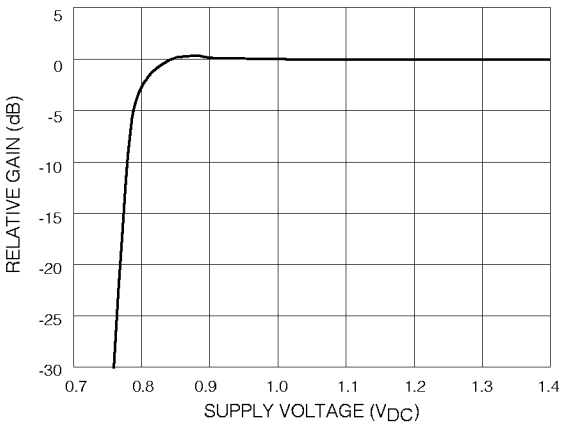


Fig. 7 Gain vs Supply Voltage

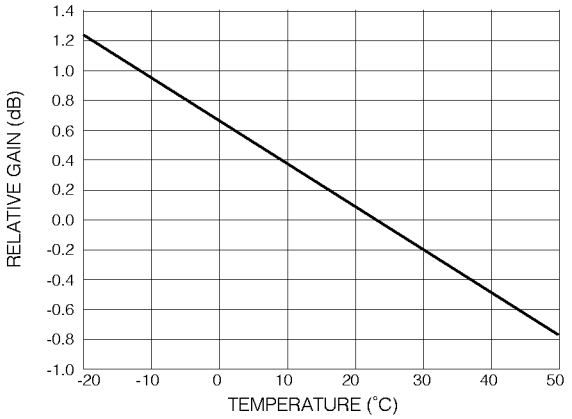


Fig. 8 Gain vs Temperature

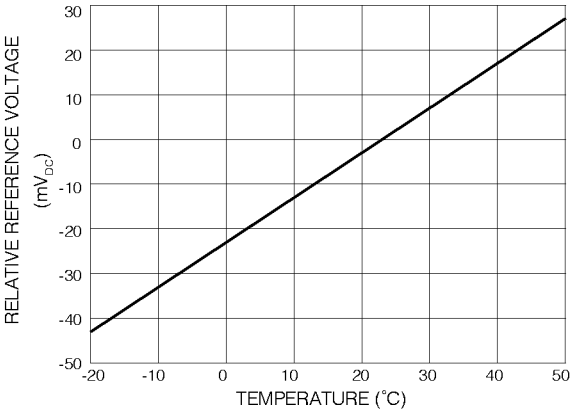


Fig. 9 Receiver Bias Voltage vs Temperature

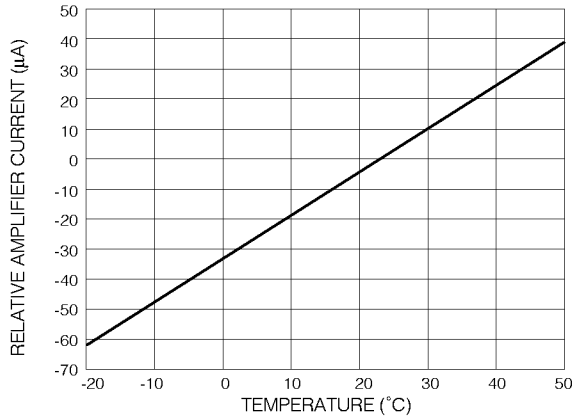


Fig. 10 Amplifier Current vs Temperature

DOCUMENT IDENTIFICATION

PRODUCT PROPOSAL
This data has been compiled for market investigation purposes only, and does not constitute an offer for sale.

ADVANCE INFORMATION NOTE
The product is in a development phase and specifications are subject to change without notice. Gennum reserves the right to remove the product at any time. Listing the product does not constitute an offer for sale

PRELIMINARY
The product is in a preproduction phase and specifications are subject to change without notice.

DATA SHEET
The product is in production. Gennum reserves the right to make changes at any time to improve reliability, function or design, in order to provide the best product possible.

REVISION NOTES
Revision 07 - Figure 5 amended.

GENNUM CORPORATION

Assembly Methods for SLT Packaged Integrated Circuits

8 & 10 PIN SLT APPLICATION NOTE

T-90-20

INTRODUCTION

The SLT is a miniature fine pitch plastic encapsulation housing an integrated circuit. The packaging utilizes tape automated bonding (TAB) technology, and has leads folded on the side of the plastic capsule. The distance between the leads is 2.38mm (0.094") with overall height of 1.17mm (0.046") maximum. The outline dimensions of the packages are:

8 Pin	2.38 (0.094") x 2.40 (0.094") x 1.17 mm (0.046")
10 Pin	2.38 (0.094") x 2.91 (0.115") x 1.17 mm (0.046")

Why SLT? The name of this product is an acronym for Stub Lead Tab Pack. Gennum has developed the SLT brand packaging for its miniature integrated circuit audio amplifiers to satisfy two distinct market needs.

The first need is driven by market demands to supply circuits in smaller packages to meet dimensional requirements of an industry that is producing products of continually decreasing size and increasing complexity, utilizing smaller real estate than chip/wire.

The second need is to supply a miniature packaged circuit which can be tested prior to assembly into a hybrid circuit using alumina substrates, epoxy printed circuit boards or flex circuit boards and offers "reworkability", (i.e. aid's "manufacturability").

The purpose of what follows is to provide assistance to design and production personnel in the assembly of SLT packaged devices onto miniature printed circuit boards or ceramic substrates. The technical details encompassed in this note are based on Gennum's findings.

SUGGESTED PAD GEOMETRY FOR SLT PACKAGED DEVICES

The lands to which SLT terminals are to be soldered should be located in accordance with the SLT terminal pattern shown in Figures 1 and 2 and should carefully be placed and sized. The dimensions of the lands and adjacent conductors must be properly determined so that the solder will not run onto the conductors and will hold the SLT devices firmly in place. The lands should ideally be 0.05 mm (0.002 inch) per side larger than the SLT lead width, causing a fillet to be formed at the contact edges. If any conductor is wider than 0.254 mm (0.010 inch), it should be necked to 0.254 mm (0.010"), as shown in Figure 2. The purpose of necking down the conductors is to prevent solder back flow (this rule is applicable when no solder resist is used). Although it is strongly recommended that solder resist be used where possible.

Note: It is very important to ensure that the coplanarity of the solder pads on the circuit board substrate be maintained to very tight tolerances.

STENCIL DESIGN

Because of the fine pitch of the SLT, it is recommended that metal stencil be used instead of screen stencil. The stencil or mask should be 0.1 mm (0.004") thick, with the pattern obtained by an etching process. It is important that the stencil be etched simultaneously from both sides to reduce undercutting of the pattern, and the amount of under cutting should be compensated for during the manufacture of the stencil.

A suggested solder mask pattern is shown in Figure 3. The solder paste should be applied to all the lands on the substrate in one stroke through the stencil as shown in Figure 5. The metal stencil is stretched tight and cemented to a fixture as shown in Figure 6.

The fixture is attached to a hinged platform, so that it can be raised to permit loading of the substrate onto a vacuum chuck located directly below. Exact positioning of the substrate on the vacuum pedestal can be best achieved by a series of locating pins. Vacuum hold-down is required to hold the substrate fixed when the stencil is raised for "snap-off" from the solder paste pattern.

Note: All other devices which are to be surface mounted, should have their solder paste screened on at the same time, (i.e. stencil should be designed as such).

For high volume production, the pattern can be step and repeated "N" number of times, to correspond with the "N" number of circuit board patterns being assembled. The accuracy and consistency of solder paste application in this instance should be taken into account in the stencil design.

SCREEN PRINTING

To set up initially, the operator places the substrate on the vacuum chuck and lowers the stencil onto the substrate. Solder paste is applied using a teflon or polyurethane squeegee as shown in Fig. 7 (for high volume production, automated screen printers are usually available). This produces a uniform paste layer of a thickness equal to the metal stencil.

After the solder paste has been screened, the stencil must be raised vertically to provide a "snap-off". This motion is necessary to leave a well defined pattern on the substrate. Any horizontal movement will smear the pattern and increase the possibility of solder bridging of conductors on solder reflow.

The substrate is now ready for placement of surface mount components.

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SOLDER REFLOW

The SLT can be easily soldered to the substrate using solder reflow techniques. Fig. 4 illustrates typically the solder temperature profile used to reflow SLTs.

For rigid substrates a 63 Sn/37 Pb solder cream (90% metal, -325 +500 mesh or type 3), containing the necessary flux is screened onto the land area. Kester Part #R-229-25 RMA or Alpha Part # RMA-390 DH3 performs well with no solder bridging evident. Excellent fillet formation at the land/device contact interface is apparent.

RECOMMENDED STEPS IN ASSEMBLY

Note: No precleaning of SLT devices is required prior to use.

STEP 1 SOLDER PASTE APPLICATION

Solder paste is screened onto the substrate using a squeegee as discussed under the heading "screen printing".

Important variables:

- age of solder paste
- time between solder paste application and reflow
- accuracy and consistency in placing solder paste

STEP 2 DEVICE PLACEMENT

The SLT is placed on the land area of the substrate with use of tweezers. A low power magnifier will assist the operator in easy, accurate location of the device over the circuit lands. It is best to bring the device above the application area, then descend vertically in one movement to avoid smearing the solder cream. It is important to precisely position the device over the contact lands.

For high volume production, the pick and place machine should have vision capability with two attributes:

1. Board error correction and
2. Component lead inspection (from under the device), or alternatively a dedicated pickup head with a recess shaped to the top section of SLT and vacuum for pickup can be used to center and square the device for placement.

The accurate placement of SLT devices is important in obtaining excellent soldering results, as the solder paste will not correct poor placement.

To prevent lead bending and maintain the pitch to pitch dimensions, the device should not be held or manipulated by the leads. Consistency and control of the placement force is also required.

STEP 3 SOLDER REFLOW

Heating the SLT and substrate for reflow soldering at 215°C (as measured at the lead/land interface) can be accompanied by any of the following techniques.

A) Infra-red solder reflow oven.

B) Vapor phase solder reflow.

Two versions are available:

B1 Batch type (immersion)

B2 Conveyor type

C) Conduction / convection - this method is not preferred as the process is difficult to control.

Since Gennum believes that these techniques are well known to users of our circuits, no discussion of them is included in this note.

STEP 4 CLEANING

Cleaning the completed hybrid circuit is the final step in this assembly process. Ultrasonic cleaning is preferred to remove the flux residue which could corrode the solder joint in time.

STEP 5 INSPECTION/PROCESS MONITORING

The importance or process selection (for optimum yields) and control is very critical in the successful use of SLT devices. It is of utmost importance to ensure the any deviation from the "normally" expected soldering results, be analyzed and the cause be established, such that steps can be taken to bring the process back into control.

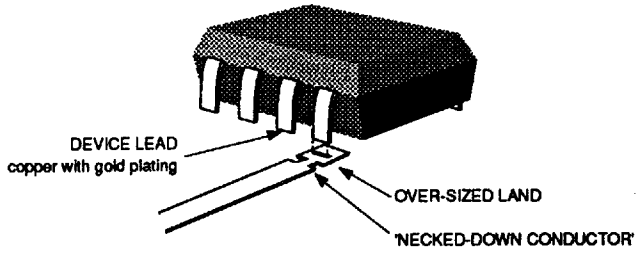
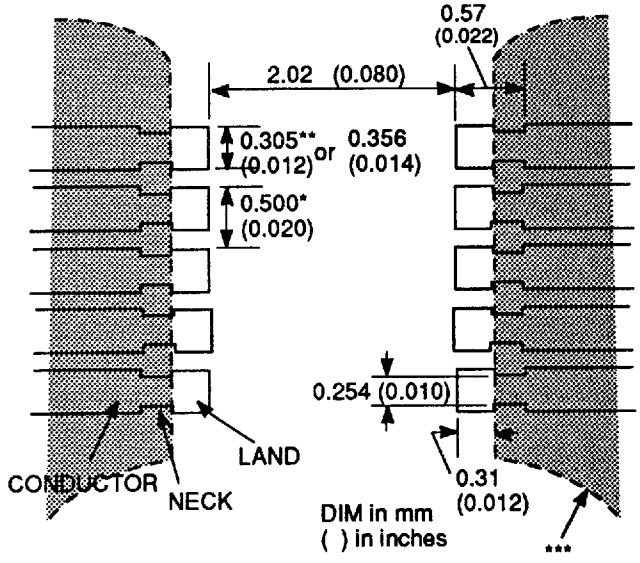


Fig. 1 Location of Conductor relative to Device Lead

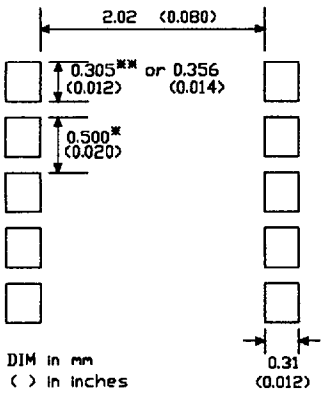


* 4 spaces at 0.5 ±0.05 non-cumulative for 8 pin SLT
5 spaces at 0.5 +0.05 non-cumulative for 10 pin SLT

** Size should be established based on
- choice of interconnect medium
- assembly process capability

*** Extent of solder resist, in which case "necking" will not be required. It is of utmost importance to have symmetrical pads only.

Fig. 2 SLT Solder Pad Pattern



* 4 spaces at 0.5 ±0.05 non-cumulative for 8 pin SLT
5 spaces at 0.5 ±0.05 non-cumulative for 10 pin SLT

** Choice of size should correspond with size selected in Fig. 2.

Fig. 3 Solder Mask Pattern for SLT

T-90-20

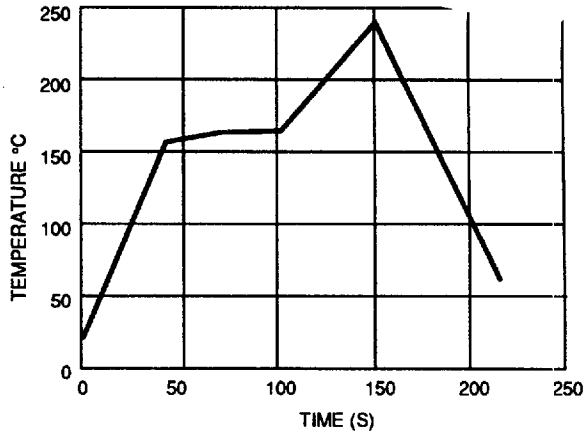


Fig. 4 SLT Solder Reflow Temperature Profile

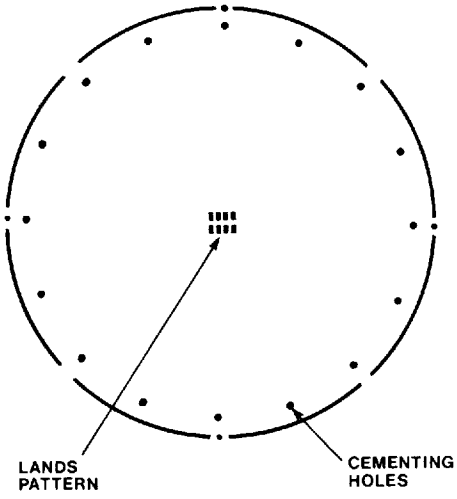


Fig. 5 Stencil for Solder Paste

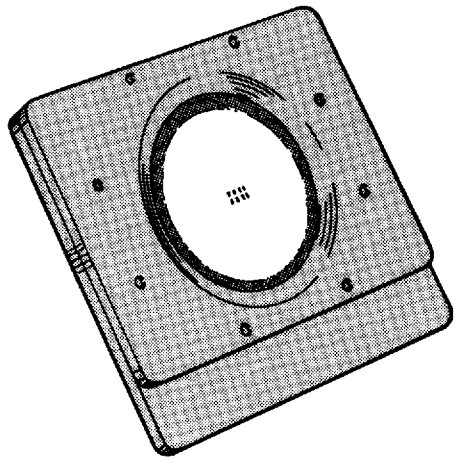


Fig. 6 Holding Plate for Stencil

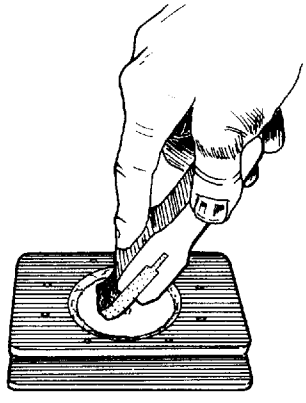


Fig. 7 Screen Printing of Paste with Squeegee