

Dual/Quad 3.2MHz, 0.8V/ μ s Low Power, Over-The-Top Precision Op Amp

FEATURES

- Input Common Mode Range: V^- to $V^- + 76V$
- Rail-to-Rail Input and Output
- Low Power: 315 μ A/Amplifier
- Operating Temperature Range: -55°C to 150°C
- V_{OS} : $\pm 50\mu\text{V}$ (Maximum)
- CMRR, PSRR: 126dB
- Reverse Battery Protection to 50V
- Gain Bandwidth Product: 3.2MHz
- Specified on 5V and $\pm 15V$ Supplies
- High Voltage Gain: 1000V/mV
- No Phase Reversal
- No Supply Sequencing Problems
- Dual 8-Lead MSOP
- Quad 22-Lead DFN (6mm \times 3mm)

APPLICATIONS

- High Side or Low Side Current Sensing
- Battery/Power Supply Monitoring
- 4mA to 20mA Transmitters
- High Voltage Data Acquisition
- Battery/Portable Instrumentation

DESCRIPTION

The LT[®]6016/LT6017 are dual and quad rail-to-rail input operational amplifiers with input offset voltage trimmed to less than 50 μ V. These amplifiers operate on single and split supplies with a total voltage of 3V to 50V and draw only 315 μ A per amplifier. They are reverse battery protected, drawing very little current for reverse supplies up to 50V.

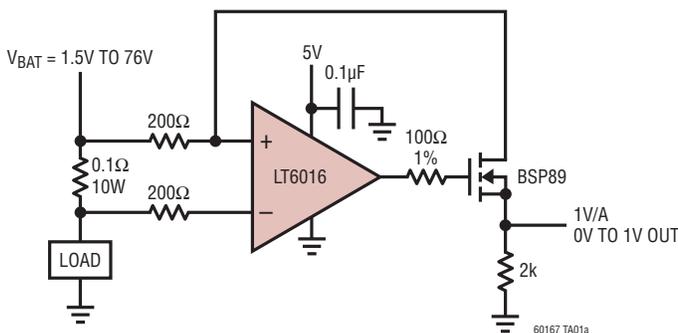
The Over-The-Top[®] input stage of the LT6016/LT6017 is designed to provide added protection in tough environments. The input common mode range extends from V^- to V^+ and beyond: these amplifiers operate with inputs up to 76V above V^- independent of V^+ . Internal resistors protect the inputs against transient faults up to 25V below the negative supply. The LT6016/LT6017 can drive loads up to 25mA and are unity-gain stable with capacitive loads as large as 200pF. Optional external compensation can be added to extend the capacitive drive capability beyond 200pF.

The LT6016 dual op amp is available in an 8-lead MSOP package. The LT6017 is offered in a 22-pin leadless DFN package.

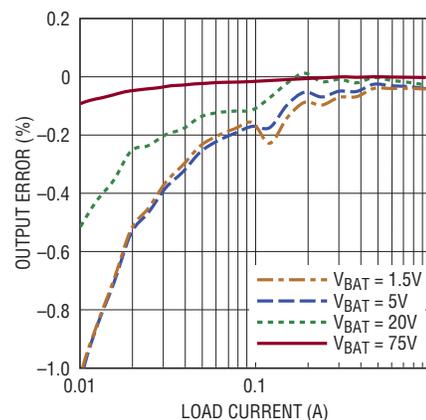
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TYPICAL APPLICATION

Precision High Voltage High Side Load Current Monitor



Output Error vs Load Current



60167 TA01b

LT6016/LT6017

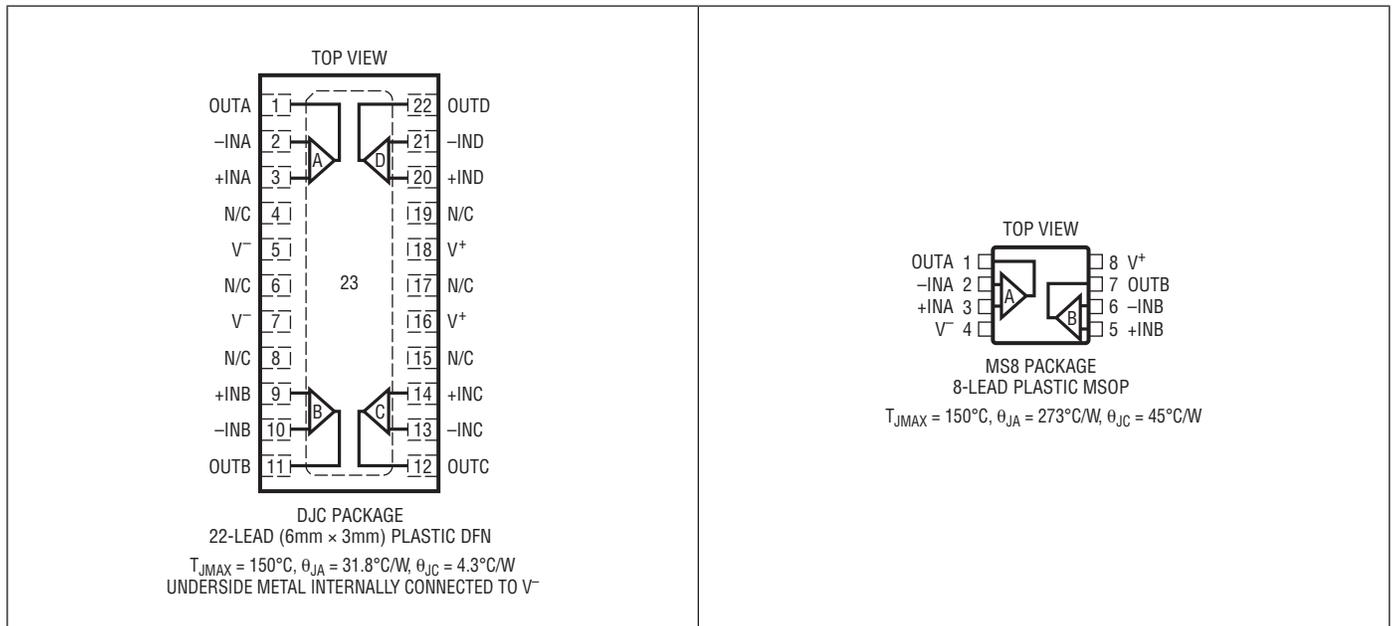
ABSOLUTE MAXIMUM RATINGS

(Note 1)

Supply Voltage (V^+ to V^-).....60V, -50V
 Input Differential Voltage±80V
 Input Voltage (Note 2).....80V, -25V
 Input Current (Note 2).....±10mA
 Output Short Circuit Duration
 (Note 3)..... Continuous

Temperature Range (Notes 4, 5)
 LT6016I/LT6017I.....-40°C to 85°C
 LT6016H/LT6017H.....-40°C to 125°C
 LT6016MP/LT6017MP($T_{JUNCTION}$)-55°C to 150°C
 Storage Temperature Range-65°C to 150°C
 Maximum Junction Temperature 150°C
 Lead Temperature (Soldering, 10sec)..... 300°C

PIN CONFIGURATION



ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LT6016IMS8#PBF	LT6016IMS8#TRPBF	LTGFK	8-Lead Plastic MSOP	-40°C to 85°C
LT6016HMS8#PBF	LT6016HMS8#TRPBF	LTGFK	8-Lead Plastic MSOP	-40°C to 125°C
LT6016MPMS8#PBF	LT6016MPMS8#TRPBF	LTGFK	8-Lead Plastic MSOP	-55°C to 150°C
LT6017IDJC#PBF	LT6017IDJC#TRPBF	6017	22-Lead Plastic DFN	-40°C to 85°C
LT6017HDJC#PBF	LT6017HDJC#TRPBF	6017	22-Lead Plastic DFN	-40°C to 125°C
LT6017MPDJC#PBF	LT6017MPDJC#TRPBF	6017	22-Lead Plastic DFN	-55°C to 150°C

Consult LTC Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.

For more information on lead free part marking, go to: <http://www.linear.com/leadfree/>

For more information on tape and reel specifications, go to: <http://www.linear.com/tapeandreeel/>

ELECTRICAL CHARACTERISTICS The ● denotes the specifications which apply over the specified temperature range, $-40^{\circ}\text{C} < T_A < 85^{\circ}\text{C}$ for I-grade parts, $-40^{\circ}\text{C} < T_A < 125^{\circ}\text{C}$ for H-grade parts, otherwise specifications are at $T_A = 25^{\circ}\text{C}$, $V_S = 5\text{V}$, $V_{CM} = V_{OUT} = \text{mid-supply}$.

SYMBOL	PARAMETER	CONDITIONS	I-, H-GRADE			UNITS
			MIN	TYP	MAX	
V _{OS}	Input Offset Voltage	0 < V _{CM} < V ⁺ - 1.75V MS8 Package	-50	±25	50	μV
		0 < V _{CM} < V ⁺ - 1.75V DJC22 Package	-80	±45	80	μV
		V _{CM} = 5V	-125	±50	125	μV
		V _{CM} = 76V	-135	±50	135	μV
		0 < V _{CM} < V ⁺ - 1.75V V _{CM} = 5V to V _{CM} = 76V	● -250	±45	250	μV
● -350	±50	350	μV			
$\frac{\Delta V_{OS}}{\Delta \text{TEMP}}$	Input Offset Voltage Drift			0.75		μV/°C
$\frac{\Delta V_{OS}}{\Delta \text{TIME}}$	Long Term Voltage Offset Stability			0.75		μV/Mo
I _B	Input Bias Current	0.25V < V _{CM} < V ⁺ - 1.75V V _{CM} = 0V	-5	±2	5	nA
		V _{CM} = 5V to 76V	-30	-16.5	0	nA
		0.25V < V _{CM} < V ⁺ - 1.75V V _{CM} = 0V	● 11	14	17.5	μA
		V _{CM} = 5V to 76V	● -15	±2	15	nA
		V _S = 0V, V _{CM} = 0V to 76V	● -150	-16.5	0	nA
		● 7	14	23	μA	
● 0.001	1		μA			
I _{OS}	Input Offset Current	0.25V < V _{CM} < V ⁺ - 1.75V V _{CM} = 0V	-5	±2	5	nA
		V _{CM} = 5V to 76V (Note 6)	-5	±2	5	nA
		0.25V < V _{CM} < V ⁺ - 1.75V V _{CM} = 0V	● -500	±50	500	nA
		V _{CM} = 5V to 76V (Note 6)	● -15	±2	15	nA
		● -500	±50	500	nA	
VC _{MR}	Common Mode Input Range		● 0		76	V
C _{IN}	Differential Input Capacitance			5		pF
R _{IN}	Differential Input Resistance	0 < V _{CM} < V ⁺ - 1.75V		1		MΩ
		V _{CM} > V ⁺		3.7		kΩ
R _{INCM}	Common Mode Input Resistance	0 < V _{CM} < V ⁺ - 1.75V V _{CM} > V ⁺		>1		GΩ
				>100		MΩ
e _n	Input Referred Noise Voltage Density	f = 1kHz V _{CM} < V ⁺ - 1.75V V _{CM} > V ⁺		18		nV/√Hz
	Input Referred Noise Voltage	f = 0.1Hz to 10Hz V _{CM} < V ⁺ - 1.75V		25		nV/√Hz
				0.5		μV _{P-P}
i _n	Input Referred Noise Current Density	f = 1kHz V _{CM} < V ⁺ - 1.75V V _{CM} > V ⁺		0.1		pA/√Hz
				11.5		pA/√Hz
A _{VOL}	Open Loop Gain	R _L = 10kΩ ΔV _{OUT} = 3V	● 300	3000		V/mV
PSRR	Supply Rejection Ratio	V _S = ±1.65V to ±15V V _{CM} = V _{OUT} = Mid-Supply	● 110	126		dB
CMRR	Input Common Mode Rejection Ratio	V _{CM} = 0V to 3.25V	● 100	126		dB
		V _{CM} = 5V to 76V	● 126	140		dB
V _{OL}	Output Voltage Swing Low	V _S = 5V, No Load	●	3	55	mV
		V _S = 5V, 5mA	●	280	500	mV
V _{OH}	Output Voltage Swing High	V _S = 5V, No Load	●	450	700	mV
		V _S = 5V, 5mA	●	1000	1250	mV
I _{SC}	Short-Circuit Current	V _S = 5V, 50Ω to V ⁺	● 10	25		mA
		V _S = 5V, 50Ω to V ⁻	● 10	25		mA

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the specified temperature range, $-40^{\circ}\text{C} < T_A < 85^{\circ}\text{C}$ for I-grade parts, $-40^{\circ}\text{C} < T_A < 125^{\circ}\text{C}$ for H-grade parts, otherwise specifications are at $T_A = 25^{\circ}\text{C}$, $V_S = 5\text{V}$, $V_{CM} = V_{OUT} = \text{mid-supply}$.

SYMBOL	PARAMETER	CONDITIONS	I-, H-GRADE			UNITS
			MIN	TYP	MAX	
GBW	Gain Bandwidth Products	$f_{TEST} = 10\text{kHz}$	● 2.85	3.2		MHz
			2.5	3.2		MHz
SR	Slew Rate	$\Delta V_{OUT} = 3\text{V}$	● 0.55	0.75		V/ μs
			0.45	0.75		V/ μs
t_S	Settling Time Due to Input Step $\Delta V_{OUT} = \pm 2\text{V}$	0.1% Settling		3.5		μs
V_S	Supply Voltage		● 3		50	V
			3.3		50	V
	Reverse Supply (Note 7)	$I_S < -25\mu\text{A}/\text{Amplifier}$	●	-65	-50	V
I_S	Supply Current Per Amplifier	$V_S = 5\text{V}$	●	315	335	μA
				315	500	μA
R_O	Output Impedance	$\Delta I_O = \pm 5\text{mA}$		0.15		Ω

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SYMBOL	PARAMETER	CONDITIONS	I-, H-GRADE			UNITS
			MIN	TYP	MAX	
V_{OSI}	Input Offset Voltage		● -80	± 55	80	μV
			● -250	± 55	250	μV
			● -110	± 75	110	μV
			● -250	± 75	250	μV
$\frac{\Delta V_{OSI}}{\Delta \text{TEMP}}$	Input Offset Voltage Drift			0.75		$\mu\text{V}/^{\circ}\text{C}$
I_B	Input Bias Current		● -5	± 2	5	nA
			● -15	± 2	15	nA
I_{OS}	Input Offset Current		● -5	± 2	5	nA
			● -15	± 2	15	nA
VCMR	Common Mode Input Range		● -15		61	V
C_{IN}	Differential Input Capacitance			5		pF
R_{IN}	Differential Input Resistance	$0 < V_{CM} < V^+ - 1.75\text{V}$		1		M Ω
		$V_{CM} > V^+$		3.7		k Ω
R_{INCM}	Common Mode Input Resistance	$0 < V_{CM} < V^+ - 1.75\text{V}$		>1		G Ω
		$V_{CM} > V^+$		>100		M Ω
e_n	Input Referred Noise Voltage Density	$f = 1\text{kHz}$ $V_{CM} < V^+ - 1.75\text{V}$ $V_{CM} > V^+$		18		nV/ $\sqrt{\text{Hz}}$
				25		nV/ $\sqrt{\text{Hz}}$
	Input Referred Noise Voltage	$f = 0.1\text{Hz to } 10\text{Hz}$ $V_{CM} < V^+ - 1.25\text{V}$		0.5		μV_{P-P}
i_n	Input Referred Noise Current Density	$f = 1\text{kHz}$ $V_{CM} < V^+ - 1.75\text{V}$ $V_{CM} > V^+$		0.1		pA/ $\sqrt{\text{Hz}}$
					11.5	
A_{VOL}	Open Loop Gain	$R_L = 10\text{k}\Omega$ $\Delta V_{OUT} = 27\text{V}$	● 200	1000		V/mV
PSRR	Supply Rejection Ratio	$V_S = \pm 2.5\text{V to } \pm 25\text{V}$ $V_{CM} = V_{OUT} = 0\text{V}$	● 114	126		dB
CMRR	Input Common Mode Rejection Ratio	$V_{CM} = -15\text{V to } 13.25\text{V}$	● 110	126		dB
V_{OL}	Output Voltage Swing Low	$V_S = \pm 15\text{V}$, No Load $V_S = \pm 15\text{V}$, 5mA	● 3		55	mV
			● 280		500	mV
V_{OH}	Output Voltage Swing High	$V_S = \pm 15\text{V}$, No Load $V_S = \pm 15\text{V}$, 5mA	● 450		700	mV
			● 1000		1250	mV

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SYMBOL	PARAMETER	CONDITIONS	I-, H-GRADE			UNITS	
			MIN	TYP	MAX		
I_{SC}	Short-Circuit Current	$V_S = \pm 15\text{V}$, 50Ω to GND	●	10	30	mA	
			●	10	32		
GBW	Gain Bandwidth Product	$f_{TEST} = 10\text{kHz}$	●	2.9	3.3	MHz	
			●	2.55	3.3		
SR	Slew Rate	$\Delta V_{OUT} = 3\text{V}$	●	0.6	0.8	V/ μs	
			●	0.5	0.8		
t_S	Settling Time Due to Input Step	0.1% Settling $\Delta V_{OUT} = \pm 2\text{V}$			3.5	μs	
V_S	Supply Voltage		●	3	50	V	
	Reverse Supply	$I_S = -25\mu\text{A}/\text{Amplifier}$	●	3.3	50	V	
I_S	Supply Current Per Amplifier	$V_S = \pm 25\text{V}$ $V_S = \pm 25\text{V}$	●		-65	-30	V
			●				
			●		325	350	μA
			●		325	525	μA
R_O	Output Impedance	$\Delta I_O = \pm 5\text{mA}$			340	360	μA
						340	550
					0.15	Ω	

The ● denotes the specifications which apply over the specified temperature range, $-55^{\circ}\text{C} < T_{JUNCTION} < 150^{\circ}\text{C}$ for MP-grade parts, otherwise specifications are at $T_A = 25^{\circ}\text{C}$, $V_S = 5\text{V}$, $V_{CM} = V_{OUT} = \text{mid-supply}$.

SYMBOL	PARAMETER	CONDITIONS	MP-GRADE			UNITS	
			MIN	TYP	MAX		
V_{OS}	Input Offset Voltage	$0 < V_{CM} < V^+ - 1.75\text{V}$ MS8 Package		-50	± 25	50	μV
		$0 < V_{CM} < V^+ - 1.75\text{V}$ DJC22 Package		-80	± 45	80	μV
		$V_{CM} = 5\text{V}$		-125	± 50	125	μV
		$V_{CM} = 76\text{V}$		-135	± 50	135	μV
		$0 < V_{CM} < V^+ - 1.75\text{V}$	●	-500	± 45	500	μV
		$V_{CM} = 5\text{V}$ to $V_{CM} = 76\text{V}$	●	-600	± 50	600	μV
$\frac{\Delta V_{OS}}{\Delta \text{TEMP}}$	Input Offset Voltage Drift			0.75		$\mu\text{V}/^{\circ}\text{C}$	
$\frac{\Delta V_{OS}}{\Delta \text{TIME}}$	Long Term Voltage Offset Stability			0.75		$\mu\text{V}/\text{Mo}$	
I_B	Input Bias Current	$0.25\text{V} < V_{CM} < V^+ - 1.75\text{V}$ $V_{CM} = 0\text{V}$		-5	± 2	5	nA
		$V_{CM} = 5\text{V}$ to 76V		-30	-16.5	0	nA
		$0.25\text{V} < V_{CM} < V^+ - 1.75\text{V}$ $V_{CM} = 0\text{V}$	●	11	14	17.5	μA
		$V_{CM} = 5\text{V}$ to 76V	●	-100	± 2	100	nA
		$V_S = 0\text{V}$, $V_{CM} = 0\text{V}$ to 76V	●	-500	-16.5	0	nA
			●	6.5	14	24	μA
I_{OS}	Input Offset Current	$0.25\text{V} < V_{CM} < V^+ - 1.75\text{V}$ $V_{CM} = 0\text{V}$		-5	± 2	5	nA
		$V_{CM} = 5\text{V}$ to 76V (Note 6)		-5	± 2	5	nA
		$0.25\text{V} < V_{CM} < V^+ - 1.75\text{V}$ $V_{CM} = 0\text{V}$	●	-500	± 50	500	nA
		$V_{CM} = 5\text{V}$ to 76V (Note 6)	●	-50	± 2	50	nA
			●	-200	± 2	200	nA
			●	-500	± 150	500	nA
VCMR	Common Mode Input Range		●	0		76	V
C_{IN}	Differential Input Capacitance				5	pF	
R_{IN}	Differential Input Resistance	$0 < V_{CM} < V^+ - 1.75\text{V}$ $V_{CM} > V^+$			1	M Ω	
					3.7	k Ω	
R_{INCM}	Common Mode Input Resistance	$0 < V_{CM} < V^+ - 1.75\text{V}$ $V_{CM} > V^+$			>1	G Ω	
					>100	M Ω	

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SYMBOL	PARAMETER	CONDITIONS	MP-GRADE			UNITS	
			MIN	TYP	MAX		
e_n	Input Referred Noise Voltage Density	$f = 1\text{kHz}$ $V_{\text{CM}} < V^+ - 1.75\text{V}$ $V_{\text{CM}} > V^+$		18 25		$\text{nV}/\sqrt{\text{Hz}}$ $\text{nV}/\sqrt{\text{Hz}}$	
	Input Referred Noise Voltage	$f = 0.1\text{Hz to } 10\text{Hz}$ $V_{\text{CM}} < V^+ - 1.75\text{V}$		0.5		$\mu\text{V}_{\text{P-P}}$	
i_n	Input Referred Noise Current Density	$f = 1\text{kHz}$ $V_{\text{CM}} < V^+ - 1.75\text{V}$ $V_{\text{CM}} > V^+$		0.1 11.5		$\text{pA}/\sqrt{\text{Hz}}$ $\text{pA}/\sqrt{\text{Hz}}$	
A_{VOL}	Open Loop Gain	$R_L = 10\text{k}\Omega$ $\Delta V_{\text{OUT}} = 3\text{V}$	●	200	3000	V/mV	
PSRR	Supply Rejection Ratio	$V_S = \pm 1.65\text{V to } \pm 15\text{V}$ $V_{\text{CM}} = V_{\text{OUT}} = \text{Mid-Supply}$	●	106	126	dB	
CMRR	Input Common Mode Rejection Ratio	$V_{\text{CM}} = 0\text{V to } 3.25\text{V}$ $V_{\text{CM}} = 5\text{V to } 76\text{V}$	●	90	126	dB	
			●	120	140	dB	
V_{OL}	Output Voltage Swing Low	$V_S = 5\text{V, No Load}$ $V_S = 5\text{V, } 5\text{mA}$	●		3	75	mV
			●		280	550	mV
V_{OH}	Output Voltage Swing High	$V_S = 5\text{V, No Load}$ $V_S = 5\text{V, } 5\text{mA}$	●		450	750	mV
			●		1000	1300	mV
I_{SC}	Short-Circuit Current	$V_S = 5\text{V, } 50\Omega \text{ to } V^+$ $V_S = 5\text{V, } 50\Omega \text{ to } V^-$	●	8	25	mA	
			●	8	25	mA	
GBW	Gain Bandwidth Product	$f_{\text{TEST}} = 10\text{kHz}$	●	2.85	3.2	MHz	
				2.4	3.2	MHz	
SR	Slew Rate	$\Delta V_{\text{OUT}} = 3\text{V}$	●	0.55	0.75	$\text{V}/\mu\text{s}$	
				0.4	0.75	$\text{V}/\mu\text{s}$	
t_s	Settling Time Due to Input Step	0.1% Settling $\Delta V_{\text{OUT}} = \pm 2\text{V}$			3.5	μs	
V_S	Supply Voltage		●	3	50	V	
	Reverse Supply (Note 7)	$I_S < -25\mu\text{A}/\text{Amplifier}$	●	3.3	-63	-50	V
I_S	Supply Current Per Amplifier	$V_S = 5\text{V}$			315	335	μA
			●		315	540	μA
R_O	Output Impedance	$\Delta I_O = \pm 5\text{mA}$			0.15	Ω	

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SYMBOL	PARAMETER	CONDITIONS	MP-GRADE			UNITS	
			MIN	TYP	MAX		
V_{OSI}	Input Offset Voltage	$V_S = \pm 25\text{V}$ $V_S = \pm 25\text{V}$	●	-80	± 55	80	μV
				-500	± 55	500	μV
				-110	± 75	110	μV
			●	-500	± 75	500	μV
$\frac{\Delta V_{\text{OSI}}}{\Delta \text{TEMP}}$	Input Offset Voltage Drift			0.75		$\mu\text{V}/^{\circ}\text{C}$	
I_B	Input Bias Current		●	-5	± 2	5	nA
				-300	± 2	300	nA
I_{OS}	Input Offset Current		●	-5	± 2	5	nA
				-50	± 2	50	nA
VCMR	Common Mode Input Range		●	-15		61	V
C_{IN}	Differential Input Capacitance				5	pF	
R_{IN}	Differential Input Resistance	$0 < V_{\text{CM}} < V^+ - 1.75\text{V}$ $V_{\text{CM}} > V^+$			1		M Ω
					3.7		k Ω

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SYMBOL	PARAMETER	CONDITIONS	MP-GRADE			UNITS	
			MIN	TYP	MAX		
R_{INCM}	Common Mode Input Resistance	$0 < V_{\text{CM}} < V^+ - 1.75\text{V}$ $V_{\text{CM}} > V^+$		>1 >100		$\text{G}\Omega$ $\text{M}\Omega$	
e_n	Input Referred Noise Voltage Density	$f = 1\text{kHz}$ $V_{\text{CM}} < V^+ - 1.75\text{V}$ $V_{\text{CM}} > V^+$		18 25		$\text{nV}/\sqrt{\text{Hz}}$ $\text{nV}/\sqrt{\text{Hz}}$	
	Input Referred Noise Voltage	$f = 0.1\text{Hz to } 10\text{Hz}$ $V_{\text{CM}} < V^+ - 1.75\text{V}$		0.5		$\mu\text{V}_{\text{P-P}}$	
i_n	Input Referred Noise Current Density	$f = 1\text{kHz}$ $V_{\text{CM}} < V^+ - 1.75\text{V}$ $V_{\text{CM}} > V^+$		0.1 11.5		$\text{pA}/\sqrt{\text{Hz}}$ $\text{pA}/\sqrt{\text{Hz}}$	
A_{VOL}	Open Loop Gain	$R_L = 10\text{k}\Omega$ $\Delta V_{\text{OUT}} = 27\text{V}$	●	100	1000	V/mV	
PSRR	Supply Rejection Ratio	$V_S = \pm 2.5\text{V to } \pm 25\text{V}$ $V_{\text{CM}} = V_{\text{OUT}} = 0\text{V}$	●	106	126	dB	
CMRR	Input Common Mode Rejection Ratio	$V_{\text{CM}} = -15\text{V to } 13.25\text{V}$	●	100	126	dB	
V_{OL}	Output Voltage Swing Low	$V_S = \pm 15\text{V}$, No Load $V_S = \pm 15\text{V}$, 5mA	●		3	75	mV
			●		280	550	mV
V_{OH}	Output Voltage Swing High	$V_S = \pm 15\text{V}$, No Load $V_S = \pm 15\text{V}$, 5mA	●		450	750	mV
			●		1000	1300	mV
I_{SC}	Short-Circuit Current	$V_S = \pm 15\text{V}$, 50 Ω to GND $V_S = \pm 15\text{V}$, 50 Ω to GND	●	8	30	mA	
			●	8	32	mA	
GBW	Gain Bandwidth Product	$f_{\text{TEST}} = 10\text{kHz}$	●	2.9	3.3	MHz	
				2.45	3.3	MHz	
SR	Slew Rate	$\Delta V_{\text{OUT}} = 3\text{V}$	●	0.6	0.8	$\text{V}/\mu\text{s}$	
				0.45	0.8	$\text{V}/\mu\text{s}$	
t_s	Settling Time Due to Input Step	0.1% Settling $\Delta V_{\text{OUT}} = \pm 2\text{V}$		3.5		μs	
V_S	Supply Voltage		●	3	50	V	
	Reverse Supply	$I_S = -25\mu\text{A}/\text{Amplifier}$	●	3.3	50	V	
I_S	Supply Current Per Amplifier	$V_S = \pm 25\text{V}$ $V_S = \pm 25\text{V}$	●		-65	-30	V
			●		325	350	μA
			●		325	575	μA
			●		340	360	μA
			●		340	600	μA
R_O	Output Impedance	$\Delta I_O = \pm 5\text{mA}$			0.15	Ω	

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: Voltages applied are with respect to V^- . The inputs are tested to the Absolute Maximum Rating by applying -25V (relative to V^-) to each input for 10ms. In general, faults capable of sinking current from either input should be current limited to under 10mA. See the Applications Information section for more details.

Note 3: A heat sink may be required to keep the junction temperature below absolute maximum. This depends on the power supply voltage and how many amplifiers are shorted.

Note 4: The LT6016I/LT6017 are guaranteed functional over the operating temperature range of -40°C to 85°C . The LT6016H/LT6017H are guaranteed functional over the operating temperature range of -40°C to 125°C . The LT6016MP/LT6017MP are guaranteed functional over the

junction temperature range of -55°C to 150°C . Junction temperatures greater than 125°C will promote accelerated aging. The LT6016/LT6017 has a demonstrated typical performance beyond 1000 hours at $T_J = 150^{\circ}\text{C}$.

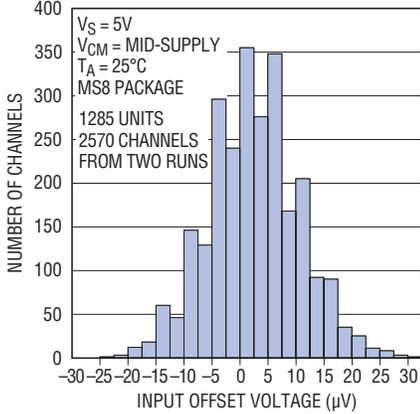
Note 5: The LT6016I/LT6017I are guaranteed to meet specified performance from -40°C to 85°C . The LT6016H/LT6017H are guaranteed to meet specified performance from -40°C to 125°C . The LT6016MP/LT6017MP are guaranteed to meet specified performance with junction temperature ranging from -55°C to 150°C .

Note 6: Test accuracy is limited by high speed test equipment repeatability. Bench measurements indicate the input offset current in the Over-The-Top configuration is typically controlled to under $\pm 50\text{nA}$ at 25°C and $\pm 150\text{nA}$ over temperature.

Note 7: The Reverse Supply voltage is tested by pulling $25\mu\text{A}/\text{Amplifier}$ out of the V^+ pin while measuring the V^+ pin's voltage with both inputs and V^- grounded, verifying $V^+ < -50\text{V}$.

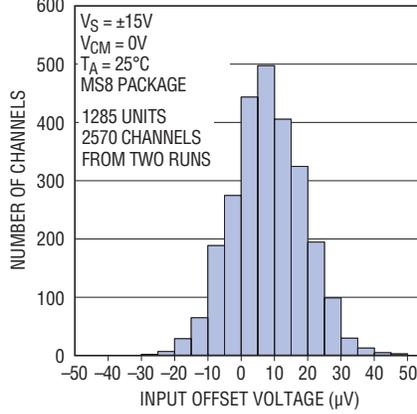
TYPICAL PERFORMANCE CHARACTERISTICS

Typical Distribution of Input Offset Voltage



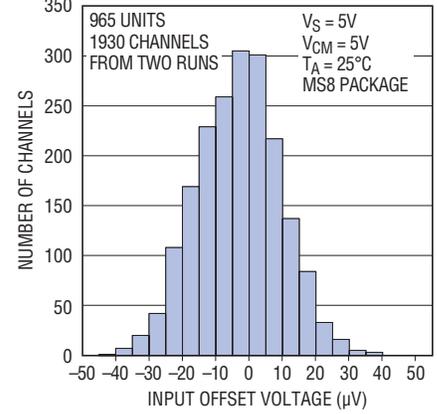
60167 G01

Typical Distribution of Input Offset Voltage



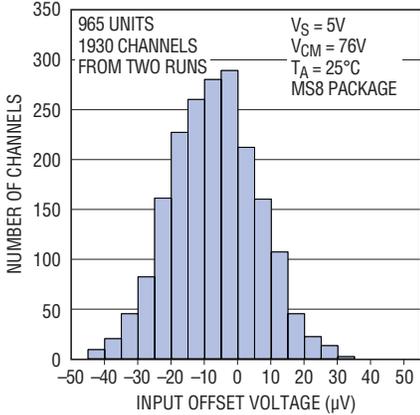
60167 G02

Typical Distribution of Over-The-Top Input Offset Voltage



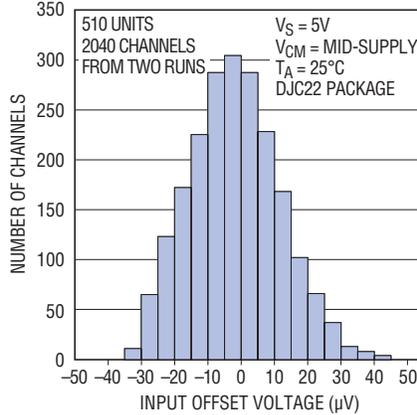
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Typical Distribution of Over-The-Top Input Offset Voltage



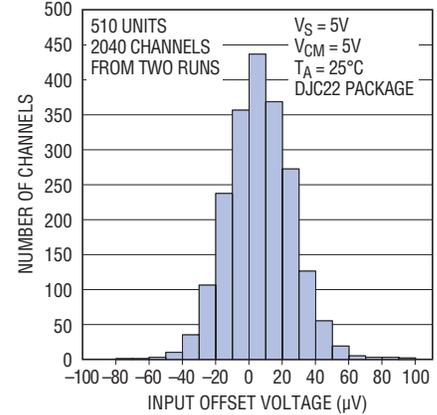
60167 G04

Typical Distribution of Input Offset Voltage



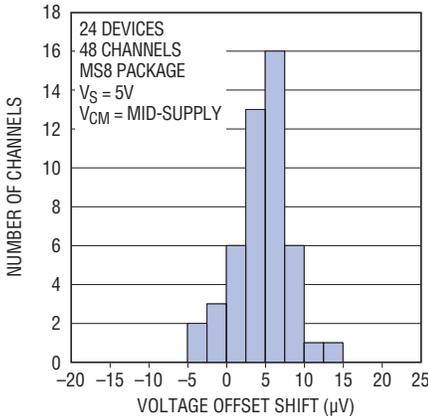
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Typical Distribution of Over-The-Top Input Offset Voltage



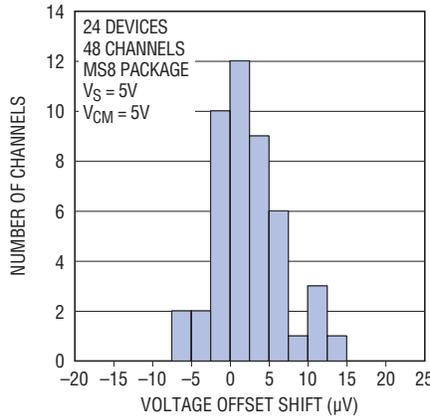
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Voltage Offset Shift vs Lead Free IR Reflow



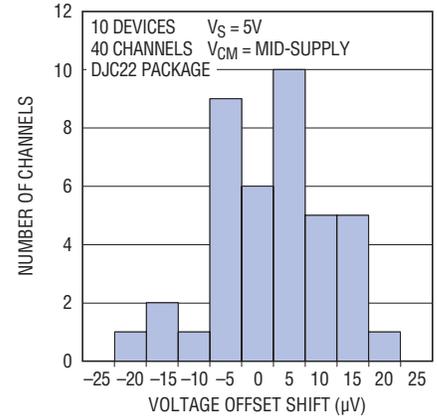
60167 G07

Over-The-Top Voltage Offset Shift vs Lead Free IR Reflow



60167 G08

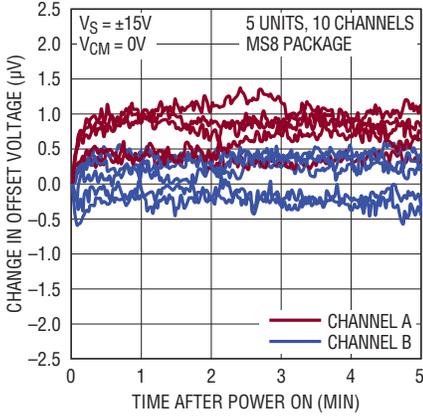
Voltage Offset Shift vs Lead Free IR Reflow



60167 G09

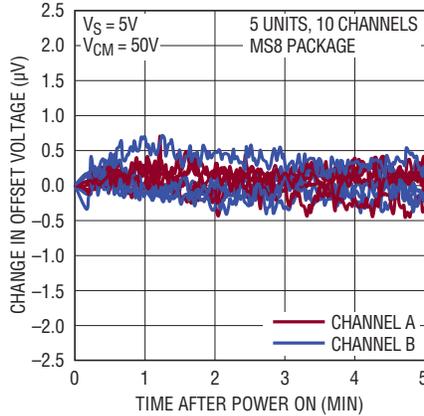
TYPICAL PERFORMANCE CHARACTERISTICS

Warm-Up Drift



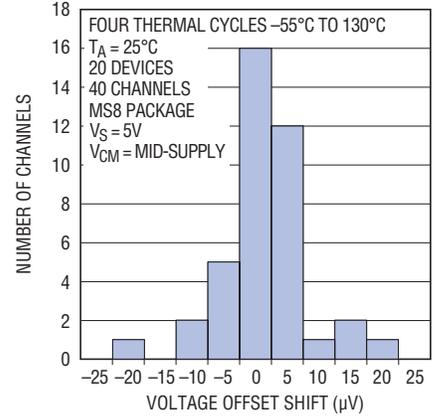
60167 G10

Over-The-Top Warm-Up Drift



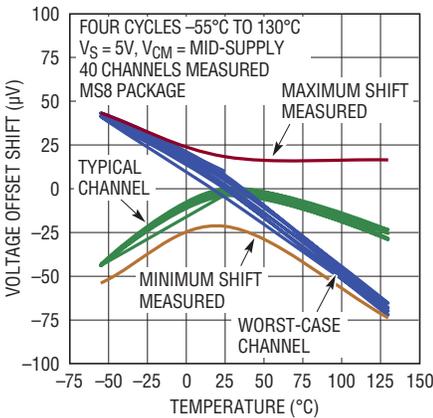
60167 G11

Voltage Offset Shift vs Thermal Cycling



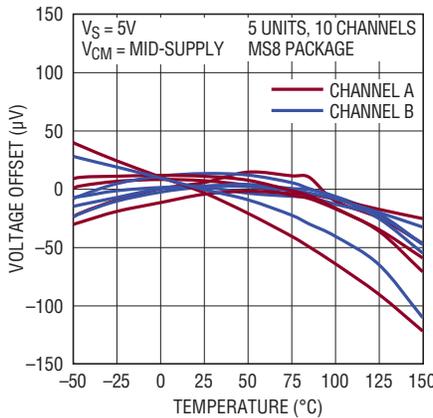
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Voltage Offset Shift vs Temperature Cycling



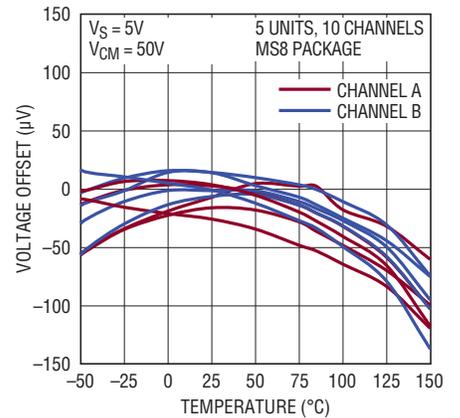
60167 G13

Voltage Offset vs Temperature



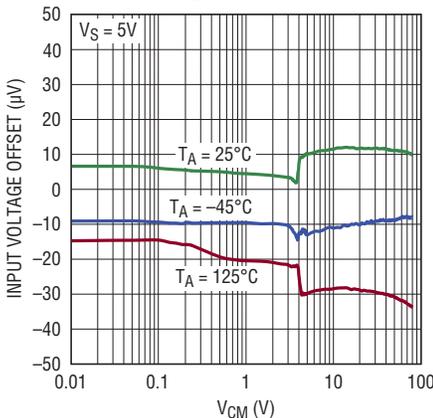
60167 G14

Over-The-Top Voltage Offset vs Temperature



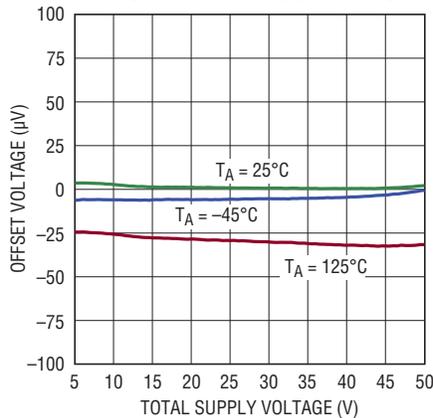
60167 G15

Voltage Offset vs Input Common Mode Voltage



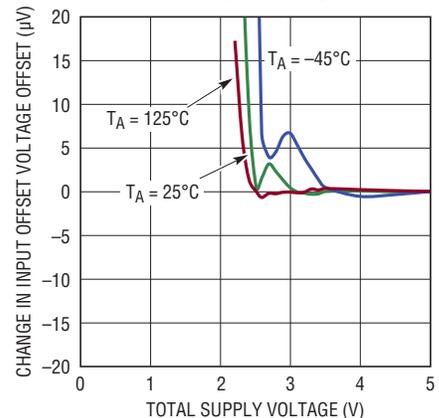
60167 G16

Voltage Offset vs Supply Voltage



60167 G17

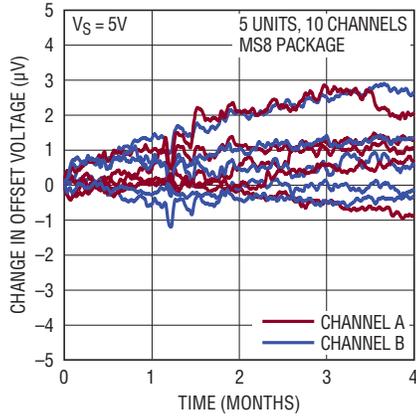
Minimum Supply Voltage



60167 G18

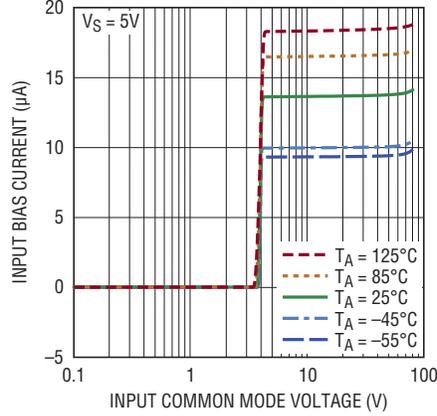
TYPICAL PERFORMANCE CHARACTERISTICS

Long Term Stability of Five Representative Units



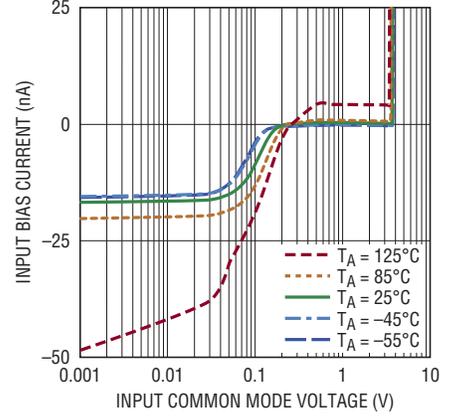
60167 G19

Input Bias Current vs Input Common Mode Voltage



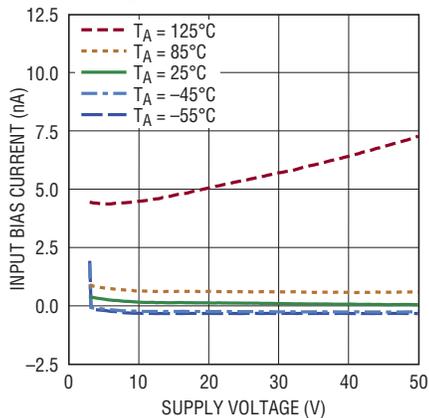
60167 G20

Input Bias Current vs Input Common Mode Voltage



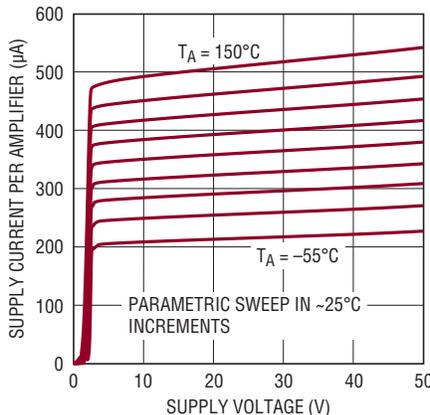
60167 G21

Input Bias Current vs Supply Voltage



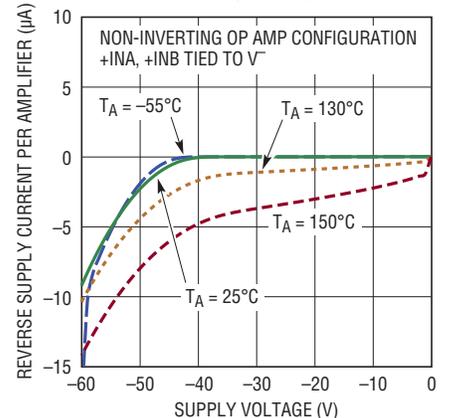
60167 G22

Supply Current vs Supply Voltage



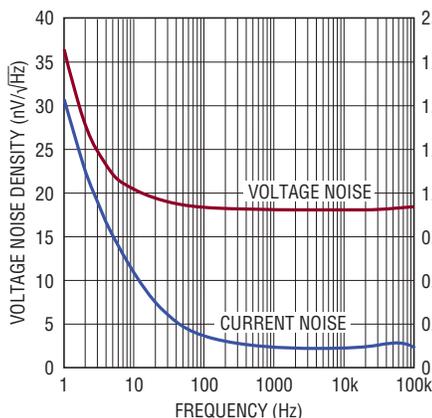
60167 G23

Reverse Supply Current vs Reverse Supply Voltage



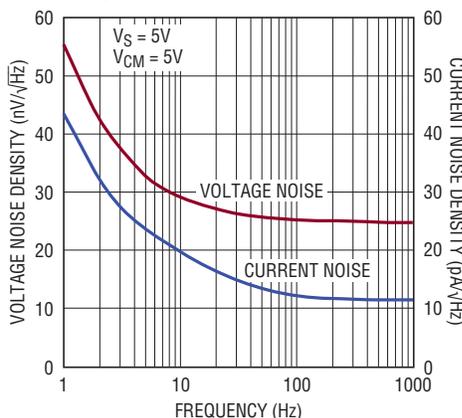
60167 G24

Noise Density vs Frequency



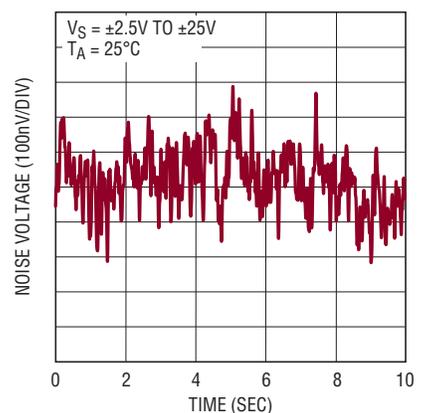
60167 G25

Over-The-Top Noise Density vs Frequency



60167 G26

0.1Hz to 10Hz Noise

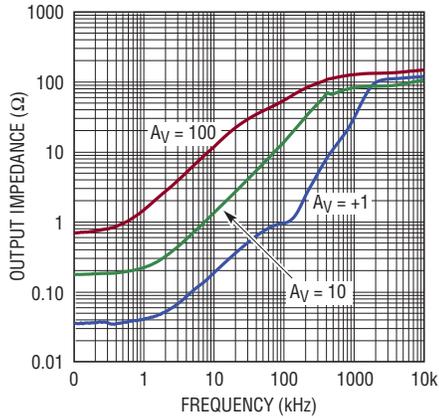


60167 G27

60167fa

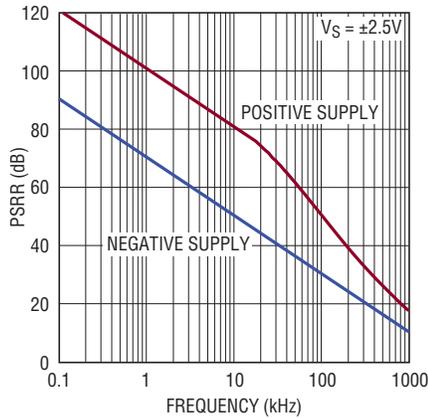
TYPICAL PERFORMANCE CHARACTERISTICS

Output Impedance vs Frequency



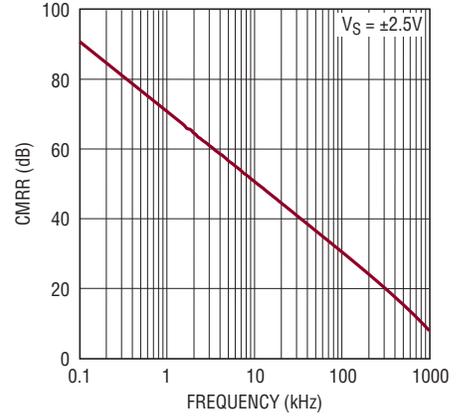
60167 G28

PSRR vs Frequency



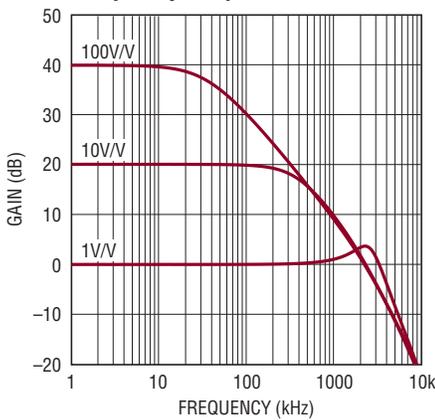
60167 G29

CMRR vs Frequency



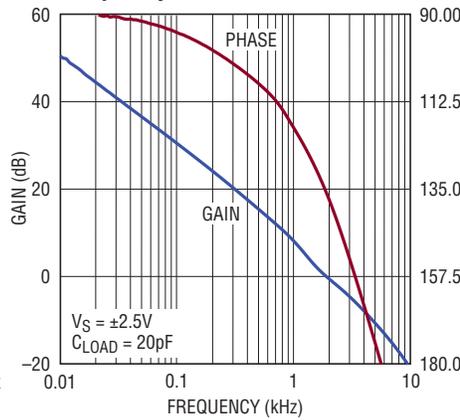
60167 G30

Closed-Loop Small Signal Frequency Response



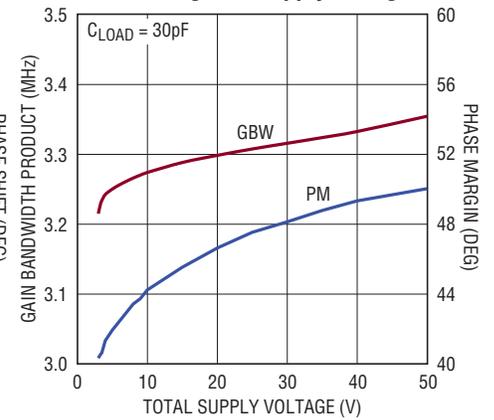
60167 G31

Gain and Phase Shift vs Frequency



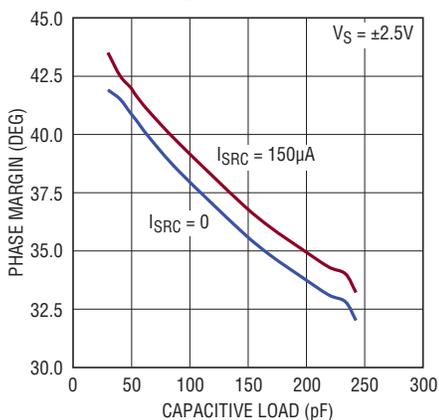
60167 G32

Gain Bandwidth Product and Phase Margin vs Supply Voltage



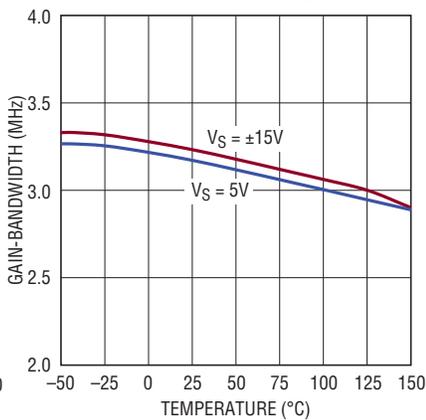
60167 G33

Phase Margin vs Capacitive Load



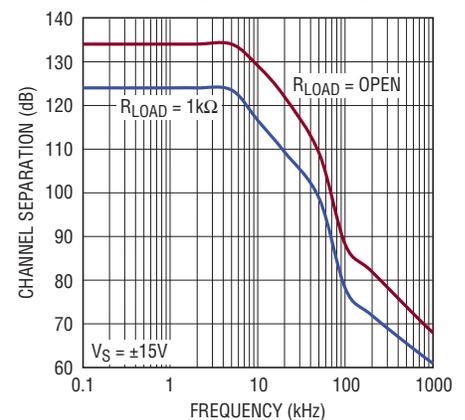
60167 G34

Gain-Bandwidth vs Temperature



60167 G35

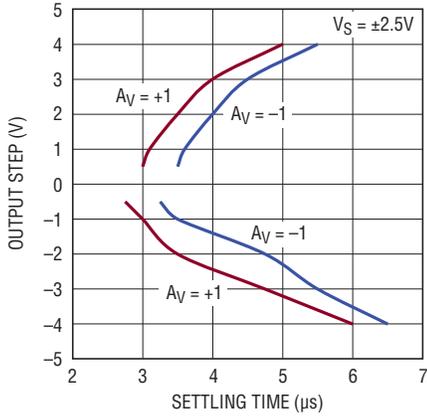
Channel Separation vs Frequency



60167fa

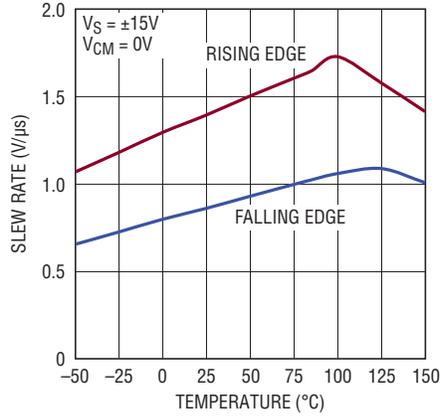
TYPICAL PERFORMANCE CHARACTERISTICS

Settling Time to 0.1% vs Output Step



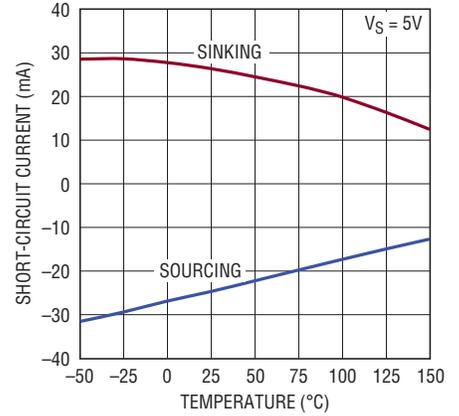
60167 G37

Slew Rate vs Temperature



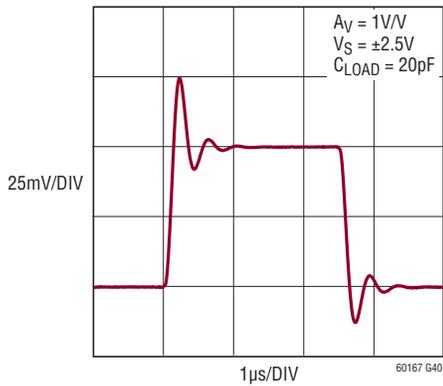
60167 G38

Short-Circuit vs Temperature



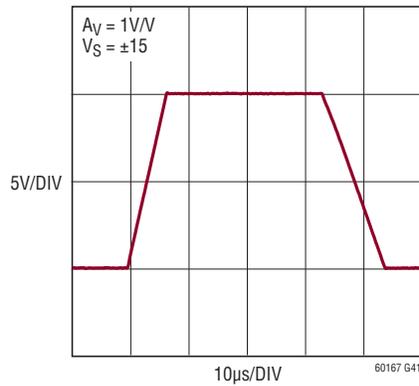
60167 G39

Small Signal Transient Response



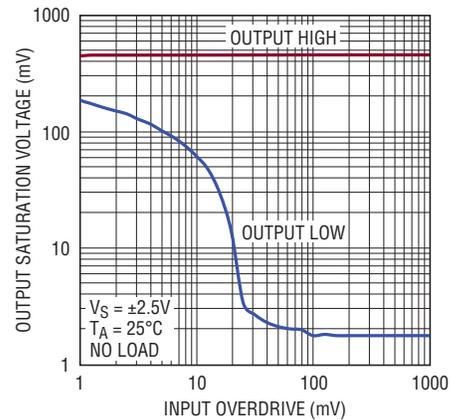
60167 G40

Large Signal Transient Response



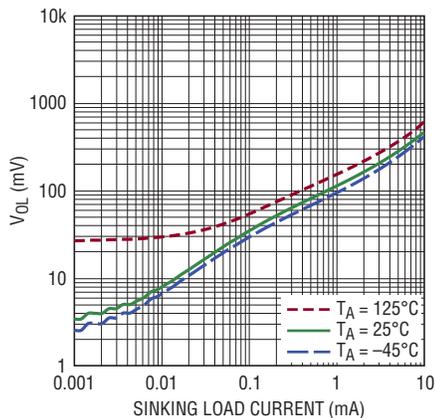
60167 G41

Output Saturation Voltage vs Input Overdrive



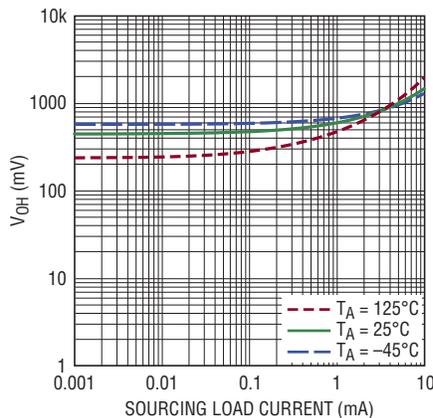
60167 G42

Output Saturation Voltage (V_{OL}) vs Load Current



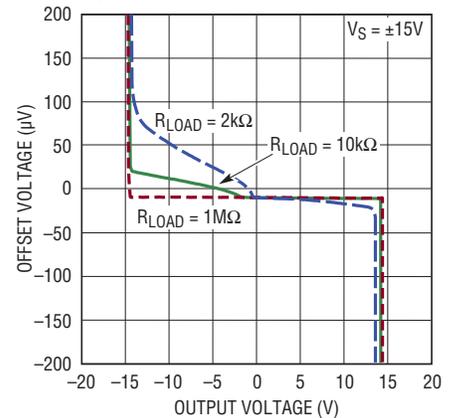
60167 G43

Output Saturation Voltage (V_{OH}) vs Load Current



60167 G44

Open-Loop Gain



60167 G45

APPLICATIONS INFORMATION

Supply Voltage

The positive supply pin of the LT6016/LT6017 should be bypassed with a small capacitor (typically 0.1 μ F) as close to the supply pins as possible. When driving heavy loads an additional 4.7 μ F electrolytic capacitor should be added. When using split supplies, the same is true for the V^- supply pin.

The LT6017 consists of two dual amplifier dice assembled in a single DFN package which share a common substrate (V^-). While the V^- pins of the quad (pins 5 and 7) must always be tied together and to the exposed pad underneath, the V^+ power supply pins (pins 16 and 18) may be supplied independently. The B and C channel amplifiers are supplied through V^+ by pin 16, and the A and D channel amplifiers are supplied by pin 18. If pin 16 and pin 18 are not tied together and are biased independently, each V^+ pin should have their own dedicated supply bypass to ground.

Shutdown

While there are no dedicated shutdown pins for the LT6016/LT6017, the amplifiers can effectively be shut down into a low power state by removing V^+ . In this condition the input bias current is typically less than 1nA with the inputs biased between V^- and 76V above V^- , and if the inputs are taken below V^- , they appear as a diode in series with 1k of resistance. The output may be pulled up to 50V above the V^+ power supply in this condition (See Figure 1). Pulling the output pin below V^- will produce unlimited current and can damage the part.

Reverse Battery

The LT6016/LT6017 are protected against reverse battery voltages up to 50V. In the event a reverse battery condition occurs, the supply current is typically less than 5 μ A (assuming the inputs are biased within a diode drop from V^-). For typical single supply applications with ground referred loads and feedback networks, no other precautions are required. If the reverse battery condition results in a negative voltage at the input pins, the current into the pin should be limited by an external resistor to less than 10mA.

Inputs

Referring to the Simplified Schematic, the LT6016/LT6017 has two input stages: a common emitter differential input stage consisting of PNP transistors Q1 and Q2 which operate when the inputs are biased between V^- and 1.5V below V^+ , and a common base input stage consisting of PNP transistors Q3 to Q6 which operate when the common mode input is biased greater than $V^+ - 1.5V$. This results in two distinct operating regions as shown in Figure 2.

For common mode input voltages approximately 1.5V or more below the V^+ supply (Q1 and Q2 active), the common emitter PNP input stage is active and the input bias current is typically under $\pm 2nA$. When the common mode input is within approximately 1V of the V^+ supply or higher

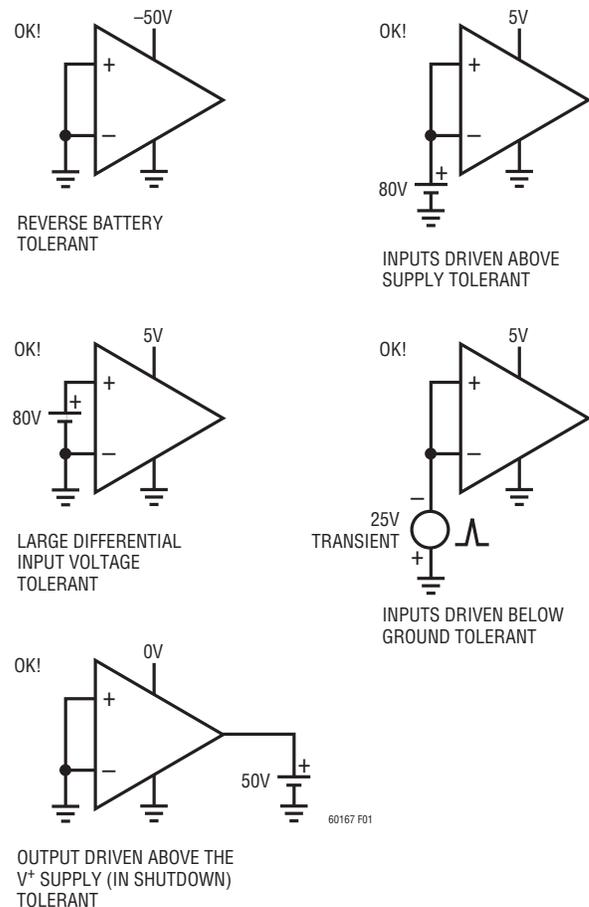


Figure 1. LT6016/LT6017 Fault Tolerant Conditions

APPLICATIONS INFORMATION

(Over-The-Top operation), Q9 begins to turn on diverting bias current away from the common emitter differential input pair to the current mirror consisting of Q11 and Q12. The current from Q12 will bias the common base differential input pair consisting of Q3 to Q6. Because the Over-The-Top input pair is operating in a common base configuration, the input bias current will increase to about, 14 μ A. Both input stages have their voltage offsets trimmed tightly and are specified in the Electrical Characteristics table.

The inputs are protected against temporary excursions to as much as 25V below V^- by internal 1k resistor in series with each input and a diode from the input to the negative supply. Adding additional external series resistance will extend the protection beyond 25V below V^- . The input stage of the LT6016/LT6017 incorporates phase reversal protection to prevent the output from phase reversing for inputs below V^- .

There are no clamping diodes between the inputs. The inputs may be over-driven differentially to 80V without damage, or without drawing appreciable input current. Figure 1 summarizes the kind of faults that may be applied to the LT6016/LT6017 without damage.

Over-The-Top Operation Considerations

When the input common mode of the LT6016/LT6017 is biased near or above the V^+ supply, the amplifier is said to be operating in the Over-The-Top configuration. The differential input pair which control amplifier operation is common base pair Q3 to Q6 (refer to the Simplified Schematic). If the input common mode is biased between V^- and approximately 1.5V below V^+ , the amplifier is said to be operating in the normal configuration. The differential input pair which control amplifier operation is common emitter pair Q1 and Q2.

A plot of the Over-The-Top Transition region vs Temperature (the region between normal operation and Over-The-Top operation) on a 5V single supply is shown in Figure 2.

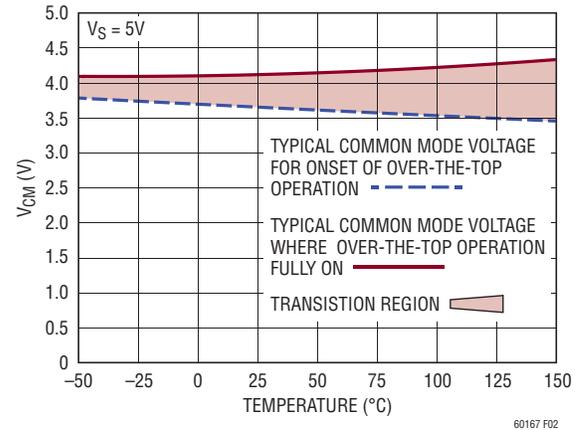


Figure 2. LT6016/LT6017 Over-The-Top Transition Region vs Temperature

Some implications should be understood about Over-The-Top operation. The first, and most obvious is the input bias currents change from under ± 2 nA in normal operation to 14 μ A in Over-The-Top operation as the input stage transitions from common emitter to common base. Even though the Over-The-Top input bias currents run around 14 μ A, they are very well matched and their offset is typically under ± 100 nA.

The second and more subtle change to amplifier operation is the differential input impedance which decreases from 1M Ω in normal operation, to approximately 3.7k Ω in Over-The-Top operation (specified as R_{IN} in the Electrical Characteristics table). This resistance appears across the summing nodes in Over-The-Top operation and is due to the common base input stage configuration. Its value is easily derived from the specified input bias current flowing into the op amp inputs and is equal to $2 \cdot k \cdot T / (q \cdot I_b)$ (k -Boltzmann's constant, T – operating temperature, I_b -operating input bias current of the amplifier in the Over-The-Top region). And because the inputs are biased proportional to absolute temperature, it is relatively constant with temperature. The user may think this effective resistance is relatively harmless because it appears across the summing nodes which are forced

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to 0V differential by feedback action of the amplifier. However, depending on the configuration of the feedback around the amplifier, this input resistance can boost noise gain, lower overall amplifier loop gain and closed loop bandwidth, raise output noise, with one benevolent effect in increasing amplifier stability.

In the normal mode of operation (where $V^- < V_{CM} < V^+$ $-1.5V$), R_{IN} is typically large compared to the value of the input resistor used, and R_{IN} can be ignored (refer to Figure 3). In this case the noise gain is defined by the equation:

$$\text{NOISE GAIN} \approx 1 + \frac{R_F}{R_I}$$

However, when the amplifier transitions into Over-The-Top mode with the input common mode biased near or above the V^+ supply, R_{IN} should be considered. The noise gain of the amplifier changes to:

$$\text{NOISE GAIN} = 1 + \frac{R_F}{R_I \parallel (R_{IN} + R_I \parallel R_F)}$$

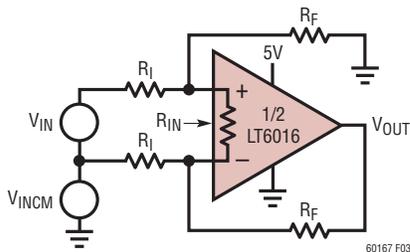


Figure 3. Difference Amplifier Configured for Both Normal and Over-The-Top Operation

While it is true that the DC closed loop gain will remain mostly unaffected ($= \frac{R_F}{R_I}$), the loop gain of the amplifier

has decreased from $\frac{A_{OL}}{1 + \frac{R_F}{R_I}}$ to $\frac{A_{OL}}{1 + \frac{R_F}{R_I \parallel (R_{IN} + R_I \parallel R_F)}}$

Likewise the closed loop bandwidth of the amplifier will change going from normal mode operation to Over-The-Top operation:

$$\text{Normal mode: } BW_{\text{CLOSED-LOOP}} \approx \frac{GBW}{1 + \frac{R_F}{R_I}}$$

Over-The-Top mode:

$$BW_{\text{CLOSED-LOOP}} \approx \frac{GBW}{1 + \frac{R_F}{R_I \parallel (R_{IN} + R_I \parallel R_F)}}$$

And output noise is negatively impacted going from normal mode to Over-The-Top:

Normal mode: (neglecting resistor noise)

$$e_{no} \approx e_{ni} \cdot \left(1 + \frac{R_F}{R_I} \right)$$

Over-The-Top mode: (neglecting resistor noise)

$$e_{no} \approx e_{ni} \cdot \left(1 + \frac{R_F}{R_I \parallel (R_{IN} + R_I \parallel R_F)} \right)$$

Output

The output of the LT6016/LT6017 can swing within a Schottky diode drop ($\sim 0.4V$) of the V^+ supply, and within 5mV of the negative supply with no load. The output is capable of sourcing and sinking approximately 25mA.

The LT6016/LT6017 are internally compensated to drive at least 200pF of capacitance under any output loading conditions. For larger capacitive loads, a 0.22 μ F capacitor in series with a 150 Ω resistor between the output and ground will compensate these amplifiers to drive capacitive loads greater than 200pF.

APPLICATIONS INFORMATION

Distortion

There are two main contributors of distortion in op amps: output crossover distortion as the output transitions from sourcing to sinking current and distortion caused by nonlinear common mode rejection. If the op amp is operating in an inverting configuration there is no common mode induced distortion. If the op amp is operating in the noninverting configuration within the normal input common mode range (V^- to $V^+ - 1.5V$) the CMRR is very good, typically over 120dB. When the LT6016 transitions input stages going from the normal input stage to the Over-The-Top input stage or vice-versa, there will be a significant degradation in linearity due to the change in input circuitry.

Lower load resistance increases distortion due to a net decrease in loop gain, and greater voltage swings internal to the amp necessary to drive the load, but has no effect on the input stage transition distortion. The lowest distortion can be achieved with the LT6016/LT6017 sourcing in class-A operation in an inverting configuration, with the input common mode biased mid-way between the supplies.

Power Dissipation Considerations

Because of the ability of the LT6016/LT6017 to operate on power supplies up to $\pm 25V$ and to drive heavy loads, there is a need to ensure the die junction temperature does not exceed $150^\circ C$. The LT6016 is housed in an 8-lead MSOP package ($\theta_{JA} = 273^\circ C/W$). The LT6017 is housed in a 22 pin leadless DFN package (DJC22, $\theta_{JA} = 31.8^\circ C/W$).

In general, the die junction temperature (T_J) can be estimated from the ambient temperature T_A , and the device power dissipation P_D :

$$T_J = T_A + P_D \cdot \theta_{JA}$$

The power dissipation in the IC is a function of supply voltage and load resistance. For a given supply voltage, the worst-case power dissipation $P_{D(MAX)}$ occurs at the maximum supply current with the output voltage at half of either supply voltage (or the maximum swing is less than one-half the supply voltage). $P_{D(MAX)}$ is given by:

$$P_{D(MAX)} = (V_S \cdot I_{S(MAX)}) + (V_S/2)^2/R_{LOAD}$$

Example: An LT6016 in a MSOP package mounted on a PC board has a thermal resistance of $273^\circ C/W$. Operating on $\pm 25V$ supplies with both amplifiers simultaneously driving $2.5k\Omega$ loads, the worst-case IC power dissipation for the given load occurs when driving $12.5V_{PEAK}$ and is given by:

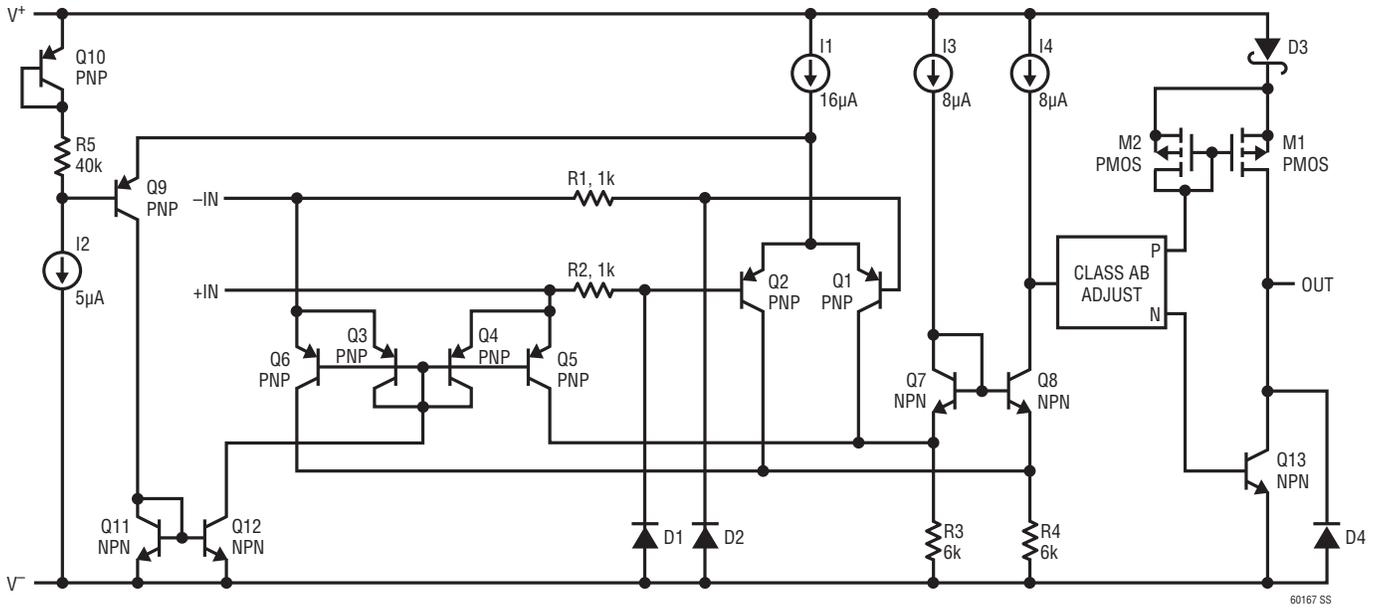
$$P_{D(MAX)} = 2 \cdot 50 \cdot 0.6mA + 2 \cdot (12.5)^2/2500 = 0.185W$$

With a thermal resistance of $273^\circ C/W$, the die temperature will experience approximately a $50^\circ C$ rise above ambient. This implies the maximum ambient temperature the LT6016 should ever operate under the assumed conditions:

$$T_A = 150^\circ C - 50^\circ C = 100^\circ C$$

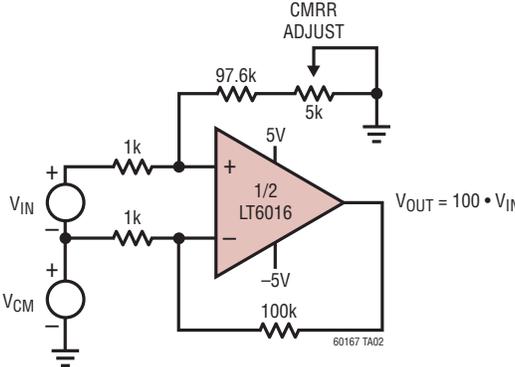
To operate to higher ambient temperatures, use two channels of the LT6017 quad which has lower thermal resistance $\theta_{JA} = 31.8^\circ C/W$, and an exposed pad which may be soldered down to a copper plane (connected to V^-) to further lower the thermal resistance below $\theta_{JA} = 31.8^\circ C/W$.

SIMPLIFIED SCHEMATIC



TYPICAL APPLICATIONS

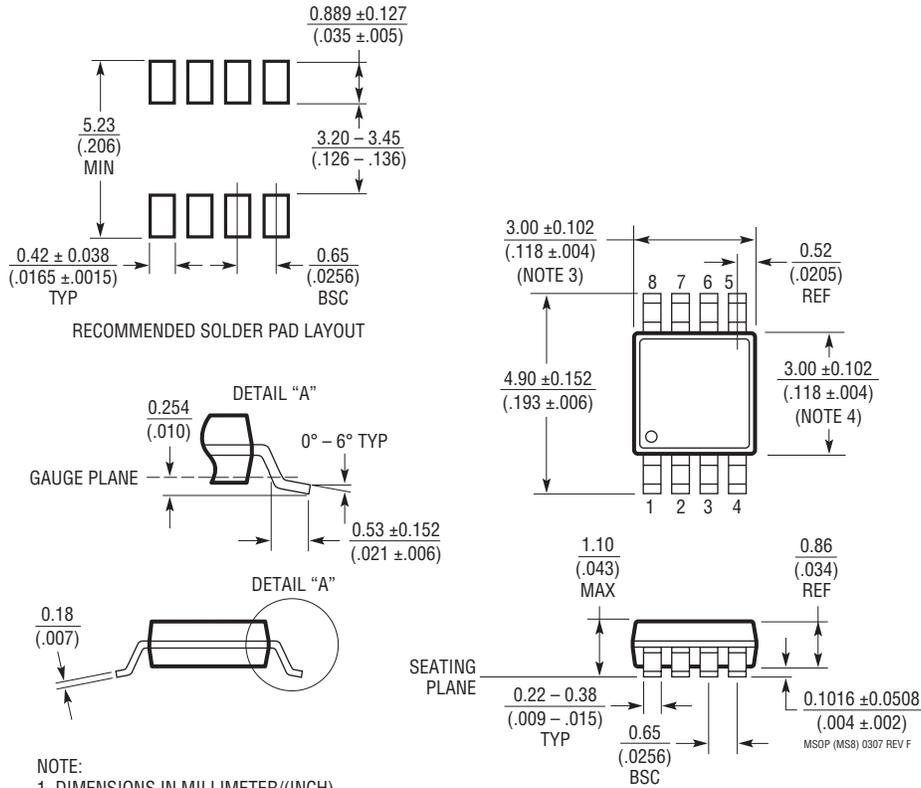
Gain of 100 High Voltage Difference Amplifier with -5V/75V Common Mode Range



PACKAGE DESCRIPTION

Please refer to <http://www.linear.com/designtools/packaging/> for the most recent package drawings.

MS8 Package 8-Lead Plastic MSOP (Reference LTC DWG # 05-08-1660 Rev F)

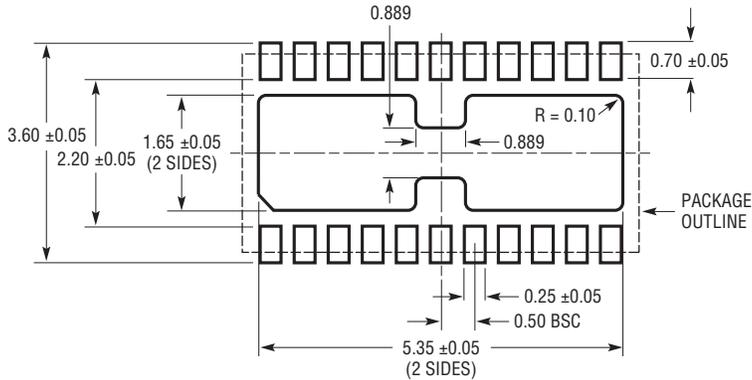


- NOTE:
1. DIMENSIONS IN MILLIMETER/(INCH)
 2. DRAWING NOT TO SCALE
 3. DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
 4. DIMENSION DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
INTERLEAD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
 5. LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.102mm (.004") MAX

PACKAGE DESCRIPTION

Please refer to <http://www.linear.com/designtools/packaging/> for the most recent package drawings.

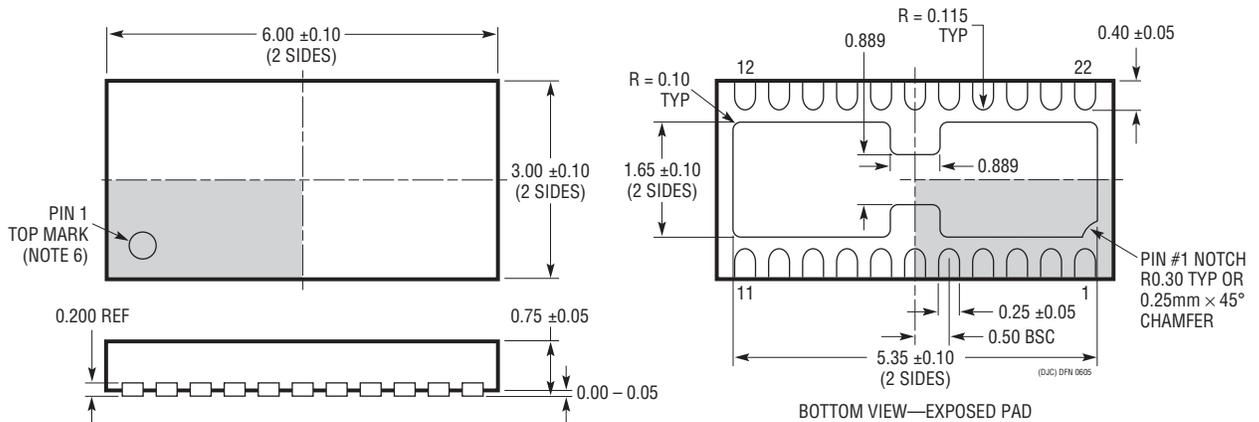
DJC Package
22-Lead Plastic DFN (6mm × 3mm)
 (Reference LTC DWG # 05-08-1714 Rev 0)



RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS

NOTE:

1. DIMENSIONS ARE IN MILLIMETERS
2. APPLY SOLDER MASK TO AREAS THAT ARE NOT SOLDERED
3. DRAWING IS NOT TO SCALE



NOTE:

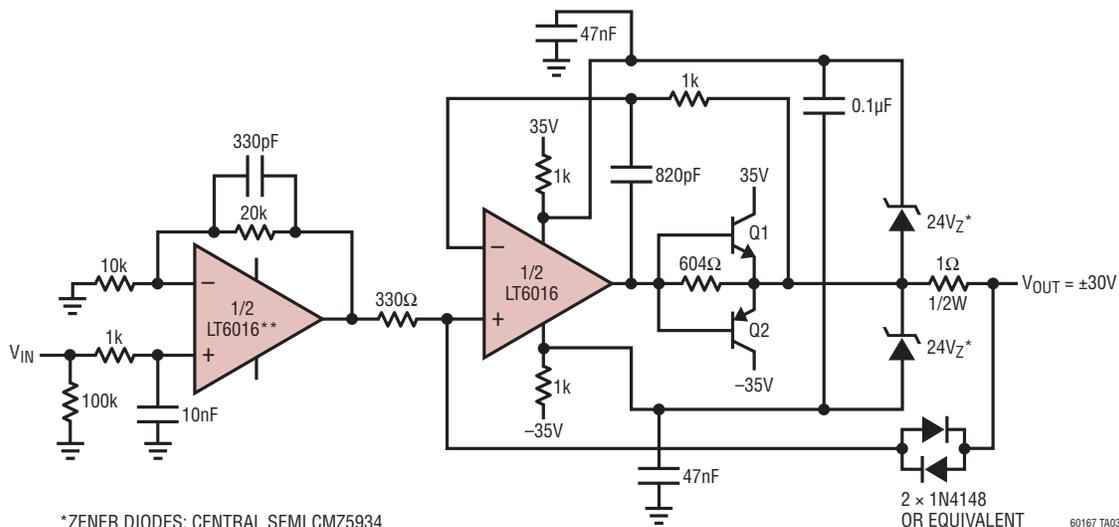
1. DRAWING PROPOSED TO BE MADE VARIATION OF VERSION (WXXX) IN JEDEC PACKAGE OUTLINE MO-229
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON TOP AND BOTTOM OF PACKAGE

REVISION HISTORY

REV	DATE	DESCRIPTION	PAGE NUMBER
A	01/13	Corrected Block Diagram Q7 and Q8	17

TYPICAL APPLICATION

Extended Supply Current Boosted Gain of Three Amplifier Drives 100Ω Load to ±30V, with 600mA Current Limit



*ZENER DIODES: CENTRAL SEMI CMZ5934
 Q1, Q2: ON-SEMI D44VH10 NPN, D45VH10 PNP WITH HEAT SINK
 **BOTH HALVES OF LT6016 ON SAME SUPPLY

2 × 1N4148 OR EQUIVALENT
 60167 TA03

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LT1490A/LT1491A	Dual and Quad Micropower Rail-to-Rail Input and Output Op amp	Over-The-Top Inputs, 50μA/Amplifier, Reverse Battery Protection to 18V
LT1638/LT1639	1.2MHz, 0.4V/μs Over-The-Top Rail-to-Rail Input and Output Op Amp	Over-The-Top Inputs, 230μA/Amplifier, 1.2MHz GBW, 0.4V/μs Slew Rate
LT1494/LT1495/LT1496	1.5μA Max, Single, Dual, and Quad, Over-The-Top Precision Rail-to-Rail Input and Output Op Amps	Over-The-Top Inputs, 1.5μA/Amplifier, 375μV Voltage Offset
LT1112/LT1114	Dual/Quad Low Power Precision, pA Input Op Amp	60μV Offset Voltage, 400 μA/Amplifier
LT1013/LT1014	Dual/Quad Precision Op Amp	150μV Offset Voltage, 500 μA/Amplifier