GENERAL DESCRIPTION

The XRT86VL34 is a four-channel 1.544 Mbit/s or 2.048 Mbit/s DS1/E1/J1 framer and LIU integrated solution featuring R^3 technology (Relayless, Reconfigurable, Redundancy). The physical interface is optimized with internal impedance, and with the patented pad structure, the XRT86VL34 provides protection from power failures and hot swapping.

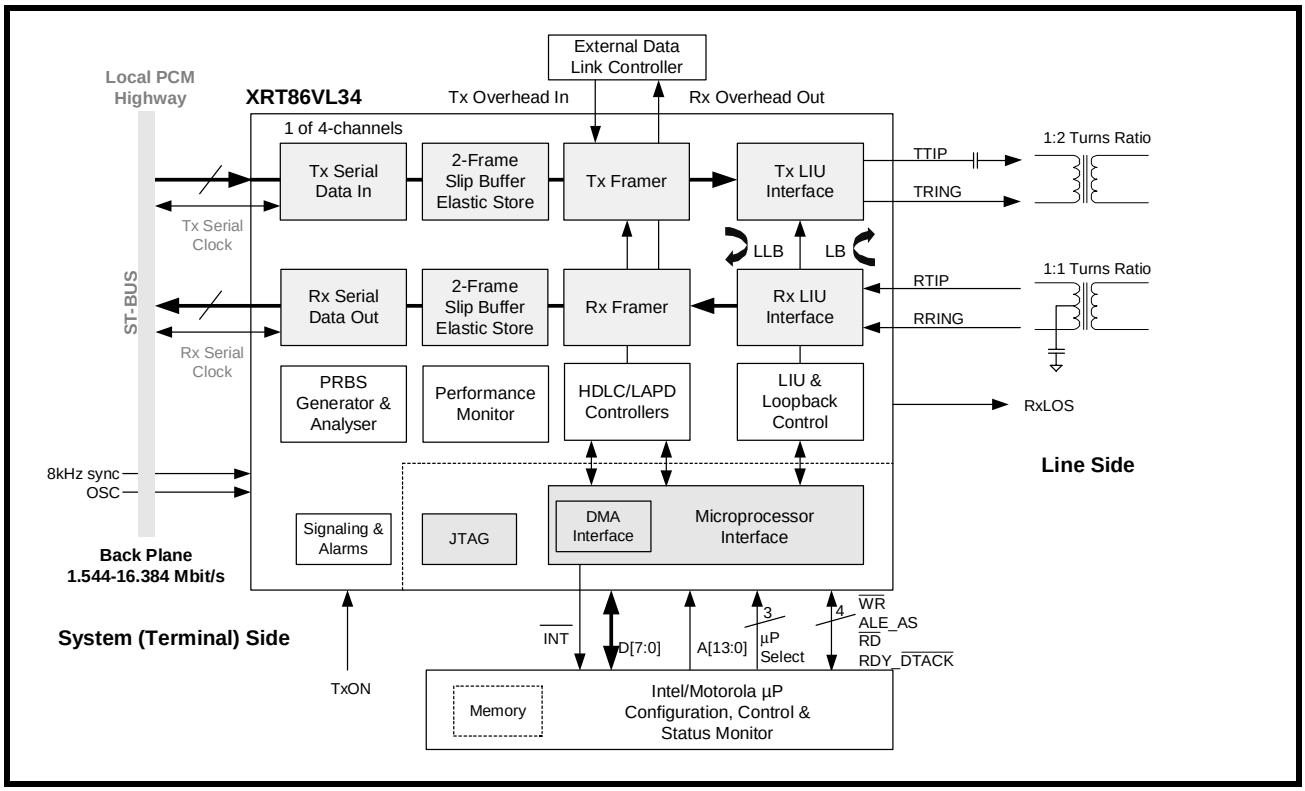
The XRT86VL34 contains an integrated DS1/E1/J1 framer and LIU which provide DS1/E1/J1 framing and error accumulation in accordance with ANSI/ITU_T specifications. Each framer has its own framing synchronizer and transmit-receive slip buffers. The slip buffers can be independently enabled or disabled as required and can be configured to frame to the common DS1/E1/J1 signal formats.

Each Framer block contains its own Transmit and Receive T1/E1/J1 Framing function. There are 3 Transmit HDLC controllers per channel which encapsulate contents of the Transmit HDLC buffers into LAPD Message frames. There are 3 Receive HDLC controllers per channel which extract the payload content of Receive LAPD Message frames from the incoming T1/E1/J1 data stream and write the contents into the Receive HDLC buffers. Each framer also contains a Transmit and Overhead Data Input port, which permits Data Link Terminal Equipment direct access to the outbound T1/E1/J1 frames. Likewise, a Receive Overhead output data port permits Data Link Terminal Equipment direct access to the Data Link bits of the inbound T1/E1/J1 frames.

The XRT86VL34 fully meets all of the latest T1/E1/J1 specifications: ANSI T1/E1.107-1988, ANSI T1/E1.403-1995, ANSI T1/E1.231-1993, ANSI T1/E1.408-1990, AT&T TR 62411 (12-90) TR54016, and ITU G-703, G.704, G706 and G.733, AT&T Pub. 43801, and ETS 300 011, 300 233, JT G.703, JT G.704, JT G706, I.431. Extensive test and diagnostic functions include Loop-backs, Boundary scan, Pseudo Random bit sequence (PRBS) test pattern generation, Performance Monitor, Bit Error Rate (BER) meter, forced error insertion, and LAPD unchannelized data payload processing according to ITU-T standard Q.921.

Applications and Features (next page)

FIGURE 1. XRT86VL34 4-CHANNEL DS1 (T1/E1/J1) FRAMER/LIU COMBO



APPLICATIONS

- High-Density T1/E1/J1 interfaces for Multiplexers, Switches, LAN Routers and Digital Modems
- SONET/SDH terminal or Add/Drop multiplexers (ADMs)
- T1/E1/J1 add/drop multiplexers (MUX)
- Channel Service Units (CSUs): T1/E1/J1 and Fractional T1/E1/J1
- Digital Access Cross-connect System (DACs)
- Digital Cross-connect Systems (DCS)
- Frame Relay Switches and Access Devices (FRADS)
- ISDN Primary Rate Interfaces (PRA)
- PBXs and PCM channel bank
- T3 channelized access concentrators and M13 MUX
- Wireless base stations
- ATM equipment with integrated DS1 interfaces
- Multichannel DS1 Test Equipment
- T1/E1/J1 Performance Monitoring
- Voice over packet gateways
- Routers

FEATURES

- Four independent, full duplex DS1 Tx and Rx Framer/LIUs
- Two 512-bit (two-frame) elastic store, PCM frame slip buffers (FIFO) on TX and Rx provide up to 8.192 MHz asynchronous back plane connections with jitter and wander attenuation
- Supports input PCM and signaling data at 1.544, 2.048, 4.096 and 8.192 Mbits. Also supports 4-channel multiplexed 12.352/16.384 (HMVIP/H.100) Mbit/s on the back plane bus
- Programmable output clocks for Fractional T1/E1/J1
- Supports Channel Associated Signaling (CAS)
- Supports Common Channel Signalling (CCS)
- Supports ISDN Primary Rate Interface (ISDN PRI) signaling
- Extracts and inserts robbed bit signaling (RBS)
- 3 Integrated HDLC controllers per channel for transmit and receive, each controller having two 96-byte buffers (buffer 0 / buffer 1)
- HDLC Controllers Support SS7
- Timeslot assignable HDLC
- V5.1 or V5.2 Interface
- Automatic Performance Report Generation (PMON Status) can be inserted into the transmit LAPD interface every 1 second or for a single transmission
- Alarm Indication Signal with Customer Installation signature (AIS-CI)
- Remote Alarm Indication with Customer Installation (RAI-CI)
- Gapped Clock interface mode for Transmit and Receive.

- Intel/Motorola and Power PC interfaces for configuration, control and status monitoring
- Parallel search algorithm for fast frame synchronization
- Wide choice of T1 framing structures: SF/D4, ESF, SLC®96, T1DM and N-Frame (non-signaling)
- Direct access to D and E channels for fast transmission of data link information
- PRBS, QRSS, and Network Loop Code generation and detection
- Programmable Interrupt output pin
- Supports programmed I/O and DMA modes of Read-Write access
- Each framer block encodes and decodes the T1/E1/J1 Frame serial data
- Detects and forces Red (SAI), Yellow (RAI) and Blue (AIS) Alarms
- Detects OOF, LOF, LOS errors and COFA conditions
- Loopbacks: Local (LLB) and Line remote (LB)
- Facilitates Inverse Multiplexing for ATM
- Performance monitor with one second polling
- Boundary scan (IEEE 1149.1) JTAG test port
- Accepts external 8kHz Sync reference
- 1.8V Inner Core
- 3.3V CMOS operation with 5V tolerant inputs
- 225-pin PBGA package with -40°C to +85°C operation

ORDERING INFORMATION

PART NUMBER	PACKAGE	OPERATING TEMPERATURE RANGE
XRT86VL34IB	225 Plastic Ball Grid Array	-40°C to +85°C

LIST OF PARAGRAPHS

LIST OF TABLES

LIST OF FIGURES

TABLE 1: LIST BY PIN NUMBER

PIN	PIN NAME
A1	GNDPLL
A2	AVDD18
A3	E1MCLKnOUT
A4	MCLKIN
A5	VSS
A6	TRST
A7	RXSERCLK0
A8	RXCHCLK0
A9	RXOHCLK0
A10	TXMSYNC0
A11	TXOHCLK0
A12	TXSERCLK0
A13	TXCHCLK0
A14	TXCHN0_3
A15	RXSER1
A16	RXCHCLK1
A17	RXCHN1_2
A18	RXSYNC1
B1	VDDPLL18
B2	JTAG_Ring
B3	AGND
B4	T1MCLKnOUT
B5	aTESTMODE
B6	TDI
B7	RXLOS0
B8	DVDD18
B9	RXCHN0_2
B10	RXCHN0_4
B11	TESTMODE
B12	TXCHN0_0
B13	TXCHN0_2
B14	VSS
B15	RXCHN1_1
B16	RXOH1
B17	RXCASYNC1
B18	TXSYNC1
C1	GNDPLL
C2	VDDPLL18
C3	JTAG_Tip
C4	DVDD18
C5	DGND
C6	TMS
C7	TCLK
C8	RXCRCSYNC0
C9	RXCHN0_1
C10	RXCHN0_3
C11	RXOH0
C12	TXOH0
C13	RXCRCSYNC1
C14	TXCHN0_4
C15	TXCHCLK1
C16	VSS
C17	TXMSYNC1
C18	RXLOS1
D1	GNDPLL
D2	VDDPLL18
D3	VDDPLL18
D4	GNDPLL
D5	TDO
D6	RXSER0
D7	RXCHN0_0
D8	RXSYNC0
D9	TXSYNC0
D10	RXCASYNC0
D11	TXSER0
D12	TXCHN0_1
D13	RXSERCLK1
D14	RXCHN1_0
D15	RXSERCLK2
D16	VDD
D17	RXOHCLK1
D18	RXCHN1_3
E1	RTIP0
E2	RGND0
E3	RVDD0
E4	TTIP0
E5	ANALOG
E15	TXOHCLK1
E16	TXSER1
E17	RXCHN1_4
E18	TXSERCLK1
F1	RRING0
F2	TGND0
F3	TVDD0
F4	TRING0
F15	TXOH1
F16	TXCHN1_0
F17	TXCHN1_1
F18	RXSYNC2
G1	RTIP1
G2	RGND1
G3	RVDD1
G4	TTIP1
G15	RXCHN2_1
G16	RXLOS2
G17	TXCHN1_2
G18	TXCHN1_3
H1	RRING1
H2	TGND1
H3	TVDD1
H4	TRING1
H15	RXCASYNC2
H16	RXCHN2_0
H17	RXCHCLK2
H18	TXCHN1_4
J1	RTIP2
J2	RGND2
J3	RVDD2
J4	TTIP2
J15	TXSERCLK2
J16	DVDD18
J17	RXCRCSYNC2
J18	RXSER2
K1	RRING2
K2	TGND2
K3	TVDD2
K4	TRING2
K15	RXOH2
K16	RXCHN2_4
K17	RXOHCLK2
K18	RXCHN2_2
L1	RTIP3
L2	RGND3
L3	RVDD3
L4	TTIP3
L15	TXSYNC2
L16	RXCHN2_3
L17	TXMSYNC2
L18	TXSER2
M1	RRING3
M2	TGND3
M3	TVDD3
M4	TRING3
M15	VSS

PIN	PIN NAME
M16	VSS
M17	TXCHN2_1
M18	TXCHN2_0
N1	TxON
N2	LOP
N3	RXTSEL
N4	8KEXTOSC
N15	TXCHN2_4
N16	TXCHN2_3
N17	TXCHCLK2
N18	TXOHCLK2
P1	$\overline{\text{RESET}}$
P2	E1OSCCLK
P3	VDD
P4	T1OSCCLK
P15	TXOH2
P16	RXSYNC3
P17	RXCHNCLK3
P18	RXOH3
R1	$\overline{\text{REQ0}}$
R2	8KSYNC
R3	$\overline{\text{REQ1}}$
R4	VSS
R5	ADDR2
R6	ADDR6
R7	ADDR10
R8	$\overline{\text{INT}}$
R9	ADDR11
R10	ADDR12
R11	DATA7
R12	TXMSYNC3
R13	DVDD18
R14	TXOH3
R15	VDD

PIN	PIN NAME
R16	RXOHCLK3
R17	RXCRCSYNC3
R18	RXCHN3_0
T1	fADDR
T2	$\overline{\text{ACK0}}$
T3	$\overline{\text{RDY}}$
T4	DATA0
T5	VSS
T6	ADDR3
T7	ADDR7
T8	PTYPE2
T9	VDD
T10	DATA4
T11	TXCHN3_4
T12	TXCHN3_2
T13	TXCHN3_0
T14	RXCHN3_3
T15	RXCHN3_2
T16	TXCHN2_2
T17	RXSERCLK3
T18	RXCASYNC3
U1	iADDR
U2	$\overline{\text{ACK1}}$
U3	DATA1
U4	$\overline{\text{DBEN}}$
U5	ADDR0
U6	ADDR4
U7	DVDD18
U8	ALE
U9	ADDR9
U10	$\overline{\text{BLAST}}$
U11	DATA6
U12	TXCHN3_3
U13	TXCHN3_1

PIN	PIN NAME
U14	RXCHN3_4
U15	TXSYNC3
U16	VSS
U17	RXSER3
U18	RLOS3
V1	PCLK
V2	PTYPE0
V3	$\overline{\text{RD}}$
V4	PTYPE1
V5	ADDR1
V6	ADDR5
V7	ADDR8
V8	DATA2
V9	DATA3
V10	DATA5
V11	ADDR13
V12	$\overline{\text{WR}}$
V13	$\overline{\text{CS}}$
V14	TXSER3
V15	TXSERCLK3
V16	TXOHCLK3
V17	TXCHCLK3
V18	RXCHN3_1

1.0 PIN DESCRIPTIONS

There are five types of pins defined throughout this pin description and the corresponding symbol is presented in table below. The per-channel pin is indicated by the channel number or the letter 'n' which is appended at the end of the signal name, for example, TxSERn, where "n" indicates channels 0 to 3. All output pins are "tri-stated" upon hardware RESET

TABLE 2:

SYMBOL	PIN TYPE
I	Input
O	Output
I/O	Bidirectional
GND	Ground
PWR	Power

The structure of the pin description is divided into twelve groups, as presented in the table below

TABLE 3: PIN DESCRIPTION STRUCTURE

SECTION	PAGE NUMBER
Transmit System Side Interface	page 7
Transmit Overhead Interface	page 15
Receive Overhead Interface	page 17
Receive System Side Interface	page 18
Receive Line Interface	page 26
Transmit Line Interface	page 28
Timing Interface	page 28
JTAG Interface	page 30
Microprocessor Interface	page 31
Power Pins (3.3V)	page 39
Power Pins (1.8V)	page 39
Ground Pins	page 40

TRANSMIT SYSTEM SIDE INTERFACE

SIGNAL NAME	BALL#	TYPE	OUTPUT DRIVE(MA)	DESCRIPTION
TxSER0/ TxPOS0 TxSER1/ TxPOS1 TxSER2/ TxPOS2 TxSER3/ TxPOS3	D11 E16 L18 V14	I	-	**Transmit Serial Data Input (TxSERn)/Transmit Positive Digital Input (TxPOSn):** The exact function of these pins depends on the mode of operation selected, as described below. **DS1/E1 Mode - TxSERn** These pins function as the transmit serial data input on the system side interface, which are latched on the rising edge of the TxSERCLKn pin. Any payload data applied to this pin will be inserted into an outbound DS1/E1 frame and output to the line. In DS1 mode, the framing alignment bits, facility data link bits, CRC-6 bits, and signaling information can also be inserted from this input pin if configured appropriately. In E1 mode, all data intended to be transported via Time Slots 1 through 15 and Time slots 17 through 31 must be applied to this input pin. Data intended for Time Slots 0 and 16 can also be applied to this input pin If configured accordingly. **DS1 or E1 High-Speed Multiplexed Mode* - TxSERn** In this mode, these pins are used as the high-speed multiplexed data input pin on the system side. High-speed multiplexed data of channels 0-3 must be applied to TxSER0 in a byte or bit-interleaved way. The framer latches in the multiplexed data on TxSER0 using TxMSYNC/TxINCLK and demultiplexes this data into 4 serial streams. The LIU block will then output the data to the line interface using TxSERCLKn. **DS1 or E1 Framer Bypass Mode - TxPOSn** In this mode, TxSERn is used for the positive digital input pin (TxPOSn) to the LIU. ***NOTE:*** 1. **High-speed multiplexed modes include (For T1/E1) 16.384MHz HMVIP, H.100, Bit-multiplexed modes, and (For T1 only) 12.352MHz Bit-multiplexed mode.* 2. *In DS1 high-speed modes, the DS-0 data is mapped into an E1 frame by ignoring every fourth time slot (don't care).* 3. *These 8 pins are internally pulled "High" for each channel.*

TRANSMIT SYSTEM SIDE INTERFACE

SIGNAL NAME	BALL#	TYPE	OUTPUT DRIVE(mA)	DESCRIPTION
TxSERCLK0/ TxLINECLK0 TxSERCLK1/ TxLINECLK1 TxSERCLK2/ TxLINECLK2 TxSERCLK3/ TxLINECLK3	A12 E18 J15 V15	I/O	12	**Transmit Serial Clock (TxSERCLKn)/Transmit Line Clock (TxSERCLKn):** The exact function of these pins depends on the mode of operation selected, as described below. **In Base-Rate Mode (1.544MHz/2.048MHz) - TxSERCLKn:** This clock signal is used by the transmit serial interface to latch the contents on the TxSERn pins into the T1/E1 framer on the rising edge of TxSERCLKn. These pins can be configured as input or output as described below. **When TxSERCLKn is configured as Input:** These pins will be inputs if the TxSERCLK is chosen as the timing source for the transmit framer. Users must provide a 1.544MHz clock rate to this input pin for T1 mode of operation, and 2.048MHz clock rate in E1 mode. **When TxSERCLKn is configured as Output:** These pins will be outputs if either the recovered line clock or the MCLK PLL is chosen as the timing source for the T1/E1 transmit framer. The transmit framer will output a 1.544MHz clock rate in T1 mode of operation, and a 2.048MHz clock rate in E1 mode. **DS1/E1 High-Speed Backplane Modes* - TxSERCLKn as INPUT ONLY** In this mode, TxSERCLK is an optional clock signal input which is used as the timing source for the transmit line interface, and is only required if TxSERCLK is chosen as the timing source for the transmit framer. If TxSERCLK is chosen as the timing source, system equipment should provide 1.544MHz (For T1 mode) or 2.048MHz (For E1 mode) to the TxSERCLKn pins on each channel. TxSERCLK is not required if either the recovered clock or MCLK PLL is chosen as the timing source of the device. High speed or multiplexed data is latched into the device using the TxMSYNC/TxINCLK high-speed clock signal. **DS1 or E1 Framer Bypass Mode - TxLINECLKn** In this mode, TxSERCLKn is used as the transmit line clock (TxLINECLK) to the LIU. ***NOTE:*** **High-speed backplane modes include (For T1/E1) 2.048MVIP, 4.096MHz, 8.192MHz, 16.384MHz HMVIP, H.100, Bit-multiplexed modes, and (For T1 only) 12.352MHz Bit-multiplexed mode.* ***NOTE:*** *In DS1 high-speed modes, the DS-0 data is mapped into an E1 frame by ignoring every fourth time slot (don't care).* ***NOTE:*** *These 8 pins are internally pulled "High" for each channel.*

TRANSMIT SYSTEM SIDE INTERFACE

SIGNAL NAME	BALL#	TYPE	OUTPUT DRIVE(MA)	DESCRIPTION
TxSYNC0/ TxNEG0 TxSYNC1/ TxNEG1 TxSYNC2/ TxNEG2 TxSYNC3/ TxNEG3	D9 B18 L15 U15	I/O	12	**Transmit Single Frame Sync Pulse (TxSYNCn) / Transmit Negative Digital Input (TxNEGn):** The exact function of these pins depends on the mode of operation selected, as described below. **DS1/E1 Base Rate Mode (1.544MHz/2.048MHz) - TxSYNCn:** These TxSYNCn pins are used to indicate the single frame boundary within an outbound T1/E1 frame. In both DS1 or E1 mode, the single frame boundary repeats every 125 microseconds (8kHz). In DS1/E1 base rate, TxSYNCn can be configured as either input or output as described below. **When TxSYNCn is configured as an Input**: Users must provide a signal which must pulse "High" for one period of TxSERCLK during the first bit of an outbound DS1/E1 frame. It is imperative that the TxSYNC input signal be synchronized with the TxSERCLK input signal. **When TxSYNCn is configured as an Output:** The transmit T1/E1 framer will output a signal which pulses "High" for one period of TxSERCLK during the first bit of an outbound DS1/E1 frame. **DS1/E1 High-Speed Backplane Modes* - TxSYNCn as INPUT ONLY:** In this mode, TxSYNCn must be an input regardless of the clock source that is chosen to be the timing source for the transmit framer. In 2.048MVIP/4.096/8.192MHz high-speed modes, TxSYNCn pins must be pulsed 'High' for one period of TxSERCLK during the first bit of the outbound T1/E1 frame. In HMVIP mode, TxSYNC0 must be pulsed 'High' for 4 clock cycles of the TxMSYNC/TxINCLK signal in the position of the first two and the last two bits of a multiplexed frame. In H.100 mode, TxSYNC0 must be pulsed 'High' for 2 clock cycles of the TxMSYNC/TxINCLK signal in the position of the first and the last bit of a multiplexed frame. **DS1 or E1 Framer Bypass Mode - TxNEGn** In this mode, TxSYNCn is used as the negative digital input pin (TxNEG) to the LIU. ***NOTE:*** **High-speed backplane modes include (For T1/E1) 2.048MVIP, 4.096MHz, 8.192MHz, 16.384MHz HMVIP, H.100, Bit-multiplexed modes, and (For T1 only) 12.352MHz Bit-multiplexed mode.* ***NOTE:*** *In DS1 high-speed modes, the DS-0 data is mapped into an E1 frame by ignoring every fourth time slot (don't care).* ***NOTE:*** *These 8 pins are internally pulled "Low" for each channel.*

TRANSMIT SYSTEM SIDE INTERFACE

SIGNAL NAME	BALL#	TYPE	OUTPUT DRIVE(MA)	DESCRIPTION
TxMSYNC0/ TxINCLK0 TxMSYNC1/ TxINCLK1 TxMSYNC2/ TxINCLK2 TxMSYNC3/ TxINCLK3	A10 C17 L17 R12	I/O	12	**Multiframe Sync Pulse (TxMSYNCn) / Transmit Input Clock (TxINCLKn)** The exact function of these pins depends on the mode of operation selected, as described below. **DS1/E1 Base Rate Mode (1.544MHz/2.048MHz) - TxMSYNCn** In this mode, these pins are used to indicate the multi-frame boundary within an outbound DS1/E1 frame. In DS1 ESF mode, TxMSYNCn repeats every 3ms. In DS1 SF mode, TxMSYNCn repeats every 1.5ms. In E1 mode, TxMSYNCn repeats every 2ms. If TxMSYNCn is configured as an input, TxMSYNCn must pulse "High" for one period of TxSERCLK during the first bit of an outbound DS1/E1 multi-frame. It is imperative that the TxMSYNC input signal be synchronized with the TxSERCLK input signal. If TxMSYNCn is configured as an output, the transmit section of the T1/E1 framer will output and pulse TxMSYNC "High" for one period of TxSERCLK during the first bit of an outbound DS1/E1 frame. **DS1/E1 High-Speed Backplane Modes* - (TxINCLKn as INPUT ONLY)** In this mode, TxINCLK0 must be used as the high-speed input clock pin for the backplane interface to latch in high-speed or multiplexed data on the TxSERn pin. The frequency of TxINCLK0 is presented in the table below.

OPERATION MODE	FREQUENCY OF TXINCLK0(MHZ)
2.048MVIP non-multiplexed	2.048
4.096MHz non-multiplexed	4.096
8.192MHz non-multiplexed	8.192
12.352MHz Bit-multiplexed (DS1 ONLY)	12.352
16.384MHz Bit-multiplexed	16.384
16.384 HMVIP Byte-multiplexed	16.384
16.384 H.100 Byte-multiplexed	16.384

NOTES:

1. **High-speed backplane modes include (For T1/E1) 2.048MVIP, 4.096MHz, 8.192MHz, 16.384MHz HMVIP, H.100, Bit-multiplexed modes, and (For T1 only) 12.352MHz Bit-multiplexed mode.*
2. *In DS1 high-speed modes, the DS-0 data is mapped into an E1 frame by ignoring every fourth time slot (don't care).*
3. *These 8 pins are internally pulled "Low" for each channel.*

TRANSMIT SYSTEM SIDE INTERFACE

SIGNAL NAME	BALL#	TYPE	OUTPUT DRIVE(MA)	DESCRIPTION
TxCHCLK0 TxCHCLK1 TxCHCLK2 TxCHCLK3	A13 C15 N17 V17	O	8	**Transmit Channel Clock Output Signal (TxCHCLKn):** The exact function of this pin depends on whether or not the transmit framer enables the transmit fractional/signaling interface to input fractional data, as described below. **If transmit fractional/signaling interface is disabled:** This pin indicates the boundary of each time slot of an outbound DS1/E1 frame. In T1 mode, each of these output pins is a 192kHz clock which pulses "High" during the LSB of each 24 time slots. In E1 mode, each of these output pins is a 256kHz clock which pulses "High" during the LSB of each 32 time slots. The Terminal Equipment can use this clock signal to sample the TxCHN0 through TxCHN4 time slot identifier pins to determine which time slot is being processed. **If transmit fractional/signaling interface is enabled:** TxCHCLKn is the fractional interface clock which either outputs a clock signal for the time slot that has been configured to input fractional data, or outputs an enable signal for the fractional time slot so that fractional data can be clocked into the device using the TxSERCLK pin. ***NOTE:*** *Transmit fractional interface can be enabled by programming to bit 4 - TxFr1544/TxFr2048 bit from register 0xn120 to '1'.*

TRANSMIT SYSTEM SIDE INTERFACE

SIGNAL NAME	BALL#	TYPE	OUTPUT DRIVE(MA)	DESCRIPTION
TxCHN0_0/ TxSIG0 TxCHN1_0/ TxSIG1 TxCHN2_0/ TxSIG2 TxCHN3_0/ TxSIG3	B12 F16 M18 T13	I/O	8	**Transmit Time Slot Octet Identifier Output 0 (TxCHNn_0) / Transmit Serial Signaling Input (TxSIGn):** The exact function of these pins depends on whether or not the transmit framer enables the transmit fractional/signaling interface, as described below: **If transmit fractional/signaling interface is disabled - TxCHNn_0:** These output pins (TxCHNn_4 through TxCHNn_0) reflect the five-bit binary value of the current time slot being processed by the transmit serial interface. Terminal Equipment can use the TxCHCLK to sample the five output pins of each channel in order to identify the time slot being processed. This pin indicates the Least Significant Bit (LSB) of the time slot channel being processed. **If transmit fractional/signaling interface is enabled - TxSIGn:** These pins can be used to input robbed-bit signaling data to be inserted within an outbound DS1 frame or to input Channel Associated Signaling (CAS) data within an outbound E1 frame, as described below. **T1 Mode:** Signaling data (A,B,C,D) of each channel must be provided on bit 4,5,6,7 of each time slot on the TxSIG pin if 16-code signaling is used. If 4-code signaling is selected, signaling data (A,B) of each channel must be provided on bit 4, 5 of each time slot on the TxSIG pin. If 2-code signaling is selected, signaling data (A) of each channel must be provided on bit 4 of each time slot on the TxSIG pin. **E1 Mode:** Signaling data in E1 mode can be provided on the TxSIGn pins on a time-slot-basis as in T1 mode, or it can be provided on time slot 16 only via the TxSIGn input pins. In the latter case, signaling data (A,B,C,D) of channel 1 and channel 17 must be inserted on the TxSIGn pin during time slot 16 of frame 1, signaling data (A,B,C,D) of channel 2 and channel 18 must be inserted on the TxSIGn pin during time slot 16 of frame 2...etc. The CAS multiframe Alignments bits (0000 bits) and the extra bits/alarm bit (xyxx) must be inserted on the TxSIGn pin during time slot 16 of frame 0. ***NOTE:*** *Transmit fractional interface can be enabled by programming to bit 4 - TxFr1544/TxFr2048 bit from register 0xn120 to '1'.* ***NOTE:*** *These 8 pins are internally pulled "Low" for each channel.*

TRANSMIT SYSTEM SIDE INTERFACE

SIGNAL NAME	BALL#	TYPE	OUTPUT DRIVE(MA)	DESCRIPTION
TxCHN0_1/ TxFrTD0 TxCHN1_1/ TxFrTD1 TxCHN2_1/ TxFrTD2 TxCHN3_1/ TxFrTD3	D12 F17 M17 U13	I/O	8	**Transmit Time Slot Octet Identifier Output 1 (TxCHNn_1) / Transmit Serial Fractional Input (TxFrTDn):** The exact function of these pins depends on whether or not the transmit framer enables the transmit fractional/signaling interface, as described below: **If transmit fractional/signaling interface is disabled - TxCHNn_1** These output signals (TxCHNn_4 through TxCHNn_0) reflect the five-bit binary value of the current time slot being processed by the transmit serial interface. Terminal Equipment can use the TxCHCLK to sample the five output pins of each channel in order to identify the time slot being processed. This pin indicates Bit 1 of the time slot channel being processed. **If transmit fractional/signaling interface is enabled - TxFrTDn** These pins are used as the fractional data input pins to input fractional DS1/E1 payload data which will be inserted within an outbound DS1/E1 frame. In this mode, terminal equipment can use either TxCHCLK or TxSERCLK to clock in fractional DS1/E1 payload data depending on the framer configuration. ***NOTES:*** *1. Transmit fractional/Signaling interface can be enabled by programming to bit 4 - TxFr1544/TxFr2048 bit from register 0xn120 to '1'.* *2. These 8 pins are internally pulled "Low" for each channel.*
TxCHN0_2/ Tx32MHz0 TxCHN1_2/ Tx32MHz1 TxCHN2_2/ Tx32MHz2 TxCHN3_2/ Tx32MHz3	B13 G17 T16 T12	O	8	**Transmit Time Slot Octet Identifier Output 2 (TxCHNn_2) / Transmit 32.678MHz Clock Output (Tx32MHZ):** The exact function of these pins depends on whether or not the transmit framer enables the transmit fractional/signaling interface, as described below: **If transmit fractional/signaling interface is disabled - TxCHNn_2** These output signals (TxCHNn_4 through TxCHNn_0) reflect the five-bit binary value of the current time slot being processed by the transmit serial interface. Terminal Equipment can use the TxCHCLK to sample the five output pins of each channel in order to identify the time slot being processed. This pin indicates Bit 2 of the time slot channel being processed. **If transmit fractional/signaling interface is enabled - Tx32MHz** These pins are used to output a 32.678MHz clock reference which is derived from the MCLKIN input pin. ***NOTE:*** *Transmit fractional interface can be enabled by programming to bit 4 - TxFr1544/TxFr2048 bit from register 0xn120 to '1'.*

TRANSMIT SYSTEM SIDE INTERFACE

SIGNAL NAME	BALL#	TYPE	OUTPUT DRIVE(MA)	DESCRIPTION
TxCHN0_3/ TxOHSYNC0 TxCHN1_3/ TxOHSYNC1 TxCHN2_3/ TxOHSYNC2 TxCHN3_3/ TxOHSYNC3	A14 G18 N16 U12	O O	8	**Transmit Time Slot Octet Identifier Output 3 (TxCHNn_3) / Transmit Overhead Synchronization Pulse (TxOHSYNCn):** The exact function of these pins depends on whether or not the transmit framer enables the transmit fractional/signaling interface, as described below: **If transmit fractional/signaling interface is disabled - TxCHNn_3** These output signals (TxCHNn_4 through TxCHNn_0) reflect the five-bit binary value of the current time slot being processed by the transmit serial interface. Terminal Equipment can use the TxCHCLK to sample the five output pins of each channel in order to identify the time slot being processed. This pin indicates Bit 3 of the time slot channel being processed. **If transmit fractional/signaling interface is enabled - TxOHSYNCn** These pins are used to output an Overhead Synchronization Pulse which indicates the first bit of each multi-frame. ***NOTE:*** *Transmit fractional interface can be enabled by programming to bit 4 - TxFr1544/TxFr2048 bit from register 0xn120 to '1'.*
TxCHN0_4 TxCHN1_4 TxCHN2_4 TxCHN3_4	C14 H18 N15 T11	O	8	**Transmit Time Slot Octet Identifier Output-Bit 4 (TxCHNn_4):** These output signals (TxCHNn_4 through TxCHNn_0) reflect the five-bit binary value of the current time slot being processed by the transmit serial interface. Terminal Equipment can use the TxCHCLK to sample the five output pins of each channel in order to identify the time slot being processed. This pin indicates the Most Significant Bit (MSB) of the time slot channel being processed.

TRANSMIT OVERHEAD INTERFACE

SIGNAL NAME	BALL #	TYPE	OUTPUT DRIVE(mA)	DESCRIPTION
TxOH0 TxOH1 TxOH2 TxOH3	C12 F15 P15 R14	I	-	**Transmit Overhead Input (TxOHn):** The exact function of these pins depends on the mode of operation selected, as described below. **DS1 Mode** These pins operate as the source of Datalink bits which will be inserted into the Datalink bits within an outbound DS1 frame if the framer is configured accordingly. Datalink Equipment can provide data to this input pin using the TxOHCLKn clock at either 2kHz or 4kHz depending on the transmit datalink bandwidth selected. ***NOTE:*** *This input pin will be disabled if the framer is using the Transmit HDLC Controller, or the TxSER input as the source for the Data Link Bits.* **E1 Mode** These pins operate as the source of Datalink bits or Signaling bits depending on the framer configuration, as described below. **Sourcing Datalink bits from TxOHn:** The E1 transmit framer will output a clock edge on TxOHCLKn for each Sa bit that has been configured to carry datalink information. Terminal equipment can then use TxOHCLKn to provide datalink bits on TxOHn to be inserted into the Sa bits within an outbound E1 frame. **Sourcing Signaling bits from TxOHn:** Users must provide signaling data on TxOHn pins on time slot 16 only. Signaling data (A,B,C,D) of channel 1 and channel 17 must be inserted on the TxOHn pin during time slot 16 of frame 1, signaling data (A,B,C,D) of channel 2 and channel 18 must be inserted on the TxOHn pin during time slot 16 of frame 2...etc. The CAS multiframe Alignments bits (0000 bits) and the extra bits/alarm bit (xyxx) must be inserted on the TxOHn pin during time slot 16 of frame 0. ***NOTE:*** *These 8 pins are internally pulled "Low" for each channel.*

TRANSMIT OVERHEAD INTERFACE

SIGNAL NAME	BALL #	TYPE	OUTPUT DRIVE(MA)	DESCRIPTION
TxOHCLK0 TxOHCLK1 TxOHCLK2 TxOHCLK3	A11 E15 N18 V16	O	8	**Transmit OH Serial Clock Output Signal(TxOHCLKn)** This pin functions as an overhead output clock signal for the transmit overhead interface, and its function is explained below. **DS1 Mode** If the TxOH pins have been configured to be the source for Datalink bits, the DS1 transmit framer will provide a clock edge for each Data Link Bit. In DS1 ESF mode, the TxOHCLK can either be a 2kHz or 4kHz output signal depending on the selection of Data Link Bandwidth (Register 0xn10A). Data Link Equipment can provide data to the TxOHn pin on the rising edge of TxOHCLK. The framer latches the data on the falling edge of this clock signal. **E1 Mode** If the TxOH pins have been configured to be the source for Data Link bits, the E1 transmit framer will provide a clock edge for each National Bit (Sa bits) that has been configured to carry data link information. (Register 0xn10A)

RECEIVE OVERHEAD INTERFACE

SIGNAL NAME	BALL #	TYPE	OUTPUT DRIVE(MA)	DESCRIPTION
RxOH0 RxOH1 RxOH2 RxOH3	C11 B16 K15 P18	O	8	**Receive Overhead Output (RxOHn):** These pins function as the Receive Overhead output, or Receive Signaling Output depending on the receive framer configuration, as described below. **DS1 Mode** If the RxOH pins have been configured as the destination for the Data Link bits within an inbound DS1 frame, datalink bits will be output to the RxOHn pins at either 2kHz or 4kHz depending on the Receive datalink bandwidth selected. (Register 0xn10C). If configured appropriately, signaling information in the receive signaling array registers (Registers 0xn500-0xn51F) can also be output to the RxOHn output pins. **E1 Mode** These output pins will always output the contents of the National Bits (Sa4 through Sa8) if these Sa bits have been configured to carry Data Link information (Register 0xn10C). The Receive Overhead Output Interface will provide a clock edge on RxOHCLKn for each Sa bit carrying Data Link information. If configured appropriately, signaling information in the receive signaling array registers (Registers 0xn500-0xn51F) can also be output to the RxOHn output pins.
RxOHCLK0 RxOHCLK1 RxOHCLK2 RxOHCLK3	A9 D17 K17 R16	O	8	**Receive Overhead Clock Output (RxOHCLKn):** This pin functions as an overhead output clock signal for the receive overhead interface, and its function is explained below. **DS1 Mode** If the RxOH pins have been configured to be the destination for Datalink bits, the DS1 transmit framer will output a clock edge for each Data Link Bit. In DS1 ESF mode, the RxOHCLK can either be a 2kHz or 4kHz output signal depending on the selection of Data Link Bandwidth (Register 0xn10C). Data Link Equipment can clock out datalink bits on the RxOHn pin using this clock signal. **E1 Mode** The E1 receive framer provides a clock edge for each National Bit (Sa bits) that is configured to carry data link information. Data Link Equipment can clock out datalink bits on the RxOHn pin using this clock signal.

RECEIVE SYSTEM SIDE INTERFACE

SIGNAL NAME	BALL #	TYPE	OUTPUT DRIVE (MA)	DESCRIPTION
RxSYNC0/ RxNEG0 RxSYNC1/ RxNEG1 RxSYNC2/ RxNEG2 RxSYNC3/ RxNEG3	D8 A18 F18 P16	I/O	12	**Receive Single Frame Sync Pulse (RxSYNCn):** The exact function of these pins depends on the mode of operation selected, as described below. **DS1/E1 Base Rate Mode (1.544MHz/2.048MHz) - RxSYNCn:** These RxSYNCn pins are used to indicate the single frame boundary within an inbound T1/E1 frame. In both DS1 or E1 mode, the single frame boundary repeats every 125 microseconds (8kHz). In DS1/E1 base rate, RxSYNCn can be configured as either input or output depending on the slip buffer configuration as described below. **When RxSYNCn is configured as an Input**: Users must provide a signal which must pulse "High" for one period of RxSERCLK and repeats every 125µS. The receive serial Interface will output the first bit of an inbound DS1/E1 frame during the provided RxSYNC pulse. ***NOTE:*** *It is imperative that the RxSYNC input signal be synchronized with the RxSERCLK input signal.* **When RxSYNCn is configured as an Output:** The receive T1/E1 framer will output a signal which pulses "High" for one period of RxSERCLK during the first bit of an inbound DS1/E1 frame. **DS1/E1 High-Speed Backplane Modes* - RxSYNCn as INPUT ONLY:** In this mode, RxSYNCn must be an input regardless of the slip buffer configuration. In 2.048MVIP/4.096/8.192MHz high-speed modes, RxSYNCn pins must be pulsed 'High' for one period of RxSERCLK during the first bit of the inbound T1/E1 frame. In HMVIP mode, RxSYNC0 must be pulsed 'High' for 4 clock cycles of the RxSERCLK signal in the position of the first two and the last two bits of a multiplexed frame. In H.100 mode, RxSYNC0 must be pulsed 'High' for 2 clock cycles of the RxSERCLK signal in the position of the first and the last bit of a multiplexed frame. **DS1 or E1 Framer Bypass Mode - RxNEGn** In this mode, RxSYNCn is used as the Receive negative digital output pin (RxNEG) from the LIU. ***NOTE:*** **High-speed backplane modes include (For T1/E1) 2.048MVIP, 4.096MHz, 8.192MHz, 16.384MHz HMVIP, H.100, Bit-multiplexed modes, and (For T1 only) 12.352MHz Bit-multiplexed mode.* ***NOTE:*** *In DS1 high-speed modes, the DS-0 data is mapped into an E1 frame by ignoring every fourth time slot (don't care).* ***NOTE:*** *These 8 pins are internally pulled "Low" for each channel.*

RECEIVE SYSTEM SIDE INTERFACE

SIGNAL NAME	BALL #	TYPE	OUTPUT DRIVE (MA)	DESCRIPTION
RxCRCSYNC0 RxCRCSYNC1 RxCRCSYNC2 RxCRCSYNC3	C8 C13 J17 R17	O	12	**Receive Multiframe Sync Pulse (RxCRCSYNCn):** The RxCRCSYNCn pins are used to indicate the receive multi-frame boundary. These pins pulse "High" for one period of RxSERCLK when the first bit of an inbound DS1/E1 Multi-frame is being output on the RxCRCSYNCn pin. • In DS1 ESF mode, RxCRCSYNCn repeats every 3ms • In DS1 SF mode, RxCRCSYNCn repeats every 1.5ms • In E1 mode, RxCRCSYNCn repeats every 2ms.
RxCASYNC0 RxCASYNC1 RxCASYNC2 RxCASYNC3	D10 B17 H15 T18	O	12	**Receive CAS Multiframe Sync Pulse (RxCASYNCn):** **- E1 Mode Only** The RxCASYNCn pins are used to indicate the E1 CAS Multif-frame boundary. These pins pulse "High" for one period of RxSERCLK when the first bit of an E1 CAS Multi-frame is being output on the RxCASYNCn pin.

RECEIVE SYSTEM SIDE INTERFACE

SIGNAL NAME	BALL #	TYPE	OUTPUT DRIVE (mA)	DESCRIPTION
RxSERCLK0/ RxLINECLK0 RxSERCLK1/ RxLINECLK1 RxSERCLK2/ RxLINECLK2 RxSERCLK3/ RxLINECLK3	A7 D13 D15 T17	I/O	12	**Receive Serial Clock Signal (RxSERCLKn) / Receive Line Clock (RxLINECLKn):** The exact function of these pins depends on the mode of operation selected, as described below. **In Base-Rate Mode (1.544MHz/2.048MHz) - RxSERCLKn:** These pins are used as the receive serial clock on the system side interface which can be configured as either input or output. The receive serial interface outputs data on RxSERn on the rising edge of RxSERCLKn. **When RxSERCLKn is configured as Input:** These pins will be inputs if the slip buffer on the Receive path is enabled. System side equipment must provide a 1.544MHz clock rate to this input pin for T1 mode of operation, and 2.048MHz clock rate in E1 mode. **When RxSERCLKn is configured as Output:** These pins will be outputs if slip buffer is bypassed. The receive framer will output a 1.544MHz clock rate in T1 mode of operation, and a 2.048MHz clock rate in E1 mode. **DS1/E1 High-Speed Backplane Modes* - (RxSERCLK as INPUT ONLY)** In this mode, this pin must be used as the high-speed input clock for the backplane interface to output high-speed or multiplexed data on the RxSERn pin. The frequency of RxSERCLK is presented in the table below.

OPERATION MODE	FREQUENCY OF RxSERCLK(MHz)
2.048MVIP non-multiplexed	2.048
4.096MHz non-multiplexed	4.096
8.192MHz non-multiplexed	8.192
12.352MHz Bit-multiplexed (DS1 ONLY)	12.352
16.384MHz Bit-multiplexed	16.384
16.384 HMVIP Byte-multiplexed	16.384
16.384 H.100 Byte-multiplexed	16.384

NOTES:

1. **High-speed backplane modes include (For T1/E1) 2.048MVIP, 4.096MHz, 8.192MHz, 16.384MHz HMVIP, H.100, Bit-multiplexed modes, and (For T1 only) 12.352MHz Bit-multiplexed mode.*
2. *For DS1 high-speed modes, the DS-0 data is mapped into an E1 frame by ignoring every fourth time slot (don't care).*

RECEIVE SYSTEM SIDE INTERFACE

SIGNAL NAME	BALL #	TYPE	OUTPUT DRIVE (MA)	DESCRIPTION
RxSERCLK0/ RxLINECLK0 RxSERCLK1/ RxLINECLK1 RxSERCLK2/ RxLINECLK2 RxSERCLK3/ RxLINECLK3	A7 D13 D15 T17	I/O	12	**(Continued)** **DS1 or E1 Framer Bypass Mode - RxLINECLKn** In this mode, RxSERCLKn is used as the Receive Line Clock output pin (RxLineClk) from the LIU. ***NOTE:*** *These 8 pins are internally pulled "High" for each channel.*
RxSER0/ RxPOS0 RxSER1/ RxPOS1 RxSER2/ RxPOS2 RxSER3/ RxPOS3	D6 A15 J18 U17	O	12	**Receive Serial Data Output (RxSERn):** The exact function of these pins depends on the mode of operation selected, as described below. **DS1/E1 Mode - RxSERn** These pins function as the receive serial data output on the system side interface, which updates on the rising edge of the RxSERCLKn pin. All the framing alignment bits, facility data link bits, CRC bits, and signaling information will also be extracted to this output pin. **DS1 or E1 High-Speed Multiplexed Mode* - RxSERn** In this mode, these pins are used as the high-speed multiplexed data output pin on the system side. High-speed multiplexed data of channels 0-3 will output on RxSER0 in a byte or bit-interleaved way. The framer outputs the multiplexed data on RxSER0 using the high-speed input clock (RxSERCLKn). **DS1 or E1 Framer Bypass Mode** In this mode, RxSERn is used as the positive digital output pin (RxPOSn) from the LIU. ***NOTE:*** **High-speed multiplexed modes include (For T1/E1) 16.384MHz HMVIP, H.100, Bit-multiplexed modes, and (For T1 only) 12.352MHz Bit-multiplexed mode.* ***NOTE:*** *In DS1 high-speed modes, the DS-0 data is mapped into an E1 frame by ignoring every fourth time slot (don't care).*

RECEIVE SYSTEM SIDE INTERFACE

SIGNAL NAME	BALL #	TYPE	OUTPUT DRIVE (mA)	DESCRIPTION
RxCHN0_0/ RxSig0 RxCHN1_0/ RxSig1 RxCHN2_0/ RxSig2 RxCHN3_0/ RxSig3	D7 D14 H16 R18	O	8	**Receive Time Slot Octet Identifier Output (RxCHNn_0) / Receive Serial Signaling Output (RxSIGn):** The exact function of these pins depends on whether or not the receive framer enables the receive fractional/signaling interface, as described below: **If receive fractional/signaling interface is disabled - RxCHNn_0:** These output pins (RxCHNn_4 through RxCHNn_0) reflect the five-bit binary value of the current time slot being output by the receive serial interface. System equipment can use the RxCHCLKn to sample the five output pins of each channel to identify the time slot being output on these pins. RxCHNn_0 indicates the Least Significant Bit (LSB) of the time slot channel being output. **If receive fractional/signaling interface is enabled - RxSIGn:** These pins can be used to output robbed-bit signaling data within an inbound DS1 frame or to output Channel Associated Signaling (CAS) data within an inbound E1 frame, as described below. **T1 Mode:** Signaling data (A,B,C,D) of each channel will be output on bit 4,5,6,7 of each time slot on the RxSIG pin if 16-code signaling is used. If 4-code signaling is selected, signaling data (A,B) of each channel will be output on bit 4, 5 of each time slot on the RxSIG pin. If 2-code signaling is selected, signaling data (A) of each channel will be output on bit 4 of each time slot on the RxSIG pin. **E1 Mode:** Signaling data in E1 mode will be output on the RxSIGn pins on a time-slot-basis as in T1 mode, or it can be output on time slot 16 only via the RxSIGn output pins. In the latter case, signaling data (A,B,C,D) of channel 1 and channel 17 will be output on the RxSIGn pin during time slot 16 of frame 1, signaling data (A,B,C,D) of channel 2 and channel 18 will be output on the RxSIGn pin during time slot 16 of frame 2...etc. The CAS multiframe Alignments bits (0000 bits) and the extra bits/alarm bit (xyxx) will be output on the RxSIGn pin during time slot 16 of frame 0. ***NOTE:*** *Receive Fractional/signaling interface can be enabled by programming to bit 4 - RxFr1544/RxFr2048 bit from register 0xn122 to '1'.*

RECEIVE SYSTEM SIDE INTERFACE

SIGNAL NAME	BALL #	TYPE	OUTPUT DRIVE (MA)	DESCRIPTION
RxCHN0_1/ RxFrTD0 RxCHN1_1/ RxFrTD1 RxCHN2_1/ RxFrTD2 RxCHN13_1/ RxFrTD3	C9 B15 G15 V18	O	8	**Receive Time Slot Octet Identifier Output Bit 1 (RxCHNn_1) / Receive Serial Fractional Output (RxFrTDn):** The exact function of these pins depends on whether or not the receive framer enables the receive fractional/signaling interface, as described below: **If receive fractional/signaling interface is disabled - RxCHNn_1:** These output pins (RxCHNn_4 through RxCHNn_0) reflect the five-bit binary value of the current time slot being output by the receive serial interface. System equipment can use the RxCHCLKn to sample the five output pins of each channel to identify the time slot being output on these pins. RxCHNn_1 indicates Bit 1 of the time slot channel being output. **If receive fractional/signaling interface is enabled - RxFrTDn:** These pins are used as the fractional data output pins to output fractional DS1/E1 payload data within an inbound DS1/E1 frame. In this mode, system equipment can use either RxCHCLK or RxSERCLK to clock out fractional DS1/E1 payload data depending on the framer configuration. ***NOTE:*** *Receive Fractional/Signaling interface can be enabled by programming to bit 4 - RxFr1544/RxFr2048 bit from register 0xn122 to '1'.*
RxCHN0_2/ RxCHN0 RxCHN1_2/ RxCHN1 RxCHN2_2/ RxCHN2 RxCHN3_2/ RxCHN3	B9 A17 K18 T15	O	8	**Receive Time Slot Octet Identifier Output-Bit 2 (RxCHNn_2) / Receive Time Slot Identifier Serial Output (RxCHNn):** The exact function of these pins depends on whether or not the receive framer enables the receive fractional/signaling interface, as described below: **If receive fractional/signaling interface is disabled - RxCHNn_2:** These output pins (RxCHNn_4 through RxCHNn_0) reflect the five-bit binary value of the current time slot being output by the receive serial interface. System equipment can use the RxCHCLKn to sample the five output pins of each channel to identify the time slot being output on these pins. RxCHNn_2 indicates Bit 2 of the time slot channel being output. **If receive fractional/signaling interface is enabled - RxCHNn** These pins serially output the five-bit binary value of the time slot being output by the receive serial interface. ***NOTE:*** *Receive Fractional/Signaling interface can be enabled by programming to bit 4 - RxFr1544/RxFr2048 bit from register 0xn122 to '1'.*

RECEIVE SYSTEM SIDE INTERFACE

SIGNAL NAME	BALL #	TYPE	OUTPUT DRIVE (mA)	DESCRIPTION
RxCHN0_3/ Rx8KHZ0 RxCHN1_3/ Rx8KHZ1 RxCHN2_3/ Rx8KHZ2 RxCHN3_3/ Rx8KHZ3	C10 D18 L16 T14	O	8	**Receive Time Slot Octet Identifier Output-Bit 3 (RxCHNn_3) / Receive 8KHz Clock Output (Rx8KHZn):** The exact function of these pins depends on whether or not the receive framer enables the receive fractional/signaling interface, as described below: **If receive fractional/signaling interface is disabled - RxCHNn_3:** These output pins (RxCHNn_4 through RxCHNn_0) reflect the five-bit binary value of the current time slot being output by the receive serial interface. System equipment can use the RxCHCLKn to sample the five output pins of each channel to identify the time slot being output on these pins. RxCHNn_3 indicates Bit 3 of the time slot channel being output. **If receive fractional/signaling interface is enabled - Rx8KHZn:** These pins output a reference 8KHz clock signal derived from the MCLKIN input. ***NOTE:*** *Receive Fractional/Signaling interface can be enabled by programming to bit 4 - RxFr1544/RxFr2048 bit from register 0xn122 to '1'.*
RxCHN0_4/ RxSCLK0 RxCHN1_4/ RxSCLK1 RxCHN2_4/ RxSCLK2 RxCHN3_4/ RxSCLK3	B10 E17 K16 U14	O	8	**Receive Time Slot Octet Identifier Output-Bit 4 (RxCHNn_4) / Receive Recovered Line Clock Output (RxSCLKn):** The exact function of these pins depends on whether or not the receive framer enables the receive fractional/signaling interface, as described below: **If receive fractional/signaling interface is disabled - RxCHNn_4:** These output pins (RxCHNn_4 through RxCHNn_0) reflect the five-bit binary value of the current time slot being output by the receive serial interface. System equipment can use the RxCHCLKn to sample the five output pins of each channel to identify the time slot being output on these pins. RxCHNn_4 indicates the Most Significant Bit (MSB) of the time slot channel being output. **If receive fractional/signaling interface is enabled - Receive Recovered Line Clock Output (RxSCLKn):** These pins output the recovered T1/E1 line clock (1.544MHz in T1 mode and 2.048MHz in E1 mode) for each channel. ***NOTE:*** *Receive Fractional/Signaling interface can be enabled by programming to bit 4 - RxFr1544/RxFr2048 bit from register 0xn122 to '1'.*

RECEIVE SYSTEM SIDE INTERFACE

SIGNAL NAME	BALL #	TYPE	OUTPUT DRIVE (MA)	DESCRIPTION
RxCHCLK0 RxCHCLK1 RxCHCLK2 RxCHCLK3	A8 A16 H17 P17	O	8	**Receive Channel Clock Output (RxCHCLKn):** The exact function of this pin depends on whether or not the receive framer enables the receive fractional/signaling interface to output fractional data, as described below. **If receive fractional/signaling interface is disabled:** This pin indicates the boundary of each time slot of an inbound DS1/E1 frame. In T1 mode, each of these output pins is a 192kHz clock which pulses "High" during the LSB of each 24 time slots. In E1 mode, each of these output pins is a 256kHz clock which pulses "High" during the LSB of each 32 time slots. System Equipment can use this clock signal to sample the RxCHN0 through RxCHN4 time slot identifier pins to determine which time slot is being output. **If receive fractional/signaling interface is enabled:** RxCHCLKn is the fractional interface clock which either outputs a clock signal for the time slot that has been configured to output fractional data, or outputs an enable signal for the fractional time slot so that fractional data can be clocked out of the device using the RxSERCLK pin. ***NOTE:*** *Receive fractional interface can be enabled by programming to bit 4 - RxFr1544/RxFr2048 bit from register 0xn122 to '1'.*

RECEIVE LINE INTERFACE

SIGNAL NAME	BALL #	TYPE	OUTPUT DRIVE (mA)	DESCRIPTION
RTIP0 RTIP1 RTIP2 RTIP3	E1 G1 J1 L1	I	-	**Receive Positive Analog Input (RTIPn):** RTIP is the positive differential input from the line interface. This input pin, along with the RRING input pin, functions as the "Receive DS1/E1 Line Signal" input for the XRT86VL34 device. The user is expected to connect this signal and the RRING input signal to a 1:1 transformer for proper operation. The center tap of the receive transformer should have a bypass capacitor of 0.1µF to ground (Chip Side) to improve long haul application receive capabilities.
RRING0 RRING1 RRING2 RRING3	F1 H1 K1 M1	I	-	**Receive Negative Analog Input (RRINGn):** RRING is the negative differential input from the line interface. This input pin, along with the RTIP input pin, functions as the "Receive DS1/E1 Line Signal" input for the XRT86VL34 device. The user is expected to connect this signal and the RTIP input signal to a 1:1 transformer for proper operation. The center tap of the receive transformer should have a bypass capacitor of 0.1µF to ground (Chip Side) to improve long haul application receive capabilities.
RxLOS_0 RxLOS_1 RxLOS_2 RxLOS_3	B7 C18 G16 U18	O	4	**Receive Loss of Signal Output Indicator (RLOSn):** The XRT86VL34 device will assert this output pin (i.e., toggle it "high") anytime (and for the duration that) the Receive DS1/E1 Framer or LIU block declares the LOS defect condition. Conversely, the XRT86VL34 device will tri-state this output pin anytime (and for the duration that) the Receive DS1/E1 Framer or LIU block is NOT declaring the LOS defect condition. ***NOTES:*** *1. This output pin will toggle "high" (to denote that LOS is being declared) whenever either the Receive DS1/E1 Framer or the Receive DS1/E1 LIU block (associated wtih Channel N) declares the LOS defect condition. In other words, the state of this output pin is a logical OR of the Framer LOS and the LIU LOS conditions.* *2. Since the XRT86VL34 device tri-states this output pin (anytime the channel is not declaring the LOS defect condition). Therefore, the user MUST connect a "pull-down" resistor (ranging from 1K to 10K) to each RxLOS output pin, in order to pull this output pin to the logic "LOW" condition, whenever the Channel is NOT declaring the LOS defect condition.*

RECEIVE LINE INTERFACE

SIGNAL NAME	BALL #	TYPE	OUTPUT DRIVE (MA)	DESCRIPTION
RxTSEL	N3	I	-	**Receive Termination Control (RxTSEL):** Upon power up, the receivers are in "High" impedance. Switching to internal termination can be selected through the microprocessor interface by programming the appropriate channel register. However, to switch control to the hardware pin, RxTCNTL must be programmed to "1" in the appropriate global register (0x0FE2). Once control has been granted to the hardware pin, it must be pulled "High" to switch to internal termination. ***NOTE:*** *Internally pulled "Low" with a 50kΩ resistor.* **RxTSEL (pin)** / **Rx Termination** 0 / External 1 / Internal *Note: RxTCNTL (bit) must be set to "1"*

TRANSMIT LINE INTERFACE

SIGNAL NAME	BALL #	TYPE	DESCRIPTION
TTIP0 TTIP1 TTIP2 TTIP3	E4 G4 J4 L4	O	**Transmit Positive Analog Output (TTIPn):** TTIP is the positive differential output to the line interface. This output pin, along with the corresponding TRING output pin, function as the Transmit DS1/E1 output signal drivers for the XRT86VL34 device. The user is expected to connect this signal and the corresponding TRING output signal to a 1:2 step up transformer for proper operation. This output pin will be tri-stated whenever the user sets the "TxON" input pin or register bit (0xnF02, bit 3) to "0". ***NOTE:*** *This pin should have a series line capacitor of 0.68µF for DC blocking purposes.*
TRING0 TRING1 TRING2 TRING3	F4 H4 K4 M4	O	**Transmit Negative Analog Output (TRINGn):** TRING is the negative differential output to the line interface. This output pin, along with the corresponding TTIP output pin, function as the Transmit DS1/E1 output signal drivers for the XRT86VL34 device. The user is expected to connect this signal and the corresponding TRING output signal to a 1:2 step up transformer for proper operation. ***NOTE:*** *This output pin will be tri-stated whenever the user sets the "TxON" input pin or register bit (0xnF02, bit 3) to "0".*
TxON	N1	I	**Transmitter On** This input pin permits the user to either enable or disable the Transmit Output Driver within the Transmit DS1/E1 LIU Block. If the TxON pin is pulled "Low", all 8 Channels are tri-stated. When this pin is pulled 'High', turning on or off the transmitters will be determined by the appropriate channel registers (address 0x0Fn2, bit 3) **LOW** = Disables the Transmit Output Driver within the Transmit DS1/E1 LIU Block. In this setting, the TTIP and TRING output pins of all 8 channels will be tri-stated. **HIGH** = Enables the Transmit Output Driver within the Transmit DS1/E1 LIU Block. In this setting, the corresponding TTIP and TRING output pins will be enabled or disabled by programming the appropriate channel register. (address 0x0Fn2, bit 3) ***NOTE:*** *Whenever the transmitters are turned off, the TTIP and TRING output pins will be tri-stated.*

TIMING INTERFACE

SIGNAL NAME	BALL #	TYPE	OUTPUT DRIVE (mA)	DESCRIPTION
MCLKIN	A4	I	-	**Master Clock Input:** This pin is used to provide the timing reference for the internal master clock of the device. The frequency of this clock is programmable from 8kHz to 16.384MHz in register 0x0FE9.
E1MCLKnOUT	A3	O	12	**LIU E1 Output Clock Reference** This output pin is defaulted to 2.048MHz, but can be programmed to 4.096MHz, 8.192MHz, or 16.384MHz in register 0x0FE4.

TIMING INTERFACE

SIGNAL NAME	BALL #	TYPE	OUTPUT DRIVE (MA)	DESCRIPTION
T1MCLKnOUT	B4	O	12	**LIU T1 Output Clock Reference** This output pin is defaulted to 1.544MHz, but can be programmed to output 3.088MHz, 6.176MHz, or 12.352MHz in register 0x0FE4.
E1OSCCLK	P2	O	8	**Framer E1 Output Clock Reference** This output pin is defaulted to 2.048MHz, but can be programmed to 65.536MHz in register 0x011E.
T1OSCCLK	P4	O	8	**Framer T1 Output Clock Reference** This output pin is defaulted to 1.544MHz, but can be programmed to output 49.408MHz in register 0x011E.
8KSYNC	R2	O	8	**8kHz Clock Output Reference** This pin is an output reference of 8kHz based on the MCLKIN input. Therefore, the duty cycle of this output is determined by the time period of the input clock reference.
8KEXTOSC	N4	I	-	**External Oscillator Select** For normal operation, this pin should not be used, or pulled “Low”. This pin is internally pulled “Low” with a 50kΩ resistor.
ANALOG	E5	O		**Factory Test Mode Pin** ***NOTE:*** *For Internal Use Only*
LOP	N2	I	-	**Loss of Power for E1 Only** This is a Loss of Power pin in the E1 application only. Upon detecting LOP in E1 mode, the device will automatically transmit the Sa5 and Sa6 bit to a different pattern, so that the Receive terminal can detect a power failure in the network. Please see register 0xn131 for the Transmit SA control.

JTAG INTERFACE

The XRT86VL34 device's JTAG features comply with the IEEE 1149.1 standard. Please refer to the industry specification for additional information on boundary scan operations.

SIGNAL NAME	BALL #	TYPE	OUTPUT DRIVE (mA)	DESCRIPTION
TCK	C7	I	-	**Test clock: Boundary Scan Test clock input:** The TCLK signal is the clock for the TAP controller, and it generates the boundary scan data register clocking. The data on TMS and TDI is loaded on the positive edge of TCK. Data is observed at TDO on the falling edge of TCK.
TMS	C6	I	-	**Test Mode Select:** Boundary Scan Test Mode Select input. The TMS signal controls the transitions of the TAP controller in conjunction with the rising edge of the test clock (TCK). ***NOTE:*** *For normal operation this pin MUST be pulled "High".*
TDI	B6	I	-	**Test Data In:** Boundary Scan Test data input The TDI signal is the serial test data input. ***NOTE:*** *This pin is internally pulled 'high'.*
TDO	D5	O	8	**Test Data Out:** Boundary Scan Test data output The TDO signal is the serial test data output.
TRST	A6	I	-	**Test Reset Input:** The TRST signal (Active Low) asynchronously resets the TAP controller to the Test-Logic-Reset state. ***NOTE:*** *This pin is internally pulled 'high'*
TESTMODE	B11	I	-	**Factory Test Mode Pin** ***NOTE:*** *This pin is internally pulled 'low', and should be pulled 'low' for normal operation.*
aTESTMODE	B5	I	-	**Factory Test Mode Pin** ***NOTE:*** *This pin is internally pulled 'low', and should be pulled 'low' for normal operation.*
ATP_Ring	B2	I	-	**ATP_Ring Test Pin** This analog test pin is used for testing the continuity between the TTIP/TRING, RTIP/RRING of each channel and the on-board transformer.
ATP_Tip	C3	I	-	**ATP_Tip Test Pin** This analog test pin is used for testing the continuity between the TTIP/TRING, RTIP/RRING of each channel and the on-board transformer.

MICROPROCESSOR INTERFACE

SIGNAL NAME	BALL #	TYPE	OUTPUT DRIVE (MA)	DESCRIPTION
DATA0 DATA1 DATA2 DATA3 DATA4 DATA5 DATA6 DATA7	T4 U3 V8 V9 T10 V10 U11 R11	I/O	8	**Bidirectional Microprocessor Data Bus** These pins are used to drive and receive data over the bi-directional data bus, whenever the Microprocessor performs READ or WRITE operations with the Microprocessor Interface of the XRT86VL34 device. When DMA interface is enabled, these 8-bit bidirectional data bus is also used by the T1/E1 Framer or the external DMA Controller for storing and retrieving information.
$\overline{\text{REQ0}}$	R1	O	8	**DMA Cycle Request Output—DMA Controller 0 (Write)**: These output pins are used to indicate that DMA transfers (Write) are requested by the T1/E1 Framer. On the transmit side (i.e., To transmit data from external DMA controller to HDLC buffers within the XRT86VL34), DMA transfers are only requested when the transmit buffer status bits indicate that there is space for a complete message or cell. The DMA Write cycle starts by T1/E1 Framer asserting the DMA Request ($\overline{\text{REQ0}}$) 'low', then the external DMA controller should drive the DMA Acknowledge ($\overline{\text{ACK0}}$) 'low' to indicate that it is ready to start the transfer. The external DMA controller should place new data on the Microprocessor data bus each time the Write Signal is Strobed low if the $\overline{\text{WR}}$ is configured as a Write Strobe. If $\overline{\text{WR}}$ is configured as a direction signal, then the external DMA controller would place new data on the Microprocessor data bus each time the Read Signal ($\overline{\text{RD}}$) is Strobed low. The Framer asserts this output pin (toggles it "Low") when at least one of the Transmit HDLC buffers are empty and can receive one more HDLC message. The Framer negates this output pin (toggles it "High") when the HDLC buffer can no longer receive another HDLC message.

MICROPROCESSOR INTERFACE

SIGNAL NAME	BALL #	TYPE	OUTPUT DRIVE (MA)	DESCRIPTION
$\overline{REQ1}$	R3	O	8	**DMA Cycle Request Output—DMA Controller 1 (Read):** These output pins are used to indicate that DMA transfers (Read) are requested by the T1/E1 Framer. On the receive side (i.e., To transmit data from HDLC buffers within the XRT86VL34 to external DMA Controller), DMA transfers are only requested when the receive buffer contains a complete message or cell. The DMA Read cycle starts by T1/E1 Framer asserting the DMA Request ($\overline{REQ1}$) 'low', then the external DMA controller should drive the DMA Acknowledge ($\overline{ACK1}$) 'low' to indicate that it is ready to receive the data. The T1/E1 Framer should place new data on the Microprocessor data bus each time the Read Signal is Strobed low if the $\overline{RD}$ is configured as a Read Strobe. If $\overline{RD}$ is configured as a direction signal, then the T1/E1 Framer would place new data on the Microprocessor data bus each time the Write Signal ($\overline{WR}$) is Strobed low. The Framer asserts this output pin (toggles it "Low") when one of the Receive HDLC buffer contains a complete HDLC message that needs to be read by the µC/µP. The Framer negates this output pin (toggles it "High") when the Receive HDLC buffers are depleted.
$\overline{INT}$	R8	O	8	**Interrupt Request Output:** This active-low output signal will be asserted when the XRT86VL34 device is requesting interrupt service from the Microprocessor. This output pin should typically be connected to the "Interrupt Request" input of the Microprocessor. The Framer will assert this active "Low" output (toggles it "Low"), to the local µP, anytime it requires interrupt service.
PCLK	V1	I	-	**Microprocessor Clock Input:** This clock input signal is only used if the Microprocessor Interface has been configured to operate in the Synchronous Modes (e.g., Power PC 403 Mode). If the Microprocessor Interface is configured to operate in this mode, then it will use this clock signal to do the following. **1.** To sample the CS*, WR*/R/W*, A[14:0], D[7:0], RD*/DS* and DBEN input pins, and **2.** To update the state of the D[7:0] and the RDY/DTACK output signals. ***NOTES:*** *1. The Microprocessor Interface can work with PCLK frequencies ranging up to 33MHz.* *2. This pin is inactive if the user has configured the Microprocessor Interface to operate in either the Intel-Asynchronous or the Motorola-Asynchronous Modes. In this case, the user should tie this pin to GND.* When DMA interface is enabled, the PCLK input pin is also used by the T1/E1 Framer to latch in or latch out receive or output data respectively.
iADDR	U1	I	-	**This Pin Must be Tied "Low" for Normal Operation.** This pin is internally pulled "High" with a 50kΩ resistor.

MICROPROCESSOR INTERFACE

SIGNAL NAME	BALL #	TYPE	OUTPUT DRIVE (MA)	DESCRIPTION
fADDR	T1	I	-	**This Pin Must be Tied "High" for Normal Operation.** This pin is internally pulled "Low" with a 50kΩ resistor.
PTYPE0 PTYPE1 PTYPE2	V2 V4 T8	I	-	**Microprocessor Type Input:** These input pins permit the user to specify which type of Microprocessor/Microcontroller to be interfaced to the XRT86VL34 device. The following table presents the three different microprocessor types that the XRT86VL34 supports. **NOTE:** *These pins are internally pulled "Low" with a 50kΩ resistor.*

° PType2	° PType1	° PType0	MICROPROCESSOR TYPE
0	0	0	Intel Asynchronous
0	0	1	Motorola Asynchronous
1	0	1	IBM POWER PC 403

MICROPROCESSOR INTERFACE

SIGNAL NAME	BALL #	TYPE	OUTPUT DRIVE (MA)	DESCRIPTION

$\overline{\text{RDY}}$	T3	O	12	**Ready/Data Transfer Acknowledge Output:**
				The exact behavior of this pin depends upon the type of Microprocessor/Microcontroller the XRT86VL34 has been configured to operate in, as defined by the PTYPE[2:0] pins.
				Intel Asynchronous Mode - RDY* - Ready Output
				Tis output pin will function as the “active-low” READY output.
				During a READ or WRITE cycle, the Microprocessor Interface block will toggle this output pin to the logic low level, ONLY when the Microprocessor Interface is ready to complete or terminate the current READ or WRITE cycle. Once the Microprocessor has determined that this input pin has toggled to the logic “low” level, then it is now safe for it to move on and execute the next READ or WRITE cycle.
				If (during a READ or WRITE cycle) the Microprocessor Interface block is holding this output pin at a logic “high” level, then the Microprocessor is expected to extend this READ or WRITE cycle, until it detects this output pin being toggled to the logic low level.
				Motorola Asynchronous Mode - DTACK* - Data Transfer Acknowledge Output
				Tis output pin will function as the “active-low” DTACK output.
				During a READ or WRITE cycle, the Microprocessor Interface block will toggle this output pin to the logic low level, ONLY when the Microprocessor Interface is ready to complete or terminate the current READ or WRITE cycle. Once the Microprocessor has determined that this input pin has toggled to the logic “low” level, then it is now safe for it to move on and execute the next READ or WRITE cycle.
				If (during a READ or WRITE cycle) the Microprocessor Interface block is holding this output pin at a logic “high” level, then the Microprocessor is expected to extend this READ or WRITE cycle, until it detects this output pin being toggled to the logic low level.
				Power PC 403 Mode - RDY Ready Output:
				This output pin will function as the “active-high” READY output.
				During a READ or WRITE cycle, the Microprocessor Interface block will toggle this output pin to the logic high level, ONLY when the Microprocessor Interface is ready to complete or terminate the current READ or WRITE cycle. Once the Microprocessor has sampled this signal being at the logic “high” level upon the rising edge of PCLK, then it is now safe for it to move on and execute the next READ or WRITE cycle.
				If (during a READ or WRITE cycle) the Microprocessor Interface block is holding this output pin at a logic “low” level, then the Microprocessor is expected to extend this READ or WRITE cycle, until it samples this output pin being at the logic low level.
				NOTE: *The Microprocessor Interface will update the state of this output pin upon the rising edge of PCLK.*

MICROPROCESSOR INTERFACE

SIGNAL NAME	BALL #	TYPE	OUTPUT DRIVE (MA)	DESCRIPTION
ADDR0 ADDR1 ADDR2 ADDR3 ADDR4 ADDR5 ADDR6 ADDR7 ADDR8 ADDR9 ADDR10 ADDR11 ADDR12 ADDR13	U5 V5 R5 T6 U6 V6 R6 T7 V7 U9 R7 R9 R10 V11	I	-	**Microprocessor Interface Address Bus Input** These pins permit the Microprocessor to identify on-chip registers and Buffer/Memory locations within the XRT86VL34 device whenever it performs READ and WRITE operations with the XRT86VL34 device. ***NOTE:*** *These pins are internally pulled "Low" with a 50kΩ resistor, except ADDR [8:13].*
$\overline{\text{DBEN}}$	U4	I	-	**Data Bus Enable Input pin.** This active-low input pin permits the user to either enable or tri-state the Bi-Directional Data Bus pins (D[7:0]), as described below. • Setting this input pin "low" enables the Bi-directional Data bus. • Setting this input pin "high" tri-states the Bi-directional Data Bus.
ALE	U8	I	-	**Address Latch Enable Input Address Strobe** The exact behavior of this pin depends upon the type of Microprocessor/Microcontroller the XRT86VL34 has been configured to operate in, as defined by the PTYPE[2:0] pins. **Intel-Asynchronous Mode - ALE** This active-high input pin is used to latch the address (present at the Microprocessor Interface Address Bus pins (A[14:0]) into the XRT86VL34 Microprocessor Interface block and to indicate the start of a READ or WRITE cycle. Pulling this input pin "high" enables the input bus drivers for the Address Bus input pins (A[14:0]). The contents of the Address Bus will be latched into the XRT86VL34 Microprocessor Interface circuitry, upon the falling edge of this input signal. **Motorola-Asynchronous (68K) Mode - AS*** This active-low input pin is used to latch the data residing on the Address Bus, A[14:0] into the Microprocessor Interface circuitry of the XRT86VL34 device. Pulling this input pin "low" enables the input bus drivers for the Address Bus input pins. The contents of the Address Bus will be latched into the Microprocessor Interface circuitry, upon the rising edge of this signal. **Power PC 403 Mode - No Function -Tie to GND:** This input pin has no role nor function and should be tied to GND.

MICROPROCESSOR INTERFACE

SIGNAL NAME	BALL #	TYPE	OUTPUT DRIVE (mA)	DESCRIPTION
$\overline{CS}$	V13	I	-	**Microprocessor Interface—Chip Select Input:** The user must assert this active low signal in order to select the Microprocessor Interface for READ and WRITE operations between the Microprocessor and the XRT86VL34 on-chip registers and buffer/memory locations.
$\overline{RD}$	V3	I	-	**Microprocessor Interface—Read Strobe Input:** The exact behavior of this pin depends upon the type of Microprocessor/Microcontroller the Framer has been configured to operate in, as defined by the PTYPE[2:0] pins. **Intel-Asynchronous Mode - RD* - READ Strobe Input:** This input pin will function as the RD* (Active Low Read Strobe) input signal from the Microprocessor. Once this active-low signal is asserted, then the XRT86VL34 device will place the contents of the addressed register (or buffer location) on the Microprocessor Interface Bi-directional data bus (D[7:0]). When this signal is negated, then the Data Bus will be tri-stated. **Motorola-Asynchronous (68K) Mode - DS* - Data Strobe:** This input pin will function as the DS* (Data Strobe) input signal. **Power PC 403 Mode - WE* - Write Enable Input:** This input pin will function as the WE* (Write Enable) input pin. Anytime the Microprocessor Interface samples this active-low input signal (along with CS* and WR/R/W*) also being asserted (at a logic low level) upon the rising edge of PCLK, then the Microprocessor Interface will (upon the very same rising edge of PCLK) latch the contents on the Bi-Directional Data Bus (D[7:0]) into the “target” on-chip register or buffer location within the XRT86VL34 device.

MICROPROCESSOR INTERFACE

SIGNAL NAME	BALL #	TYPE	OUTPUT DRIVE (MA)	DESCRIPTION
$\overline{WR}$	V12	I	-	**Microprocessor Interface—Write Strobe Input** The exact behavior of this pin depends upon the type of Microprocessor/Microcontroller the XRT86VL34 has been configured to operate in, as defined by the PTYPE[2:0] pins. **Intel-Asynchronous Mode - WR* - Write Strobe Input:** This input pin functions as the WR* (Active Low WRITE Strobe) input signal from the Microprocessor. Once this active-low signal is asserted, then the input buffers (associated with the Bi-Directional Data Bus pin, D[7:0]) will be enabled. The Microprocessor Interface will latch the contents on the Bi-Directional Data Bus (into the "target" register or address location, within the XRT86VL34) upon the rising edge of this input pin. **Motorola-Asynchronous Mode - R/W* - Read/Write Operation Identification Input Pin:** This pin is functionally equivalent to the "R/W*" input pin. In the Motorola Mode, a "READ" operation occurs if this pin is held at a logic "1", coincident to a falling edge of the RD/DS* (Data Strobe) input pin. Similarly a WRITE operation occurs if this pin is at a logic "0", coincident to a falling edge of the RD/DS* (Data Strobe) input pin. **Power PC 403 Mode - R/W* - Read/Write Operation Identification Input:** This input pin will function as the "Read/Write Operation Identification Input" pin. Anytime the Microprocessor Interface samples this input signal at a logic low (while also sampling the CS* input pin "low") upon the rising edge of PCLK, then the Microprocessor Interface will (upon the very same rising edge of PCLK) latch the contents of the Address Bus (A[14:0]) into the Microprocessor Interface circuitry, in preparation for this forthcoming READ operation. At some point (later in this READ operation) the Microprocessor will also assert the DBEN*/OE* input pin, and the Microprocessor Interface will then place the contents of the "target" register (or address location within the XRT86VL34 device) upon the Bi-Directional Data Bus pins (D[7:0]), where it can be read by the Microprocessor. Anytime the Microprocessor Interface samples this input signal at a logic high (while also sampling the CS* input pin a logic "low") upon the rising edge of PCLK, then the Microprocessor Interface will (upon the very same rising edge of PCLK) latch the contents of the Address Bus (A[14:0]) into the Microprocessor Interface circuitry, in preparation for the forthcoming WRITE operation. At some point (later in this WRITE operation) the Microprocessor will also assert the RD*/DS*/WE* input pin, and the Microprocessor Interface will then latch the contents of the Bi-Directional Data Bus (D[7:0]) into the contents of the "target" register or buffer location (within the XRT86VL34).

MICROPROCESSOR INTERFACE

SIGNAL NAME	BALL #	TYPE	OUTPUT DRIVE (mA)	DESCRIPTION
$\overline{ACK0}$ $\overline{ACK1}$	T2 U2	I	-	**DMA Cycle Acknowledge Input—DMA Controller 0 (Write):** The external DMA Controller will assert this input pin "Low" when the following two conditions are met: **1.** After the DMA Controller, within the Framer has asserted (toggled "Low"), the Req_0 output signal. **2.** When the external DMA Controller is ready to transfer data from external memory to the selected Transmit HDLC buffer. At this point, the DMA transfer between the external memory and the selected Transmit HDLC buffer may begin. After completion of the DMA cycle, the external DMA Controller will negate this input pin after the DMA Controller within the Framer has negated the $\overline{Req\_0}$ output pin. The external DMA Controller must do this in order to acknowledge the end of the DMA cycle. **DMA Cycle Acknowledge Input—DMA Controller 1 (Read):** The external DMA Controller asserts this input pin "Low" when the following two conditions are met: **1.** After the DMA Controller, within the Framer has asserted (toggled "Low"), the Req_1 output signal. **2.** When the external DMA Controller is ready to transfer data from the selected Receive HDLC buffer to external memory. At this point, the DMA transfer between the selected Receive HDLC buffer and the external memory may begin. After completion of the DMA cycle, the external DMA Controller will negate this input pin after the DMA Controller within the Framer has negated the $\overline{Req\_1}$ output pin. The external DMA Controller will do this in order to acknowledge the end of the DMA cycle. ***NOTE:*** *This pin is internally pulled "High" with a 50kΩ resistor.*
$\overline{BLAST}$	U10	I	-	**Last Cycle of Burst Indicator Input:** If the Microprocessor Interface is operating in the Intel-I960 Mode, then this input pin is used to indicate (to the Microprocessor Interface block) that the current data transfer is the last data transfer within the current burst operation. The Microprocessor should assert this input pin (by toggling it "Low") in order to denote that the current READ or WRITE operation (within a BURST operation) is the last operation of this BURST operation. ***NOTES:*** *1. If the user has configured the Microprocessor Interface to operate in the Intel-Asynchronous, the Motorola-Asynchronous or the Power PC 403 Mode, then he/she should tie this input pin to GND.* *2. This pin is internally pulled "High" with a 50kΩ resistor.*

MICROPROCESSOR INTERFACE

SIGNAL NAME	BALL #	TYPE	OUTPUT DRIVE (MA)	DESCRIPTION
$\overline{\text{RESET}}$	P1	I	-	**Hardware Reset Input** $\overline{\text{Reset}}$ is an active low input. If this pin is pulled "Low" for more than 10µS, the device will be reset. When this occurs, all output will be 'tri-stated', and all internal registers will be reset to their default values.

POWER SUPPLY PINS (3.3V)

SIGNAL NAME	BALL #	TYPE	DESCRIPTION
VDD	D16 P3 R15 T9	PWR	**Framer Block Power Supply (I/O)**
RVDD	E3 G3 J3 L3	PWR	**Receiver Analog Power Supply for LIU Section**
TVDD	F3 H3 K3 M3	PWR	**Transmitter Analog Power Supply for LIU Section**

POWER SUPPLY PINS (1.8V)

SIGNAL NAME	BALL #	TYPE	DESCRIPTION
DVDD18	B8 C4 J16 R13 U7	PWR	**Digital Power Supply for LIU Section**
AVDD18	A2	PWR	**Analog Power Supply for LIU Section**
VDDPLL18	B1 C2 D2 D3	PWR	**Analog Power Supply for PLL**

GROUND PINS

SIGNAL NAME	BALL #	TYPE	DESCRIPTION
VSS	A5 B14 C16 M15 M16 R4 T5 U16	GND	**Framer Block Ground**
DGND	C5	GND	**Digital Ground for LIU Section**
AGND	B3	GND	**Analog Ground for LIU Section**
RGND	E2 G2 J2 L2	GND	**Receiver Analog Ground for LIU Section**
TGND	F2 H2 K2 M2	GND	**Transmitter Analog Ground for LIU Section**
GNDPLL18	A1 C1 D1 D4	GND	**Analog Ground for PLL**

ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUMS

Power Supply.....		Power Rating PBGA Package..... 1.39W (at zero airflow)
VDD_{IO} .. .. -0.5V to +3.465V		
VDD_{CORE}.....-0.5V to +1.890V		
Storage Temperature .....-65°C to 150°C		Input Logic Signal Voltage (Any Pin) .....-0.5V to + 5.5V
Operating Temperature Range.....-40°C to 85°C		ESD Protection (HBM).....>2000V
Supply Voltage ..... GND-0.5V to +VDD + 0.5V		Input Current (Any Pin) ..... ± 100mA

DC ELECTRICAL CHARACTERISTICS

Test Conditions: TA = 25°C, VDD_{IO} = 3.3V ± 5% , VDD_{CORE} = 1.8V ± 5%unless otherwise specified

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNITS	CONDITIONS
I_{LL}	Data Bus Tri-State Bus Leakage Current	-10		+10	µA	
V_{IL}	Input Low voltage			0.8	V	
V_{IH}	Input High Voltage	2.0		VDD	V	
V_{OL}	Output Low Voltage	0.0		0.4	V	I_{OL} = -1.6mA
VOH	Output High Voltage	2.4		VDD	V	I_{OH} = 40µA
I_{OC}	Open Drain Output Leakage Current				µA	
I_{IH}	Input High Voltage Current	-10		10	µA	V_{IH} = VDD
I_{IL}	Input Low Voltage Current	-10		10	µA	V_{IL} = GND

TABLE 4: XRT86VL34 POWER CONSUMPTION

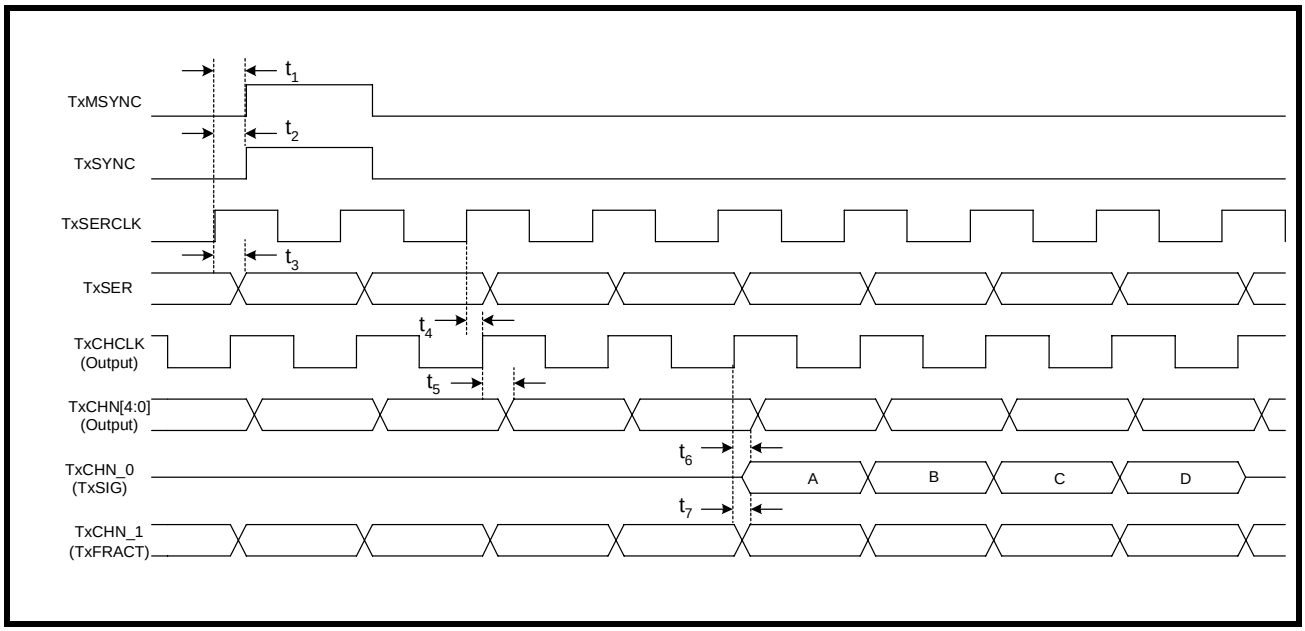
VDD_{IO} = 3.3V ± 5% , VDD_{CORE} = 1.8V ± 5%, T_A=25°C, UNLESS OTHERWISE SPECIFIED

MODE	SUPPLY VOLTAGE	IMPEDANCE	TERMINATION RESISTOR	TRANSFORMER RATIO		TYP.	MAX.	UNIT	TEST CONDITIONS
				RECEIVER	TRANSMITTER				
E1	3.3V	75Ω	Internal	1:1	1:2	1.035		W	PRBS Pattern
E1	3.3V	120Ω	Internal	1:1	1:2	0.965		W	PRBS Pattern
T1	3.3V	100Ω	Internal	1:1	1:2	1.105		W	PRBS Pattern

AC ELECTRICAL CHARACTERISTICS TRANSMIT FRAMER (BASE RATE/NON-MUX)

Test Conditions: TA = 25°C, VDD = 3.3V ± 5% unless otherwise specified						
SYMBOL	**PARAMETER**	**MIN.**	**TYP.**	**MAX.**	**UNITS**	**CONDITIONS**
t_1	TxSERCLK to TxMSYNC delay			234	nS	
t_2	TxSERCLK to TxSYNC delay			230	nS	
t_3	TxSERCLK to TxSER data delay			230	nS	
t_4	Rising Edge of TxSERCLK to Rising Edge of TxCH-CLK			13	nS	
t_5	Rising Edge of TxCHCLK to Valid TxCHN[4:0] Data			6	nS	
t_6	TxSERCLK to TxSIG delay			230	nS	
t_7	TxSERCLK to TxFRACT delay			110	nS	

FIGURE 2. FRAMER SYSTEM TRANSMIT TIMING DIAGRAM (BASE RATE/NON-MUX)



AC ELECTRICAL CHARACTERISTICS RECEIVE FRAMER (BASE RATE/NON-MUX)

Test Conditions: TA = 25°C, VDD = 3.3V ± 5% unless otherwise specified

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNITS	CONDITIONS
RxSERCLK as an Output						
t_8	Rising Edge of RxSERCLK to Rising Edge of RxCASYNC			4	nS	
t_9	Rising Edge of RxSERCLK to Rising Edge of RxCRCSYNC			4	nS	
t_{10}	Rising Edge of RxSERCLK to Rising Edge of RxSYNC (RxSYNC as Output)			4	nS	
t_{11}	Rising Edge of RxSERCLK to Rising Edge of RxSER			6	nS	
t_{12}	Rising Edge of RxSERCLK to Rising Edge of Valid RxCHN[4:0] data			6	nS	
RxSERCLK as an Input						
t_{13}	Rising Edge of RxSERCLK to Rising Edge of RxCASYNC			8	nS	
t_{14}	Rising Edge of RxSERCLK to Rising Edge of RxCRCSYNC			8	nS	
t_{15}	Rising Edge of RxSERCLK to Rising Edge of RxSYNC (RxSYNC as Output)			10	nS	
t_{15}	Rising Edge of RxSERCLK to Rising Edge of RxSYNC (RxSYNC as Input)			230	nS	
t_{16}	Rising Edge of RxSERCLK to Rising Edge of RxSER			10	nS	
t_{17}	Rising Edge of RxSERCLK to Rising Edge of Valid RxCHN[4:0] data			9	nS	

FIGURE 3. FRAMER SYSTEM RECEIVE TIMING DIAGRAM (RXSERCLK AS AN OUTPUT)

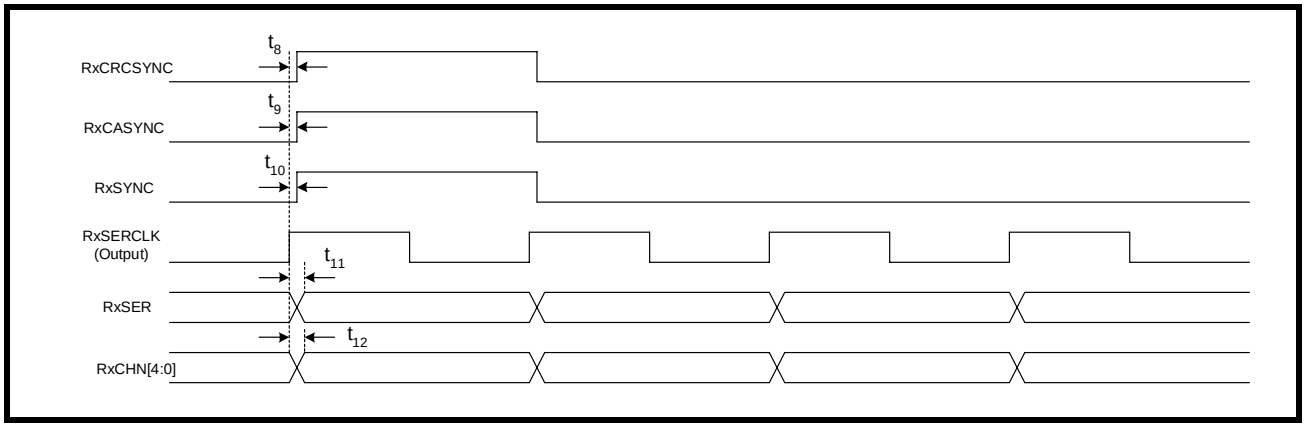
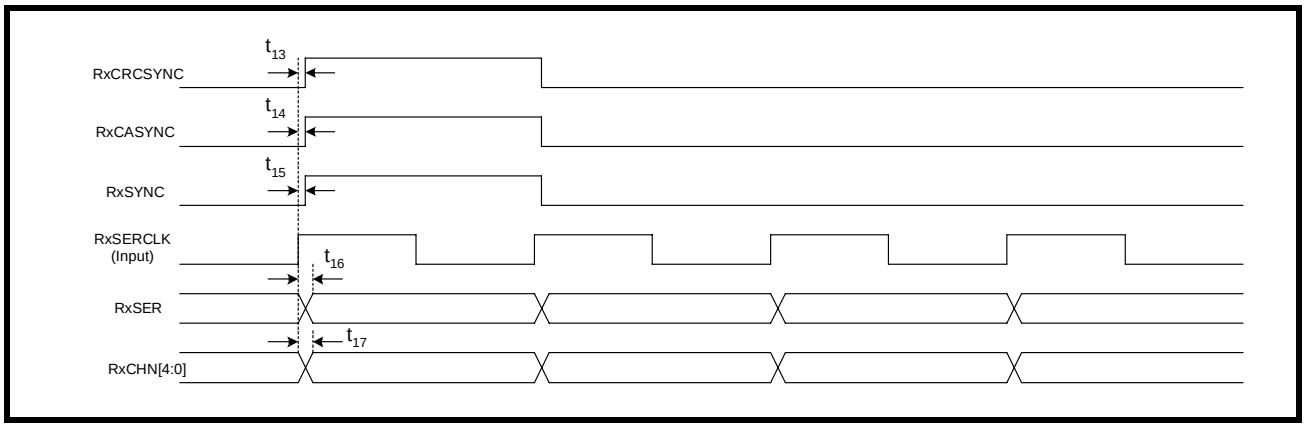


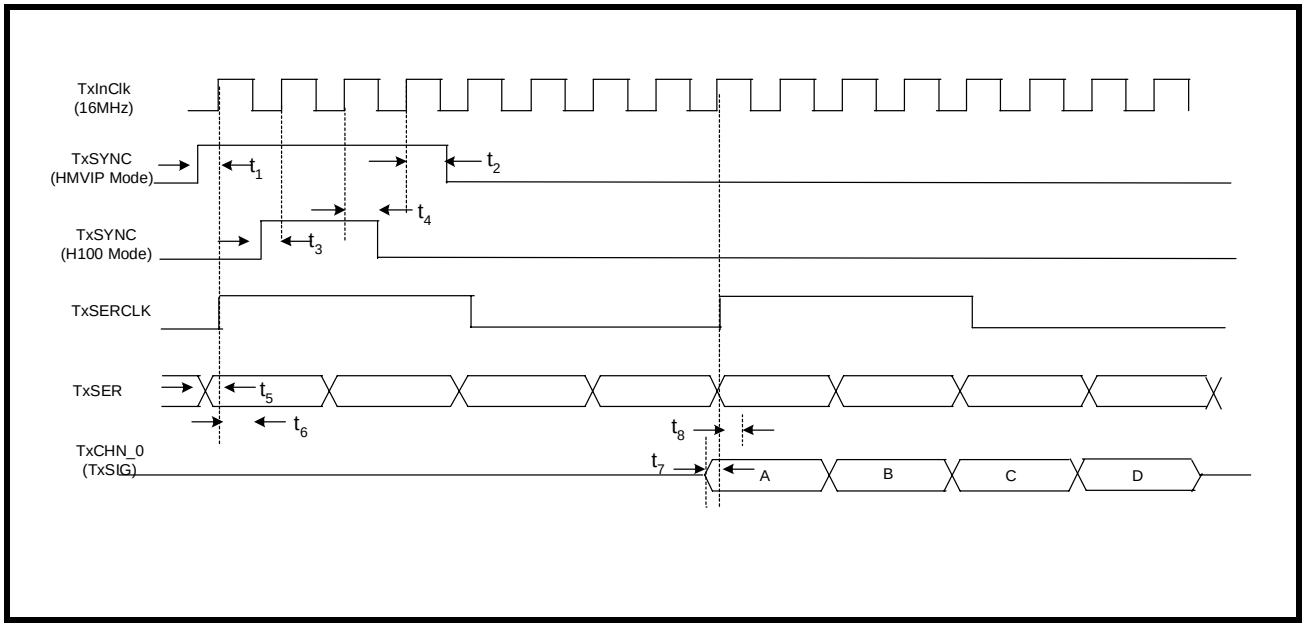
FIGURE 4. FRAMER SYSTEM RECEIVE TIMING DIAGRAM (RXSERCLK AS AN INPUT)



AC ELECTRICAL CHARACTERISTICS TRANSMIT FRAMER (HMVIP/H100 MODE)

Test Conditions: TA = 25°C, VDD = 3.3V ± 5% unless otherwise specified						
SYMBOL	**PARAMETER**	**MIN.**	**TYP.**	**MAX.**	**UNITS**	**CONDITIONS**
t_1	TxSYNC Setup Time - HMVIP Mode	7			nS	
t_2	TxSYNC Hold Time - HMVIP Mode	4			nS	
t_3	TxSYNC Setup Time - H100 Mode	7			nS	
t_4	TxSYNC Hold Time - H100 Mode	4			nS	
t_5	TxSER Setup Time - HMVIP and H100 Mode	6			nS	
t_6	TxSER Hold Time - HMVIP and H100 Mode	3			nS	
t_7	TxSIG Setup Time - HMVIP and H100 Mode	6			nS	
t_8	TxSIG Hold Time - HMVIP and H100 Mode	3			nS	

FIGURE 5. FRAMER SYSTEM TRANSMIT TIMING DIAGRAM (HMVIP AND H100 MODE)



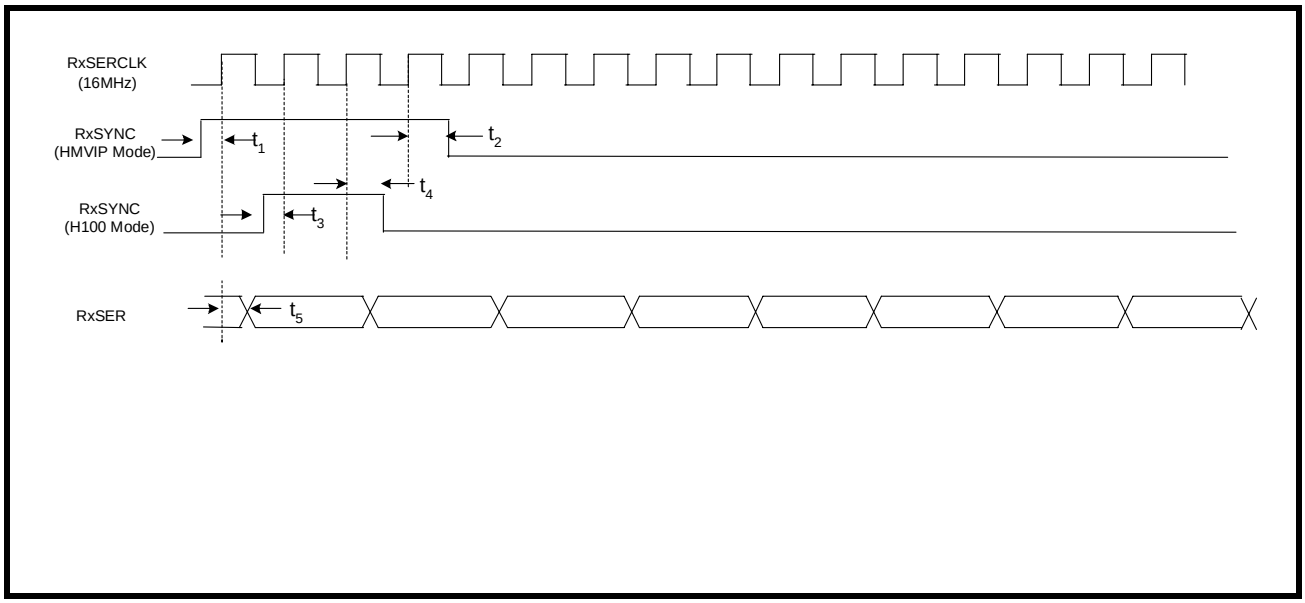
NOTE: *Setup and Hold time is not valid from TxInClk to TxSERCLK as TxInClk is used as the timing source for the back plane interface and TxSERCLK is used as the timing source on the line side.*

AC ELECTRICAL CHARACTERISTICS RECEIVE FRAMER (HMVIP/H100 MODE)

Test Conditions: TA = 25°C, VDD = 3.3V ± 5% unless otherwise specified						
SYMBOL	**PARAMETER**	**MIN.**	**TYP.**	**MAX.**	**UNITS**	**CONDITIONS**
t_1	RxSYNC Setup Time - HMVIP Mode	4			nS	
t_2	RxSYNC Hold Time - HMVIP Mode	3			nS	
t_3	RxSYNC Setup Time - H100 Mode	5			nS	
t_4	RxSYNC Hold Time - H100 Mode	3			nS	
t_5	Rising Edge of RxSERCLK to Rising Edge of RxSER delay			11	nS	

NOTE: *Both RxSERCLK and RxSYNC are inputs*

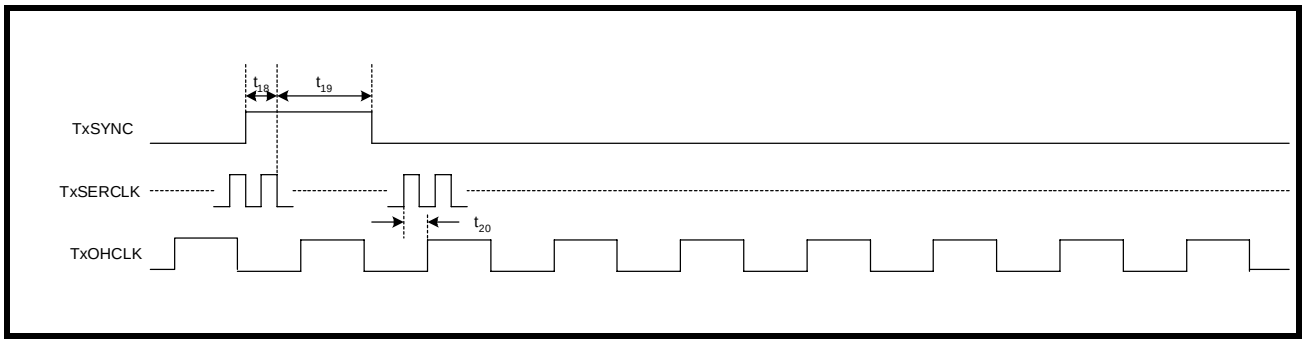
FIGURE 6. FRAMER SYSTEM RECEIVE TIMING DIAGRAM (HMVIP/H100 MODE)



AC ELECTRICAL CHARACTERISTICS TRANSMIT OVERHEAD FRAMER

Test Conditions: TA = 25°C, VDD = 3.3V ± 5% unless otherwise specified						
SYMBOL	**PARAMETER**	**MIN.**	**TYP.**	**MAX.**	**UNITS**	**CONDITIONS**
t_{18}	TxSYNC Setup Time (Falling Edge TxSERCLK)	6			nS	
t_{19}	TxSYNC Hold Time (Falling Edge TxSERCLK)	4			nS	
t_{20}	Rising Edge of TxSERCLK to TxOHCLK			12	nS	

FIGURE 7. FRAMER SYSTEM TRANSMIT OVERHEAD TIMING DIAGRAM



AC ELECTRICAL CHARACTERISTICS RECEIVE OVERHEAD FRAMER

Test Conditions: TA = 25°C, VDD = 3.3V ± 5% unless otherwise specified						
SYMBOL	**PARAMETER**	**MIN.**	**TYP.**	**MAX.**	**UNITS**	**CONDITIONS**
RxSERCLK as an Output						
t_{21}	Rising Edge of RxSERCLK to Rising Edge of RxSYNC (RxSYNC as Output)			4	nS	
t_{22}	Rising Edge of RxSERCLK to Rising Edge of RxOHCLK			6	nS	
t_{23}	Rising Edge of RxSERCLK to Rising Edge of RxOH			8	nS	
RxSERCLK as an Input						
t_{24}	Rising Edge of RxSERCLK to Rising Edge of RxSYNC (RxSYNC as Output)			12	nS	
t_{24}	Rising Edge of RxSERCLK to Rising Edge of RxSYNC (RxSYNC as Input)			230	nS	
t_{25}	Rising Edge of RxSERCLK to Rising Edge of RxOHCLK			12	nS	
t_{26}	Rising Edge of RxSERCLK to Rising Edge of RxOH			15	nS	

FIGURE 8. FRAMER SYSTEM RECEIVE OVERHEAD TIMING DIAGRAM (RXSERCLK AS AN OUTPUT)

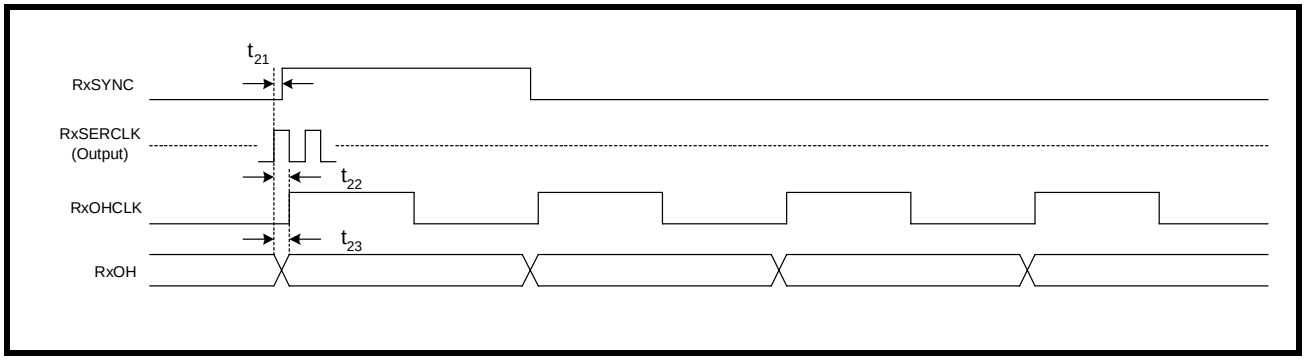


FIGURE 9. FRAMER SYSTEM RECEIVE OVERHEAD TIMING DIAGRAM (RXSERCLK AS AN INPUT)

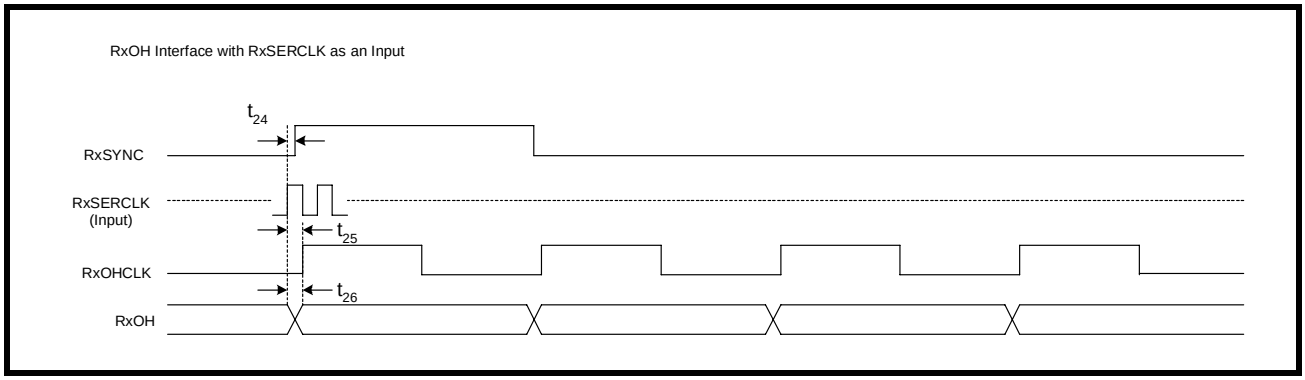


TABLE 5: E1 RECEIVER ELECTRICAL CHARACTERISTICS

VDD_{IO} = 3.3V ± 5% , VDD_{CORE} = 1.8V ± 5%, T_A= -40° to 85°C, unless otherwise specified					
PARAMETER	**MIN.**	**TYP.**	**MAX.**	**UNIT**	**TEST CONDITIONS**
Receiver loss of signal: Number of consecutive zeros before RLOS is set Input signal level at RLOS RLOS De-asserted	 15 12.5	 32 20		 dB % ones	Cable attenuation @1024kHz ITU-G.775, ETSI 300 233
Receiver Sensitivity (Short Haul with cable loss)	11			dB	With nominal pulse amplitude of 3.0V for 120Ω and 2.37V for 75Ω application.
Receiver Sensitivity (Long Haul with cable loss)	0		43	dB	With nominal pulse amplitude of 3.0V for 120Ω and 2.37V for 75Ω application.
Input Impedance		15		kΩ	
Input Jitter Tolerance: 1 Hz 10kHz-100kHz	 37 0.3			 UIpp UIpp	 ITU G.823
Recovered Clock Jitter Transfer Corner Frequency Peaking Amplitude	 -	 20	 0.5	 kHz dB	 ITU G.736
Jitter Attenuator Corner Frequency (-3dB curve) (JABW=0) (JABW=1)	-	10 1.5	-	Hz Hz	ITU G.736
Return Loss: 51kHz - 102kHz 102kHz - 2048kHz 2048kHz - 3072kHz	 12 8 8	 -	 -	 dB dB dB	 ITU-G.703

TABLE 6: T1 RECEIVER ELECTRICAL CHARACTERISTICS

VDD_{IO} = 3.3V ± 5% , VDD_{CORE} = 1.8V ± 5%, T_A=-40° to 85°C, unless otherwise specified					
PARAMETER	**MIN.**	**TYP.**	**MAX.**	**UNIT**	**TEST CONDITIONS**
Receiver loss of signal:					
Number of consecutive zeros before RLOS is set		175			
Input signal level at RLOS	15	20	-	dB	Cable attenuation @772kHz
RLOS Clear	12.5	-	-	% ones	ITU-G.775, ETSI 300 233
Receiver Sensitivity (Short Haul with cable loss)	12	-		dB	With nominal pulse amplitude of 3.0V for 100Ω termination
Receiver Sensitivity (Long Haul with cable loss)		-			With nominal pulse amplitude of 3.0V for 100Ω termination
Normal	0		36	dB	
Extended	0		45	dB	
Input Impedance		15	-	kΩ	
Jitter Tolerance:					
1Hz	138	-	-	UIpp	AT&T Pub 62411
10kHz - 100kHz	0.4	-	-		
Recovered Clock Jitter					
Transfer Corner Frequency	-	10	-	KHz	TR-TSY-000499
Peaking Amplitude	-		0.1	dB	
Jitter Attenuator Corner Frequency (-3dB curve)	-	3		Hz	AT&T Pub 62411
Return Loss:					
51kHz - 102kHz	-	14	-	dB	
102kHz - 2048kHz	-	20	-	dB	
2048kHz - 3072kHz	-	16	-	dB	

TABLE 7: E1 TRANSMITTER ELECTRICAL CHARACTERISTICS

VDD_{IO} = 3.3V ± 5% , VDD_{CORE} = 1.8V ± 5%, T_A=-40° to 85°C, unless otherwise specified					
PARAMETER	**MIN.**	**TYP.**	**MAX.**	**UNIT**	**TEST CONDITIONS**
AMI Output Pulse Amplitude:					1:2 transformer
75Ω Application	2.13	2.37	2.60	V	
120Ω Application	2.70	3.00	3.30	V	
Output Pulse Width	224	244	264	ns	
Output Pulse Width Ratio	0.95	-	1.05	-	ITU-G.703
Output Pulse Amplitude Ratio	0.95	-	1.05	-	ITU-G.703

TABLE 7: E1 TRANSMITTER ELECTRICAL CHARACTERISTICS

VDD_{IO} = 3.3V ± 5% , VDD_{CORE} = 1.8V ± 5%, T_A=-40° to 85°C, unless otherwise specified					
PARAMETER	**MIN.**	**TYP.**	**MAX.**	**UNIT**	**TEST CONDITIONS**
Jitter Added by the Transmitter Output	-	0.025	0.05	UIpp	Broad Band with jitter free TCLK applied to the input.
Output Return Loss: 51kHz -102kHz 102kHz-2048kHz 2048kHz-3072kHz	 15 9 8	 - - -	 - - -	 dB dB dB	 ETSI 300 166

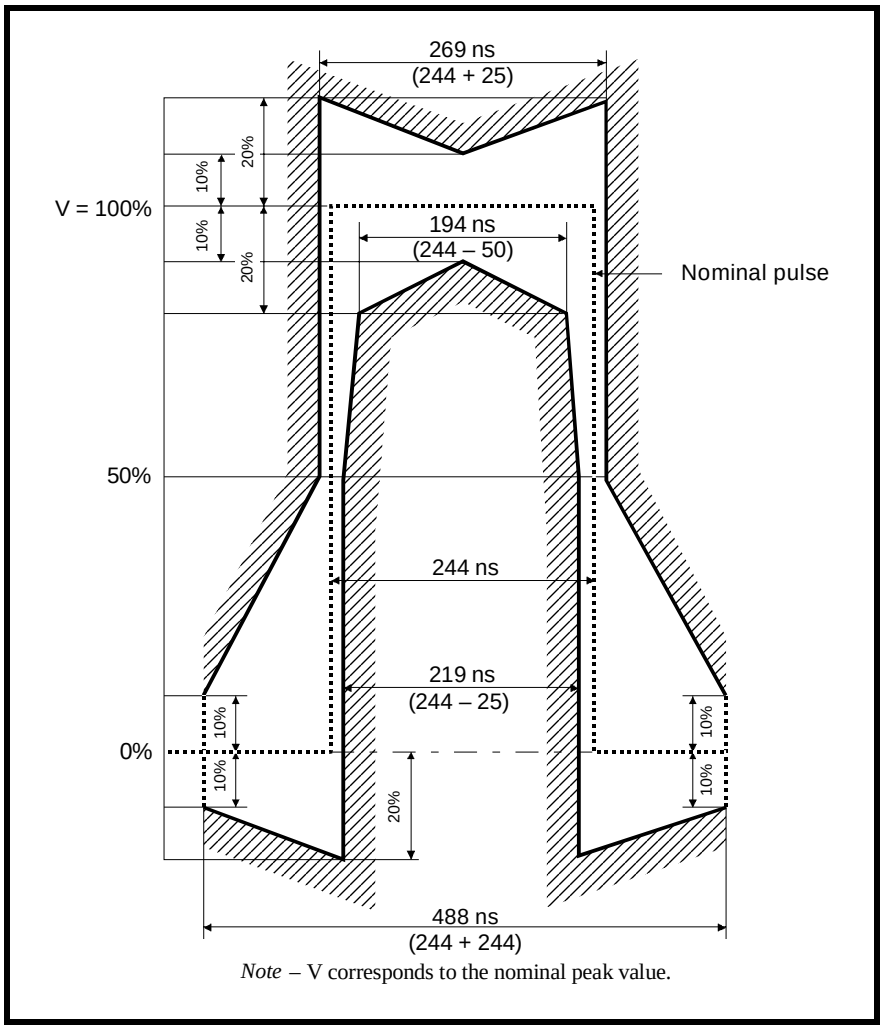
TABLE 8: E1 TRANSMIT RETURN LOSS REQUIREMENT

FREQUENCY	RETURN LOSS ETS 300166
51-102kHz	6dB
102-2048kHz	8dB
2048-3072kHz	8dB

TABLE 9: T1 TRANSMITTER ELECTRICAL CHARACTERISTICS

VDD_{IO} = 3.3V ± 5% , VDD_{CORE} = 1.8V ± 5%, T_A=-40° to 85°C, unless otherwise specified					
PARAMETER	**MIN.**	**TYP.**	**MAX.**	**UNIT**	**TEST CONDITIONS**
AMI Output Pulse Amplitude:	2.4	3.0	3.60	V	1:2 transformer measured at DSX-1.
Output Pulse Width	338	350	362	ns	ANSI T1.102
Output Pulse Width Imbalance	-	-	20	-	ANSI T1.102
Output Pulse Amplitude Imbalance	-	-	±200	mV	ANSI T1.102
Jitter Added by the Transmitter Output	-	0.025	0.05	UIpp	Broad Band with jitter free TCLK applied to the input.
Output Return Loss: 51kHz -102kHz 102kHz-2048kHz 2048kHz-3072kHz	 - - -	 17 12 10	 - - -	 dB dB dB	

FIGURE 10. ITU G.703 PULSE TEMPLATE



Note – V corresponds to the nominal peak value.

TABLE 10: TRANSMIT PULSE MASK SPECIFICATION

Test Load Impedance	75Ω Resistive (Coax)	120Ω Resistive (twisted Pair)
Nominal Peak Voltage of a Mark	2.37V	3.0V
Peak voltage of a Space (no Mark)	0 ± 0.237V	0 ± 0.3V
Nominal Pulse width	244ns	244ns
Ratio of Positive and Negative Pulses Imbalance	0.95 to 1.05	0.95 to 1.05

FIGURE 11. DSX-1 PULSE TEMPLATE (NORMALIZED AMPLITUDE)

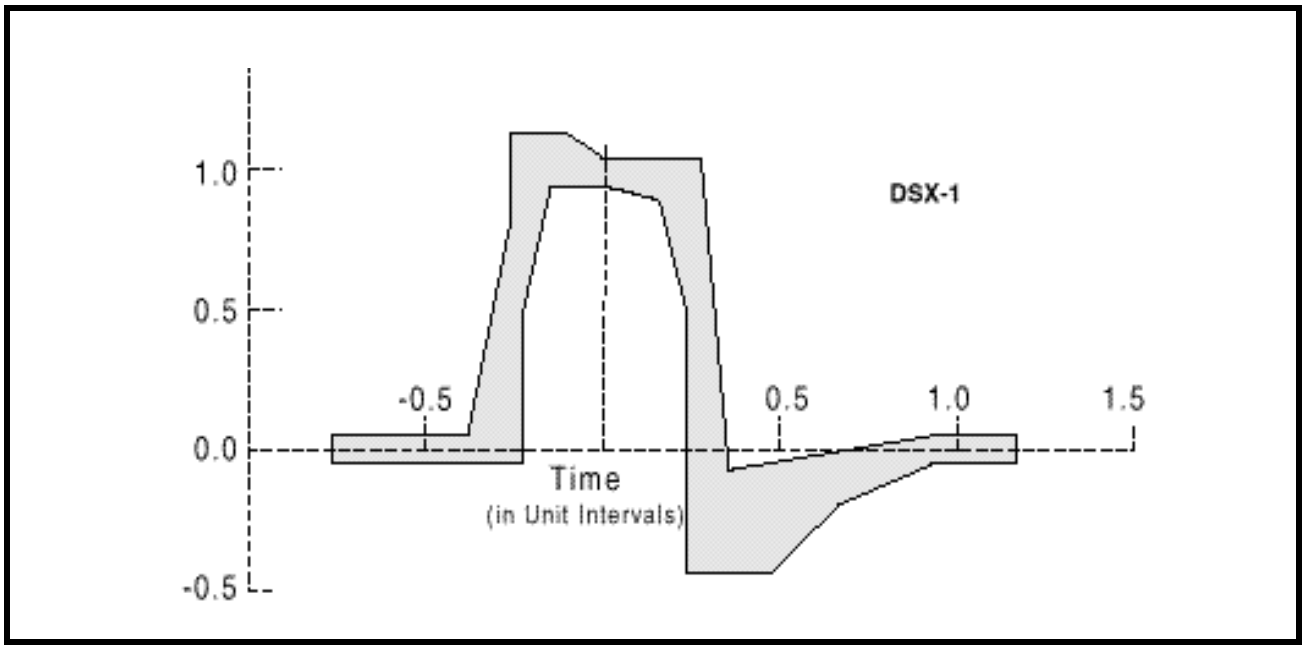


TABLE 11: DSX1 INTERFACE ISOLATED PULSE MASK AND CORNER POINTS

MINIMUM CURVE		MAXIMUM CURVE	
TIME (UI)	NORMALIZED AMPLITUDE	TIME (UI)	NORMALIZED AMPLITUDE
-0.77	-.05V	-0.77	.05V
-0.23	-.05V	-0.39	.05V
-0.23	0.5V	-0.27	.8V
-0.15	0.95V	-0.27	1.15V
0.0	0.95V	-0.12	1.15V
0.15	0.9V	0.0	1.05V
0.23	0.5V	0.27	1.05V
0.23	-0.45V	0.35	-0.07V
0.46	-0.45V	0.93	0.05V
0.66	-0.2V	1.16	0.05V
0.93	-0.05V		
1.16	-0.05V		

TABLE 12: AC ELECTRICAL CHARACTERISTICS

VDD_{IO} = 3.3V ± 5% , VDD_{CORE} = 1.8V ± 5%, TA=25°C, UNLESS OTHERWISE SPECIFIED					
PARAMETER	**SYMBOL**	**MIN.**	**TYP.**	**MAX.**	**UNITS**
MCLKIN Clock Duty Cycle		40	-	60	%
MCLKIN Clock Tolerance		-	±50	-	ppm

MICROPROCESSOR INTERFACE I/O TIMING

INTEL INTERFACE TIMING - ASYNCHRONOUS

The signals used for the Intel microprocessor interface are: Address Latch Enable (ALE), Read Enable ($\overline{RD}$), Write Enable ($\overline{WR}$), Chip Select ($\overline{CS}$), Address and Data bits. The microprocessor interface uses minimum external glue logic and is compatible with the timings of the 8051 or 80188 family of microprocessors. The ALE signal can be tied 'HIGH' if this signal is not available, and the corresponding timing interface is shown in **Figure 12** and **Table 13.**

FIGURE 12. INTEL µP INTERFACE TIMING DURING PROGRAMMED I/O READ AND WRITE OPERATIONS WHEN ALE IS NOT TIED 'HIGH'

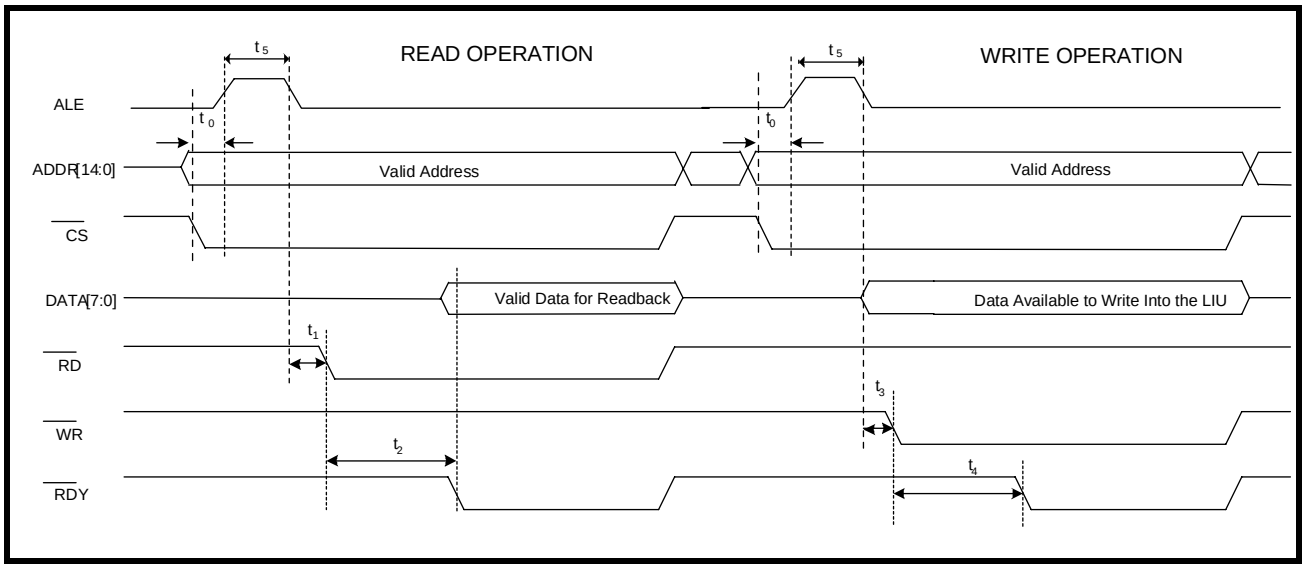


TABLE 13: INTEL MICROPROCESSOR INTERFACE TIMING SPECIFICATIONS

SYMBOL	PARAMETER	MIN	MAX	UNITS
t_0	Valid Address to $\overline{CS}$ Falling Edge and ALE Rising Edge	0	-	ns
t_1	ALE Falling Edge to $\overline{RD}$ Assert	5	-	ns
t_2	$\overline{RD}$ Assert to $\overline{RDY}$ Assert	-	320	ns
NA	$\overline{RD}$ Pulse Width (t_2)	320	-	ns
t_3	ALE Falling Edge to $\overline{WR}$ Assert	5	-	ns
t_4	$\overline{WR}$ Assert to $\overline{RDY}$ Assert	-	320	ns
NA	$\overline{WR}$ Pulse Width (t_4)	320	-	ns
t_5	ALE Pulse Width(t_5)	10		ns

FIGURE 13. INTEL µP INTERFACE TIMING DURING PROGRAMMED I/O READ AND WRITE OPERATIONS WHEN ALE IS TIED 'HIGH'

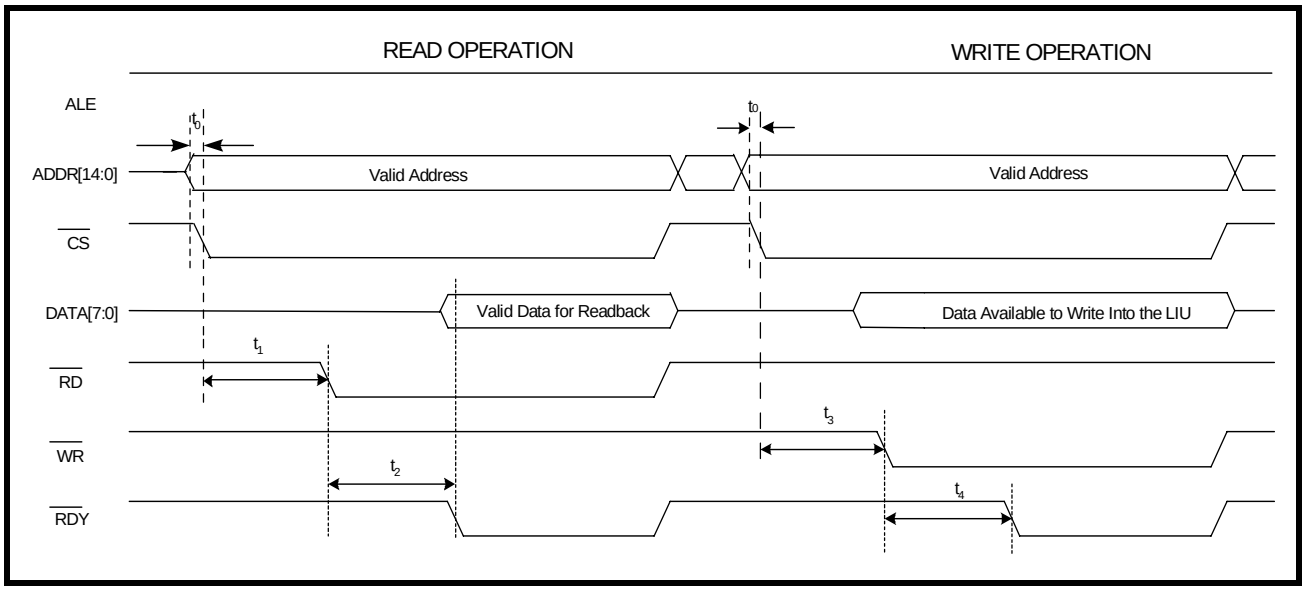


TABLE 14: INTEL MICROPROCESSOR INTERFACE TIMING SPECIFICATIONS

SYMBOL	PARAMETER	MIN	MAX	UNITS
t_0	Valid Address to $\overline{CS}$ Falling Edge	0	-	ns
t_1	$\overline{CS}$ Falling Edge to $\overline{RD}$ Assert	0	-	ns
t_2	$\overline{RD}$ Assert to $\overline{RDY}$ Assert	-	320	ns
NA	$\overline{RD}$ Pulse Width (t_2)	320	-	ns
t_3	$\overline{CS}$ Falling Edge to $\overline{WR}$ Assert	0	-	ns
t_4	$\overline{WR}$ Assert to $\overline{RDY}$ Assert	-	320	ns
NA	$\overline{WR}$ Pulse Width (t_4)	320	-	ns

MOTOROLA ASYCHRONOUS INTERFACE TIMING

The signals used in the Motorola microprocessor interface mode are: Address Strobe (AS), Data Strobe ($\overline{DS}$), Read/Write Enable (R/$\overline{W}$), Chip Select ($\overline{CS}$), Address and Data bits. The interface is compatible with the timing of a Motorola 68000 microprocessor family. The interface timing is shown in **Figure 14**. The I/O specifications are shown in **Table 15**.

FIGURE 14. MOTOROLA ASYCHRONOUS MODE INTERFACE SIGNALS DURING PROGRAMMED I/O READ AND WRITE OPERATIONS

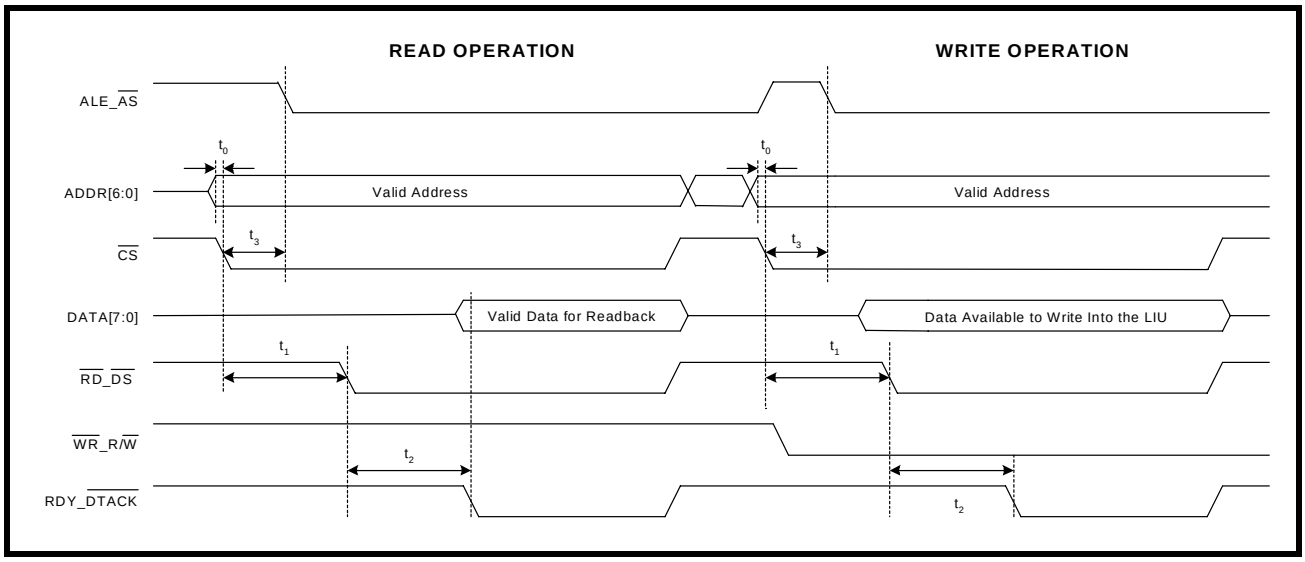


TABLE 15: MOTOROLA ASYCHRONOUS MODE MICROPROCESSOR INTERFACE TIMING SPECIFICATIONS

SYMBOL	PARAMETER	MIN	MAX	UNITS
t_0	Valid Address to $\overline{CS}$ Falling Edge	0	-	ns
t_1	$\overline{CS}$ Falling Edge to $\overline{DS}$ (Pin $\overline{RD}\_\overline{DS}$) Assert	0	-	ns
t_2	$\overline{DS}$ Assert to $\overline{DTACK}$ Assert	-	320	ns
NA	$\overline{DS}$ Pulse Width (t_2)	320	-	ns
t_3	$\overline{CS}$ Falling Edge to $\overline{AS}$ (Pin ALE_AS) Falling Edge	0	-	ns

POWER PC 403 SYCHRONOUS INTERFACE TIMING

The signals used in the Power PC 403 Synchronus microprocessor interface mode are: Address Strobe (AS), Microprocessor Clock (uPCLK), Data Strobe ($\overline{DS}$), Read/Write Enable (R/$\overline{W}$), Chip Select ($\overline{CS}$), Address and Data bits. The interface timing is shown in **Figure 15**. The I/O specifications are shown in **Table 16**.

FIGURE 15. POWER PC 403 INTERFACE SIGNALS DURING PROGRAMMED I/O READ AND WRITE OPERATIONS

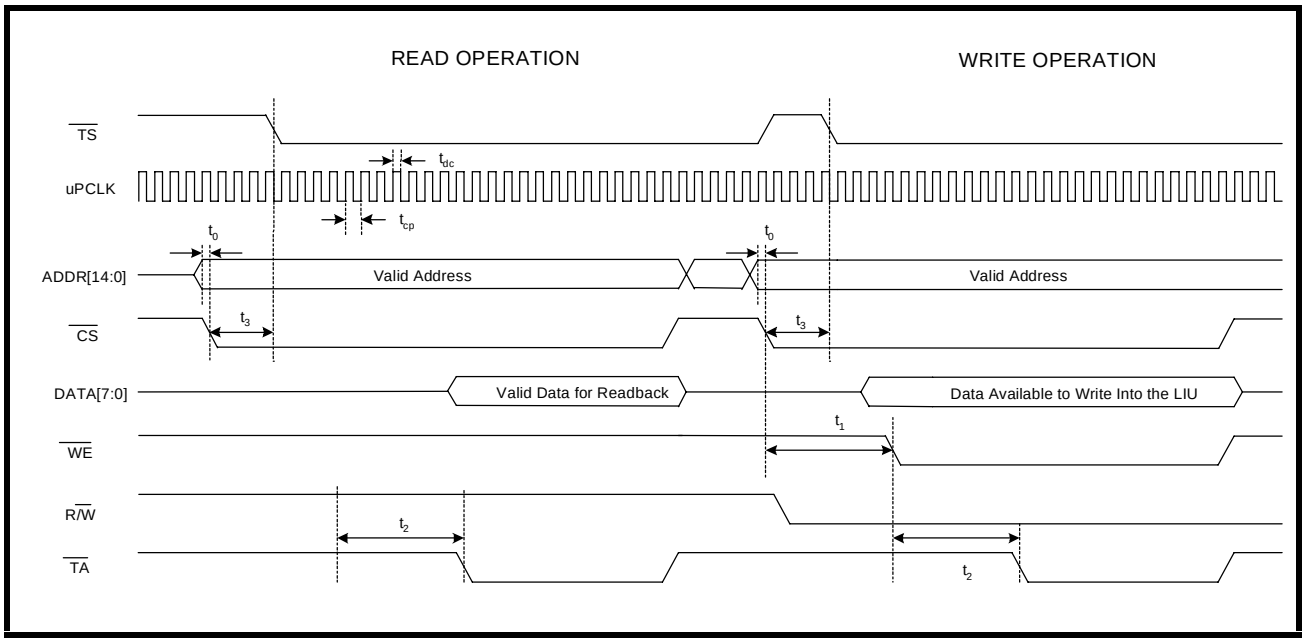


TABLE 16: POWER PC 403 MICROPROCESSOR INTERFACE TIMING SPECIFICATIONS

SYMBOL	PARAMETER	MIN	MAX	UNITS
t_0	Valid Address to $\overline{CS}$ Falling Edge	0	-	ns
t_1	$\overline{CS}$ Falling Edge to $\overline{WE}$ Assert	0	-	ns
t_2	$\overline{WE}$ Assert to $\overline{TA}$ Assert	-	320	ns
NA	$\overline{WE}$ Pulse Width (t_2)	320	-	ns
t_3	$\overline{CS}$ Falling Edge to $\overline{TS}$ Falling Edge	0	-	
t_{dc}	µPCLK Duty Cycle	40	60	%
t_{cp}	µPCLK Clock Period	20	-	ns

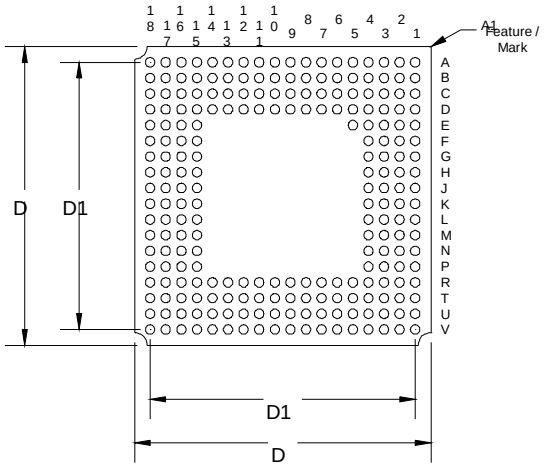
ORDERING INFORMATION

PRODUCT NUMBER	PACKAGE	OPERATING TEMPERATURE RANGE
XRT86VL34IB	225 LEAD PBGA	-40^0C to $+85^0$C

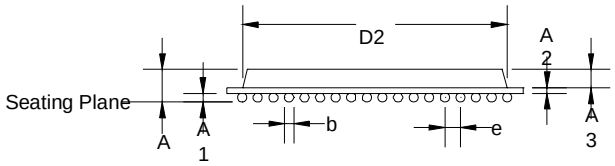
PACKAGE DIMENSIONS

225 Ball Plastic Ball Grid Array (19.0 mm x 19.0 mm, 1.0mm pitch PBGA)

Rev. 1.00



(A1 corner feature is mfger option)



Note: The control dimension is in millimeter.

	INCHES		MILLIMETERS	
SYMBOL	MIN	MAX	MIN	MAX
A	0.049	0.096	1.24	2.45
A1	0.016	0.024	0.40	0.60
A2	0.013	0.024	0.32	0.60
A3	0.020	0.048	0.52	1.22
D	0.740	0.756	18.80	19.20
D1	0.669 BSC		17.00 BSC	
D2	0.665	0.669	16.90	17.00
b	0.020	0.028	0.50	0.70
e	0.039 BSC		1.00 BSC	

REVISION HISTORY

REVISION #	DATE	DESCRIPTION
V1.2.0	January 29, 2007	Initial Release to Production version.

NOTICE