



## 12-STAGE BINARY COUNTER

The HEF4040B is a 12-stage binary ripple counter with a clock input ( $\overline{CP}$ ), an overriding asynchronous master reset input (MR) and twelve fully buffered outputs ( $O_0$  to  $O_{11}$ ). The counter advances on the HIGH to LOW transition of  $\overline{CP}$ . A HIGH on MR clears all counter stages and forces all outputs LOW, independent of  $\overline{CP}$ . Each counter stage is a static toggle flip-flop. Schmitt-trigger action in the clock input makes the circuit highly tolerant to slower clock rise and fall times.

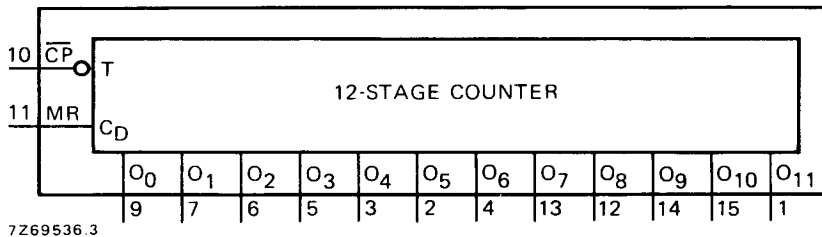


Fig. 1 Functional diagram.

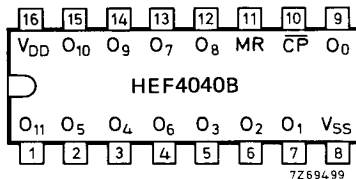


Fig. 2 Pinning diagram.

HEF4040BP : 16-lead DIL; plastic (SOT-38Z);  
HEF4040BD : 16-lead DIL; ceramic (cerdip) (SOT-74).  
HEF4040BT : 16-lead mini-pack; plastic  
(SO-16; SOT-109A).

### PINNING

$\overline{CP}$  clock input (HIGH to LOW edge-triggered)  
MR master reset input (active HIGH)  
 $O_0$  to  $O_{11}$  parallel outputs

### APPLICATION INFORMATION

Some examples of applications for the HEF4040B are:

- Frequency dividing circuits
- Time delay circuits
- Control counters

### FAMILY DATA

$I_{DD}$  LIMITS category MSI

} see Family Specifications

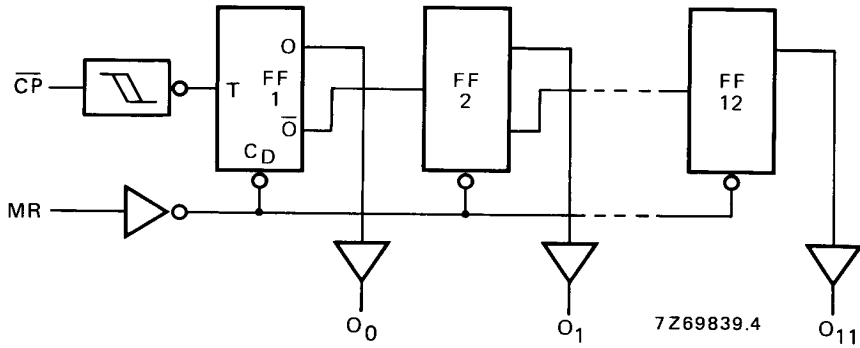


Fig. 3 Logic diagram.

**A.C. CHARACTERISTICS**

$V_{SS} = 0\text{ V}$ ;  $T_{amb} = 25\text{ }^{\circ}\text{C}$ ;  $C_L = 50\text{ pF}$ ; input transition times  $\leq 20\text{ ns}$

	$V_{DD}$ V	symbol	min.	typ.	max.	typical extrapolation formula	
Propagation delays $\overline{CP} \rightarrow O_0$ HIGH to LOW	5	$t_{PHL}$		105	210	ns	$78\text{ ns} + (0,55\text{ ns/pF}) C_L$
	10		45	90	ns	$34\text{ ns} + (0,23\text{ ns/pF}) C_L$	
	15		35	70	ns	$27\text{ ns} + (0,16\text{ ns/pF}) C_L$	
LOW to HIGH	5	$t_{PLH}$		85	170	ns	$58\text{ ns} + (0,55\text{ ns/pF}) C_L$
	10		40	80	ns	$29\text{ ns} + (0,23\text{ ns/pF}) C_L$	
	15		30	60	ns	$22\text{ ns} + (0,16\text{ ns/pF}) C_L$	
$O_n \rightarrow O_{n+1}$ HIGH to LOW	5	$t_{PHL}$		35	70	ns	note $(0,55\text{ ns/pF}) C_L$
	10		15	30	ns	note $(0,23\text{ ns/pF}) C_L$	
	15		10	20	ns	note $(0,16\text{ ns/pF}) C_L$	
LOW to HIGH	5	$t_{PLH}$		35	70	ns	note $(0,55\text{ ns/pF}) C_L$
	10		15	30	ns	note $(0,23\text{ ns/pF}) C_L$	
	15		10	20	ns	note $(0,16\text{ ns/pF}) C_L$	
$\overline{MR} \rightarrow O_n$ HIGH to LOW	5	$t_{PHL}$		90	180	ns	$63\text{ ns} + (0,55\text{ ns/pF}) C_L$
	10		40	80	ns	$29\text{ ns} + (0,23\text{ ns/pF}) C_L$	
	15		30	60	ns	$22\text{ ns} + (0,16\text{ ns/pF}) C_L$	
Output transition times HIGH to LOW	5	$t_{THL}$		60	120	ns	$10\text{ ns} + (1,0\text{ ns/pF}) C_L$
	10		30	60	ns	$9\text{ ns} + (0,42\text{ ns/pF}) C_L$	
	15		20	40	ns	$6\text{ ns} + (0,28\text{ ns/pF}) C_L$	
LOW to HIGH	5	$t_{TLH}$		60	120	ns	$10\text{ ns} + (1,0\text{ ns/pF}) C_L$
	10		30	60	ns	$9\text{ ns} + (0,42\text{ ns/pF}) C_L$	
	15		20	40	ns	$6\text{ ns} + (0,28\text{ ns/pF}) C_L$	

**Note**

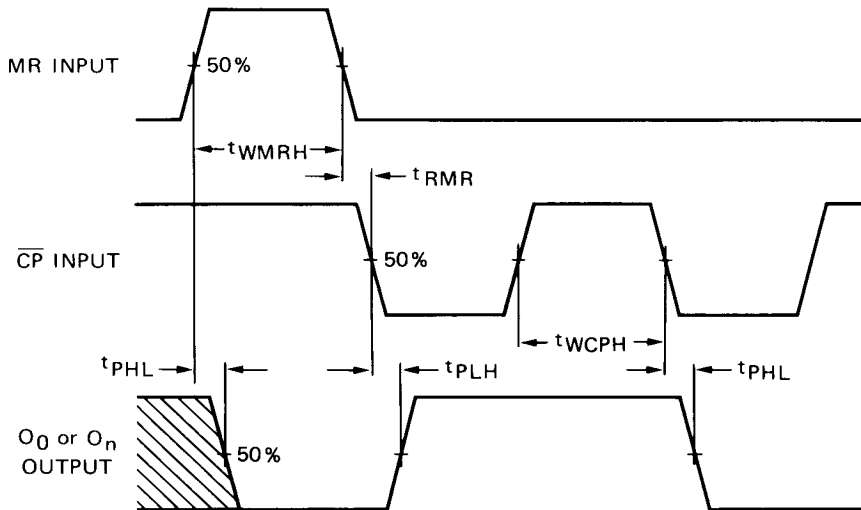
For other loads than 50 pF at the  $n^{\text{th}}$  output, use the slope given.

A.C. CHARACTERISTICS

$V_{SS} = 0\text{ V}$ ;  $T_{amb} = 25\text{ }^\circ\text{C}$ ;  $C_L = 50\text{ pF}$ ; input transition times  $\leq 20\text{ ns}$

	$V_{DD}$ V	symbol	min.	typ.	max.	
Minimum clock pulse width; HIGH	5	$t_{WCPH}$	50	25	ns	see also waveforms Fig. 4
	10		30	15	ns	
	15		20	10	ns	
Minimum MR pulse width; HIGH	5	$t_{WMRH}$	40	20	ns	
	10		30	15	ns	
	15		20	10	ns	
Recovery time for MR	5	$t_{RMR}$	40	20	ns	
	10		30	15	ns	
	15		20	10	ns	
Maximum clock pulse frequency	5	$f_{max}$	10	20	MHz	
	10		15	30	MHz	
	15		25	50	MHz	

	$V_{DD}$ V	typical formula for P ( $\mu\text{W}$ )	where	
Dynamic power dissipation per package (P)	5	$400 f_i + \sum(f_o C_L) \times V_{DD}^2$	$f_i$ = input freq. (MHz)	
	10		$2\,000 f_i + \sum(f_o C_L) \times V_{DD}^2$	$f_o$ = output freq. (MHz)
	15		$5\,200 f_i + \sum(f_o C_L) \times V_{DD}^2$	$C_L$ = load cap. (pF)
			$\sum(f_o C_L)$ = sum of outputs	
			$V_{DD}$ = supply voltage (V)	



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Fig. 4 Waveforms showing propagation delays for MR to O<sub>n</sub> and CP to O<sub>0</sub>, minimum MR and CP pulse widths.