AT&T

Advance

DATA SHEET

LC1092CP/DP AC PLASMA DISPLAY ROW DRIVERS

DESCRIPTION

The LC1092CP and LC1092DP are high-voltage CMOS (HV-CMOS) integrated circuits that are assembled in 44-pin plastic J-leaded chip carriers. The LC1092DP pinout alignment is the mirror image of the LC1092CP pinout alignment (see Figures 2 and 3 for details).

The chips contain a 32-bit shift register which can accept serial data at clock rates up to 10 MHz. The outputs of these drivers are normally logic high and can be switched either selectively or together. Any output whose associated register bit (in the internal 32-bit serial register) contains a high, will switch low when the STROBE input is switched low (if the SUSTAIN input is high). When the SUSTAIN input is switched low, all outputs switch low, independent of the DATA or STROBE inputs. This feature is used to generate a portion of the sustain pulse required in the operation of AC Plasma Displays. Serial data output from the shift register may be used to cascade shift registers. This output, and the contents of the shift registers, are set low when the CLEAR input is held low.

FEATURES

- 32-BIT SHIFT REGISTER WITH CLEAR
- 100-VOLT PUSH-PULL CMOS OUTPUTS
- 10 MHz DATA CLOCK RATE
- EACH DEVICE DRIVES 32 LINES

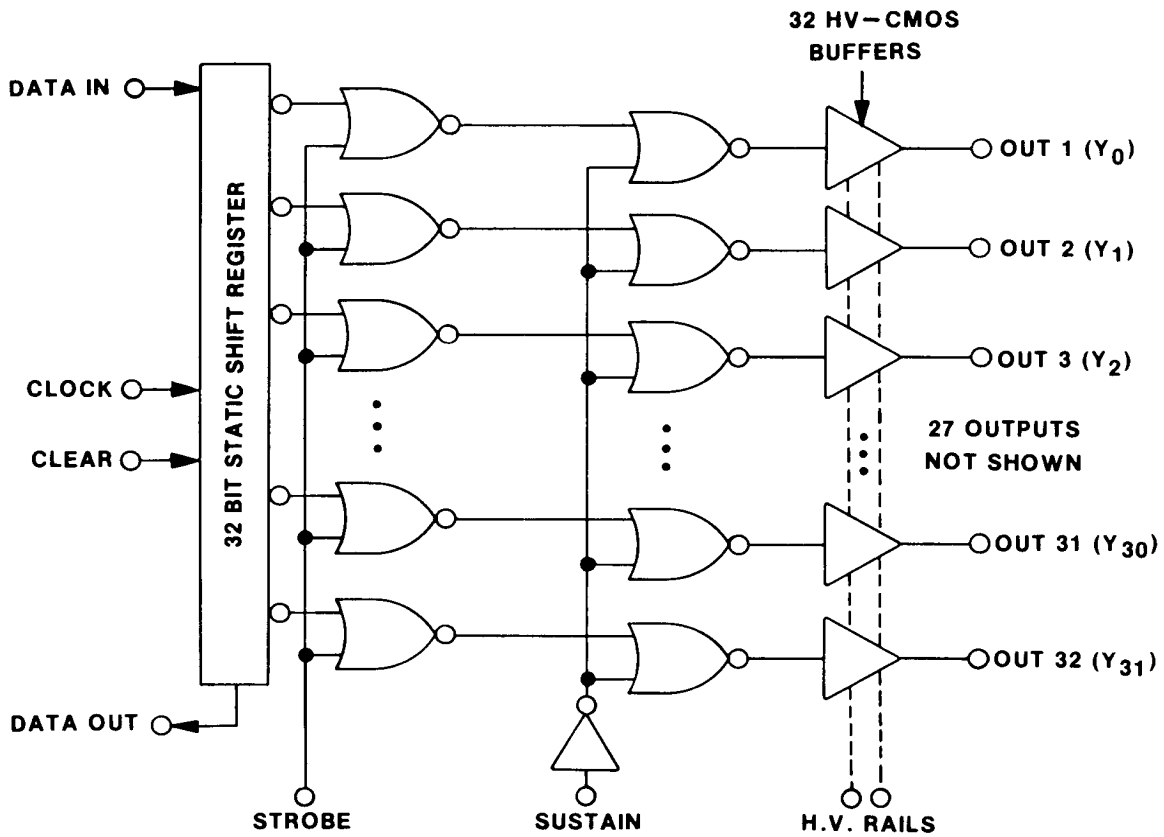


Fig. 1—Functional Diagram

OCTOBER 1986

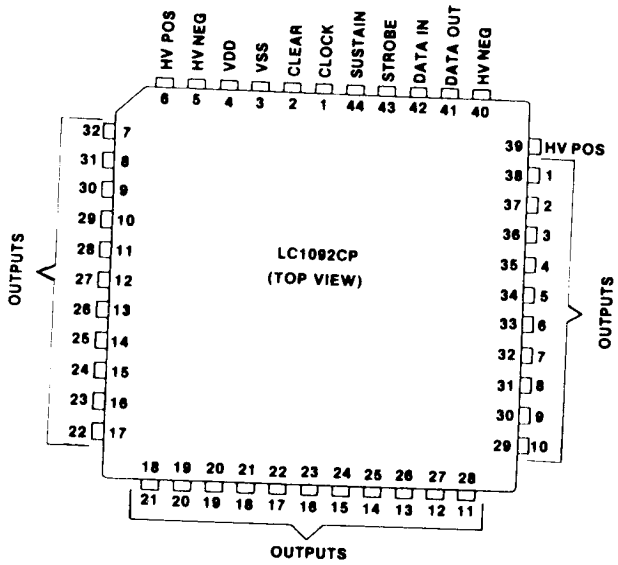


Fig. 2—LC1092CP Package Pinout

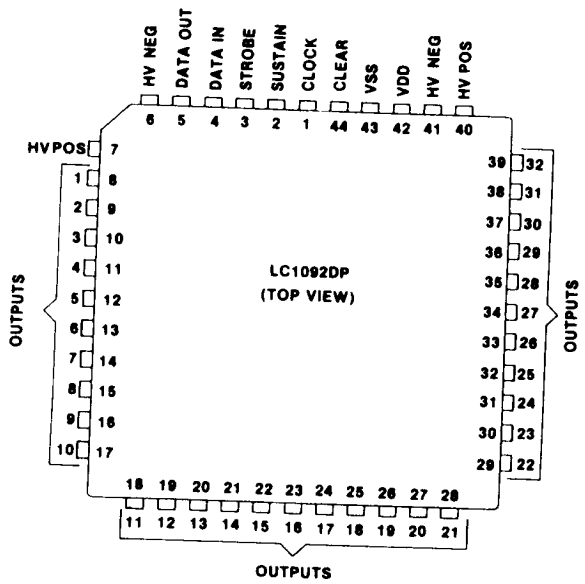


Fig. 3—LC1092DP Package Pinout

MAXIMUM RATINGS (At 25°C unless otherwise specified)	
Ambient Operating Temperature Range	0 to +60°C
Storage Temperature Range	−65 to +150°C
Lead Soldering Temperature (t = 10 sec. max.)	260°C
Supply Voltage (HV_{POS})①	+100 V
Supply Voltage (HV_{NEG})①	−95 V
Logic Supply Voltage (VDD)	+5.5 V
INPUT Voltage	VDD plus 0.5 V
Current (Each Driver Output)	40 mA
Power Dissipation	550 mW

Stresses in excess of those listed under "Maximum Ratings" may cause permanent damage to the device. This is an absolute stress rating only. Functional operation of the device at these or any other conditions in excess of those indicated in the operational sections of this Data Sheet is not implied. Exposure to maximum rating conditions for extended periods of time may affect device reliability.

①The difference between HV_{POS} and HV_{NEG} must never exceed 100 volts. HV_{POS} must always be positive with respect to HV_{NEG}.

PIN DESCRIPTION AND TIMING REQUIREMENTS

SYMBOL	NAME/FUNCTION
CLOCK	Input for clocking functions. The leading edge of CLOCK must come ≥33 nsec after valid DATA. Clock must remain high for ≥30 nsec.
DATA IN	Input for data stream. DATA must be valid for 12 nsec after CLOCK goes high.
DATA OUT	Serial data output from the Shift Register may be used to cascade shift registers.
STROBE	STROBE can go low ≥20 nsec after CLOCK goes high.
SUSTAIN	SUSTAIN can go low ≥10 nsec after STROBE goes low.
CLEAR	The Shift Register is set to zero ≥8 nsec after CLEAR goes low.
VDD	Logic supply voltage. Normal operating voltage is +5.0 V (±0.25 V).
VSS	Logic common (not necessarily system or physical ground).
HV_{POS}	External power supply. HV_{POS} must always be positive with respect to HV_{NEG}. The difference between HV_{POS} and HV_{NEG} must never exceed 100 V. External connections may be made to the most convenient HV_{POS} pin, since these pins are connected on-chip.
HV_{NEG}	External power supply. HV_{NEG} must always be negative with respect to HV_{POS}. The difference between HV_{POS} and HV_{NEG} must never exceed 100 V. External connections must be made to both HV_{NEG} pins, since these pins are **not** connected on-chip.
OUT *XX*	High-voltage CMOS outputs numbered 1 through 32.

SIMPLIFIED INPUT AND OUTPUT DIAGRAMS

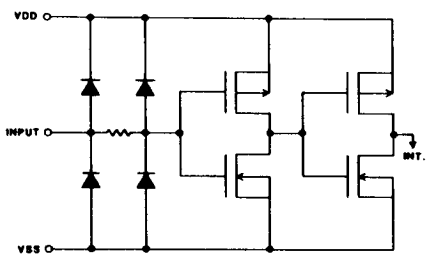


Fig. 4—Typical Input

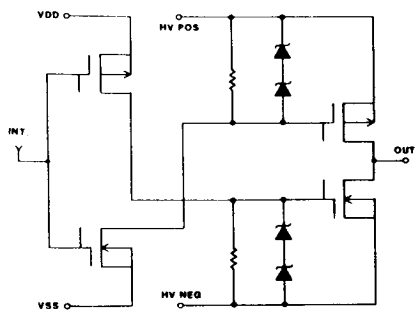


Fig. 5—Typical of All Outputs

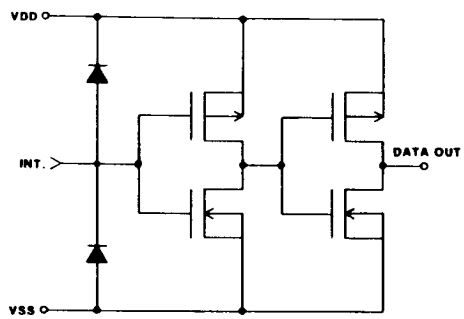
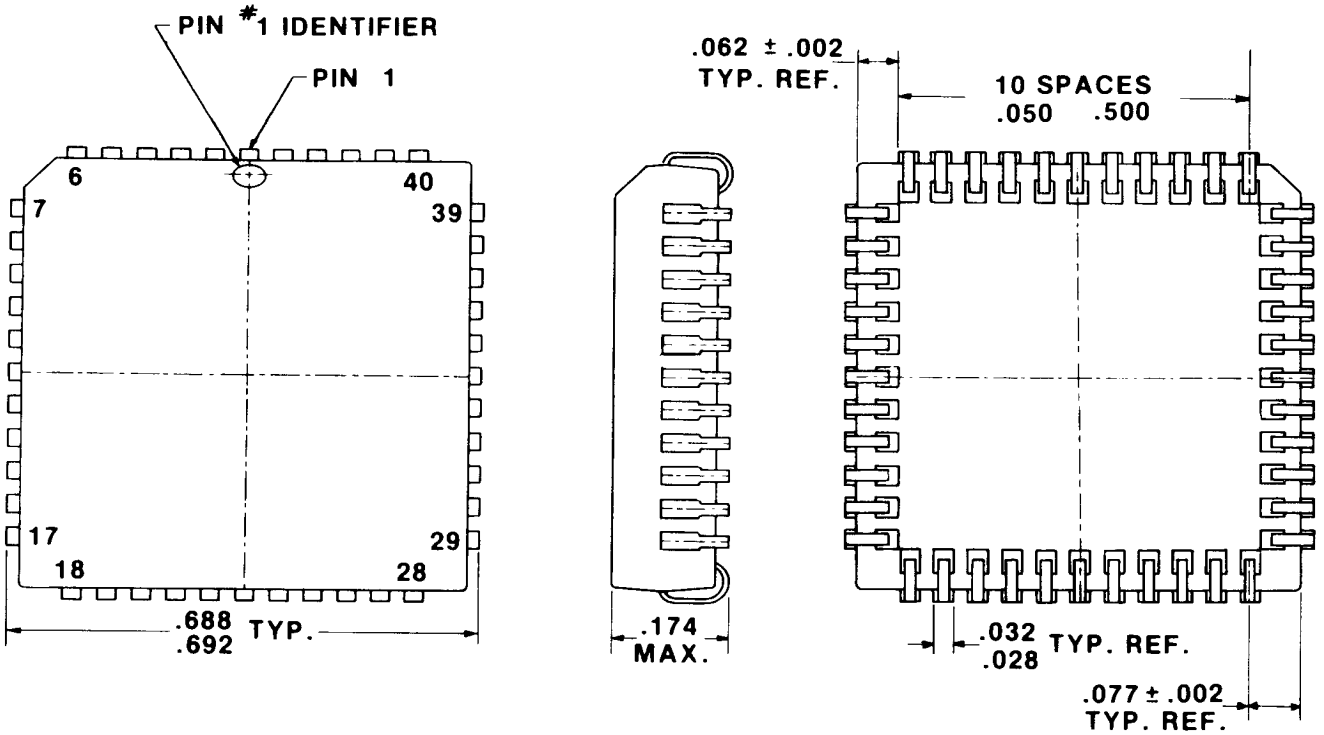


Fig. 6—Typical Data Output

OUTLINE DRAWINGS (Dimensions in Inches)



NOTE: The recommended chip carrier socket is Yamaichi #IC 51-0444-400 or equivalent.

ORDERING INFORMATION:

DEVICE	COMCODE
LC1092CP	104401534
LC1092DP	104401559

For additional information contact your AT&T Account Manager, or call:

☐ AT&T Technologies, 555 Union Boulevard, Dept. 50AL203140, Allentown, PA 18103
1-800-372-2447

TYPICAL AND RECOMMENDED OPERATING CHARACTERISTICS

(At 25°C unless otherwise specified)

CHARACTERISTICS	MIN.	TYP.	MAX.	UNIT
Supply Voltage (HV_{POS}); Pulsed Voltage	VDD	—	+100	V
Frequency	—	—	16	kHz
Logic Supply Voltage (VDD)	4.75	5.00	5.25	V
Supply Voltage (HV_{NEG}); Pulsed Voltage	−95	Gnd	Gnd	V
Frequency	—	—	16	kHz
Logic Common Voltage (VSS)	Gnd	Gnd	Gnd	V
High-Level Input Voltage	VDD-0.5	5.0	VDD+0.5	V
Low-Level Input Voltage	VSS	VSS	VSS+0.5	V
CLOCK Frequency	—	—	10	MHz
CLOCK Width Duration (Low or High Logic)	30	—	—	nsec
Setup Time (See Figure 7)				
Data Inputs Before CLOCK Transition High	20	—	—	nsec
Data Inputs After CLOCK Transition High	60	—	—	nsec
Data Low After CLEAR Goes Low	10	—	—	nsec
SUSTAIN Low Before HV_{NEG} Sustain Pulse Goes Low	1.0	—	—	μsec
SUSTAIN High After HV_{NEG} Sustain Pulse Goes High	1.0	—	—	μsec
STROBE Low After HV_{NEG} Write Pulse Low	1.0	—	—	μsec
STROBE High Before HV_{NEG} Write Pulse High	1.0	—	—	μsec
HV_{NEG} Sustain Pulse High Before HV_{NEG} Write Pulse Goes Low	1.5	—	—	μsec
Rise Time (HV_{POS}) 10% to 90%; 0 V to +100 V	0.3	—	—	μsec
Fall Time (HV_{POS}) 10% to 90%; +100 V to 0 V	0.5	—	—	μsec
Rise Time (HV_{NEG}) 10% to 90%; 0 V to −95 V	0.3	—	—	μsec
Fall Time (HV_{NEG}) 10% to 90%; −95 V to 0 V	0.5	—	—	μsec

FUNCTIONAL TABLE

Table 1.

FUNCTION	INPUTS					OUTPUTS						
						SHIFT REGISTER			SERIAL			
	DATA	CLOCK	CLEAR	STROBE	SUSTAIN	R1	R2	R3 . . . . . R32	DATA	Y0	Y1	Y2 . . Y31
DATA IN	H	↑	H	H	H	H	$R1_n$	$R2_n$ . . . $R31_n$	$R32_n$	H	H	H . . . . . H
	L	↑	H	H	H	L	$R1_n$	$R2_n$ . . . $R31_n$	$R32_n$	H	H	H . . . . . H
STROBE	X	L	H	H	H	$R1_n$	$R2_n$	$R3_n$ . . . $R32_n$	$R32_n$	H	H	H . . . . . H
	X	L	H	L	H	$R1_n$	$R2_n$	$R3_n$ . . . $R32_n$	$R32_n$	$\overline{R1}$	$\overline{R2}$	$\overline{R3}$ . . $\overline{R32}$
SUSTAIN	X	L	X	X	L	$R1_n$	$R2_n$	$R3_n$ . . . $R32_n$	$R32_n$	L	L	L L
CLEAR DATA	X	X	L	H	H	L	L	L L	L	H	H	H . . . . . H

H = high level. L = low level. X = irrelevant. ↑ = low-to-high-level transition.
R1 . . . R32 = levels currently at internal outputs of shift registers one through thirty-two, respectively.
$R1_n$ . . . $R32_n$ = levels at shift-register outputs R1 through R32 respectively, before the most recent ↑ transition at the Clock input.

TYPICAL OPERATING SEQUENCE

A typical operation sequence (Figure 7) is to clock data into the serial shift register at a clock rate of ⩽10 mHz. This data is then transferred to the HV output buffers by means of the STROBE which operates at a rate of ⩽16 kHz. A DATA high in the Shift Register will yield a low (HV_{NEG} level) on the corresponding output during the time that STROBE is low. All outputs will be low (HV_{NEG} level) while the SUSTAIN input is low, independent of the data in the Shift Register.

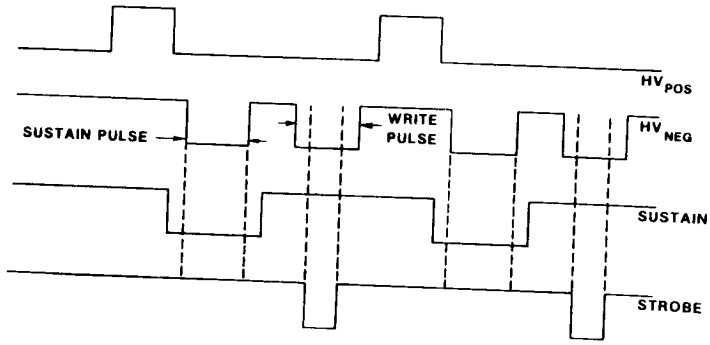


Fig. 7—Typical Operating Sequence Diagram

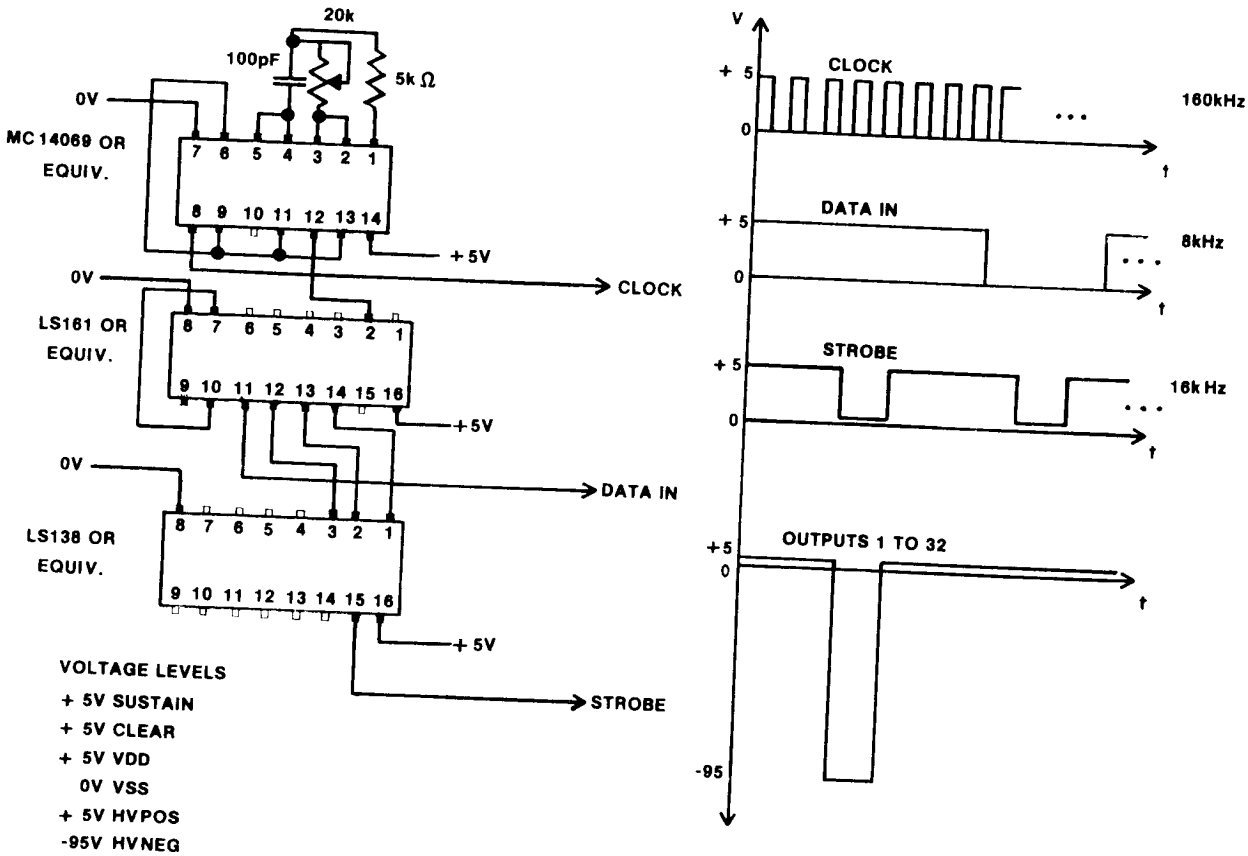


Fig. 8—LC1092C/D Typical Evaluation Test Circuit