Transition-Mode PFC Controller with Fault Condition Protection

Datasheet. P03 (for Internal Use Only)

General Description

The LD7591 is a voltage mode PFC controller operating on transition mode, integrated several functions of protection, such as OVP, OCP, and Brown-in protection. It minimizes the components counts and is available in a SOP-8 or DIP-8 package. Those make it an ideal design for low cost applications.

It provides functions of low startup current, over voltage protection, open feedback protection, disable function, over current protection, under voltage lockout and integrated LEB of the current sensing. Also, the LD7591 features without mains voltage sensing compared with traditional current mode PFC for power saving. The LD7591 can be disabled if the INV pin voltage is lower than 0.45V and the operating current decreases to 65μA

.

Features

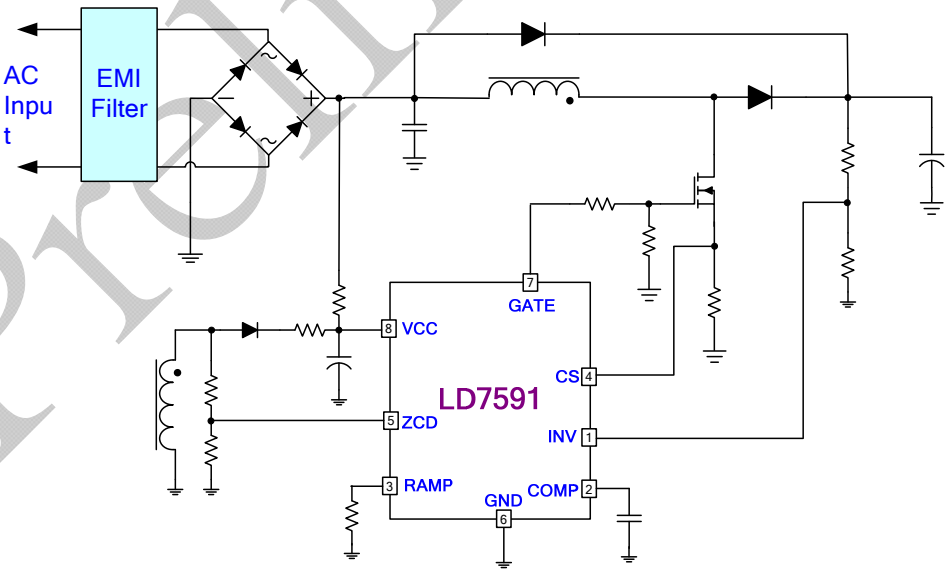
- Transition mode of PFC pre-regulator
- Voltage mode control
- Programmable max. on-time
- Low Startup Current (<30μA)
- UVLO (Under Voltage Lockout)
- LEB (Leading-Edge Blanking) on CS Pin
- Open-Feedback Protection and Disable Function
- OVP (Over Voltage Protection)
- OCP (Cycle by cycle current limiting)
- 800/-1200mA Driving Capability
- Internal OTP function

Applications

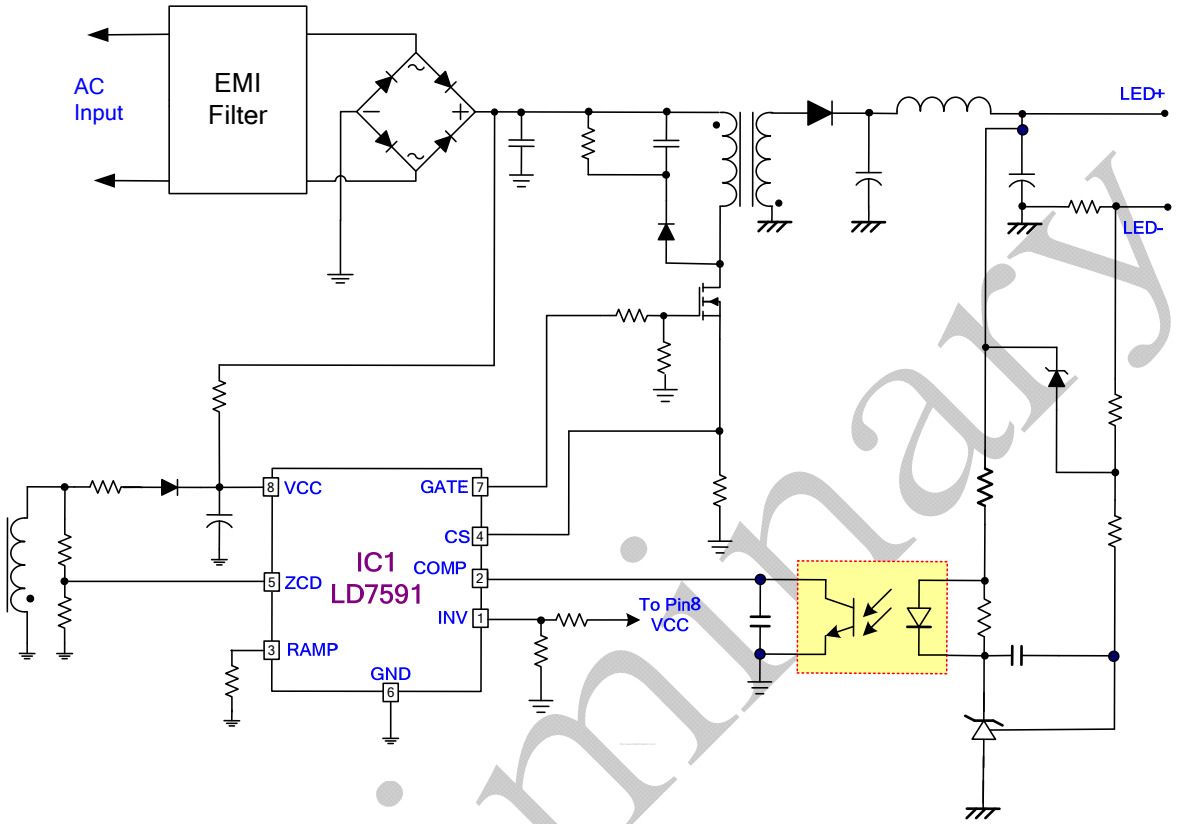
- Output above 65W adaptor.
- Open Frame Switching Power Supply
- LCD TV Power Supply
- LED Power Supply

Patent Pending

Typical Application for Boost PFC



Typical Application for LED (Flyback PFC)



Pin Configuration (Top view)

DIP-8 & SOP-8(TOP VIEW)

YY : Year code (D: 2004, E: 2005 ⋯)
WW : Week code
PP : Production code

Ordering Information

Part number	Package	Top Mark	Shipping
LD7591 GS	SOP-8 Green package	LD7591GS	3600/ Tube/ Carton
LD7591 GN	DIP-8 Green package	LD7591GN	3000/ Tube/ Carton

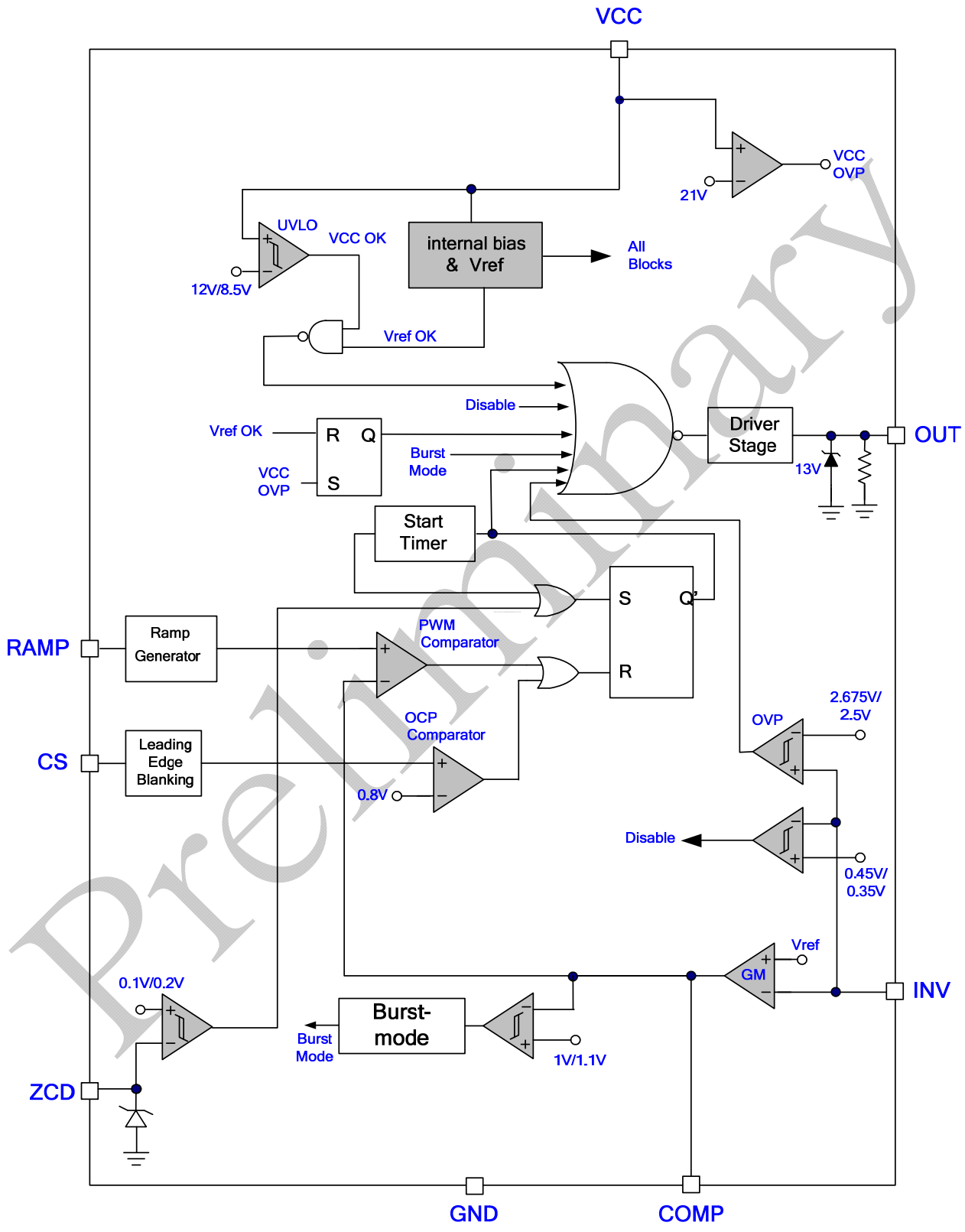
Pin Descriptions

NAME	Pin (SOP-8/DIP-8)	FUNCTION
INV	1	Output voltage feed back control
COMP	2	Output of the error amplifier for voltage loop compensation to achieve stable
RAMP	3	Ramp generator, connecting a resistor to GND pin to set the saw tooth signal
CS	4	Current sense pin, connect to sense the MOSFET current for OCP
ZCD	5	Detecting zero crossing of input signal
GND	6	Ground
OUT	7	Gate drive output to drive the external MOSFET
VCC	8	Power source VCC pin

Recommended Operating Conditions

Item	Min.	Max.	Unit
Vcc pin capacitor	22	47	μF
Comp pin capacitor	0.1	0.47	μF
RAMP pin resistor	4.7k	100k	Ω

Block Diagram



Absolute Maximum Ratings

Supply Voltage VCC	30V
OUT	-0.3 ~VCC
COMP, INV, CS, RAMP, ZCD	-0.3 ~7V
Maximum Junction Temperature	150°C
Operating Junction Temperature Range	-40°C to 125°C
Operating Ambient Temperature Range	-40°C to 85°C
Storage Temperature Range	-65°C to 150°C
Package Thermal Resistance (SO-8, θ_{JA})	155°C/W
Package Thermal Resistance (DIP-8, θ_{JA})	100°C/W
Power Dissipation (SOT-8, at Ambient Temperature = 85°C)	420mW
Power Dissipation (DIP-8, at Ambient Temperature = 85°C)	650mW
Lead temperature (Soldering, 10sec)	260°C
ESD Voltage Protection, Human Body Model	2.5 KV
ESD Voltage Protection, Machine Model	250 V
Gate Output Current	800mA/-1200mA

Caution:

Stresses beyond the ratings specified in “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Electrical Characteristics

(V_{CC}=14.0V, T_A = 25°C unless otherwise specified.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage (VCC Pin)					
Startup Current	VCC<UVLO ON		20	30	μA
Operating Current (with 1nF load on OUT pin)	V_{COMP}=0V		2.0		mA
	V_{COMP}=3V		2.5		mA
	Vcc OVP		0.45		mA
	Vinv=0V		65	95	μA
UVLO (off)		7.5	8.5	9.5	V
UVLO (on)		11.0	12.0	13.0	V
VCC OVP Level	(-20 °C ~125°C)	19.5	21	22.5	V
Error Amplifier (Comp Pin)					
Feedback Input Voltage, Vref		2.465	2.500	2.535	V
Input Bias Current	Vinv=1V~4V	-0.5		0.5	μA
Transconductance			115		μmho
Output Sink Current	V_{inv}= Vref +0.1V		12		μA
Output Source Current	V_{inv}= Vref -0.1V		-12		μA
Output Upper Clamp Voltage	Vinv= Vref -0.1V	5.35	6.0	6.65	V
Burst Mode COMP pin Threshold voltage			1		V
	Hysteresis		100		mV
INV pin					
OVP Trip Level		2.62	2.675	2.73	V
	OVP Hysteresis		0.175		V
Enable Threshold Voltage		0.4	0.45	0.5	V
	Enable Hysteresi		0.1		V
Current Sensing (CS Pin)					
Current Sense Input Threshold Voltage		0.74	0.8	0.86	V
Input bias current	Vcs=0V~1V	0		1.0	μA
LEB time			350		ns
Zero Current Detector (ZCD Pin)					
Upper Clamp Voltage	Idet=10uA	6.0	6.7	7.4	V
Lower Clamp Voltage	Idet=10uA	-0.3	-0.7	-1.0	V
Input Voltage Threshold		0.08	0.1	0.12	V
	Hysteresis		0.1		V
Input bias current	Vzcd=1V~5V, Out=OFF	0.0		1.0	μA
Maximum Delay from ZCD to Output			250		ns

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Maximum ON-Time, Ton-max (Ramp Pin)					
Maximum On Time Voltage	Rramp=40.5K	2.784	2.900V	3.016	V
Maximum On Time Programming	Rramp=40.5K	19	24	33	μS
Maximum On Time	Rramp ≧ 100K		40		μS
Minimum OFF-Time					
Minimum OFF-Time			1		μs
Minimum OFF-Time Programming			0.10		Ton-max
Gate Drive Output (OUT Pin)					
Output Low Level	V_{CC}=12V, Isink=20mA			0.5	V
Output High Level	V_{CC}=12V, Isource=20mA	9		12	V
Output High Clamp Level	V_{CC}=18V	11.5	13	14.5	V
Rising Time	Vcc=12V, CL=1000pF		75	150	ns
Falling Time	Vcc=12V, CL=1000pF		25	100	ns
Starter					
Start Timer Period		50	150	300	μs
OTP (Over Temp. Protection)					
OTP Trip level			140		°C
OTP Hysteresis			30		°C

Typical Performance Characteristics

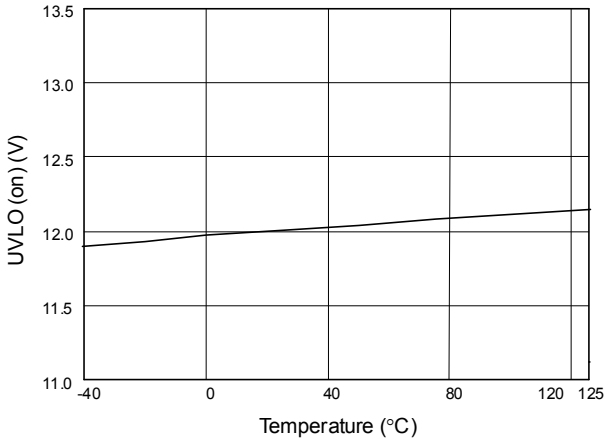


Fig. 1 UVLO (on) vs. Temperature

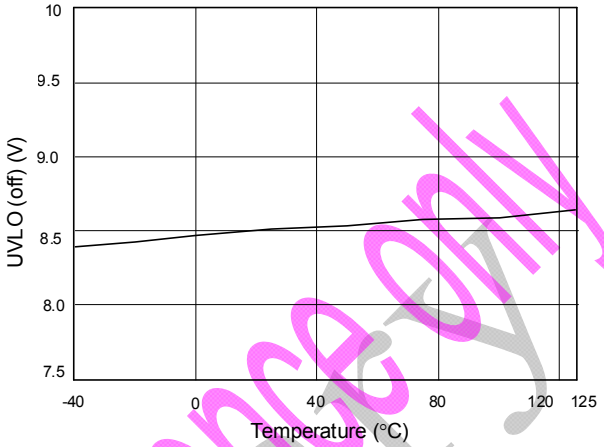


Fig. 2 UVLO (off) vs. Temperature

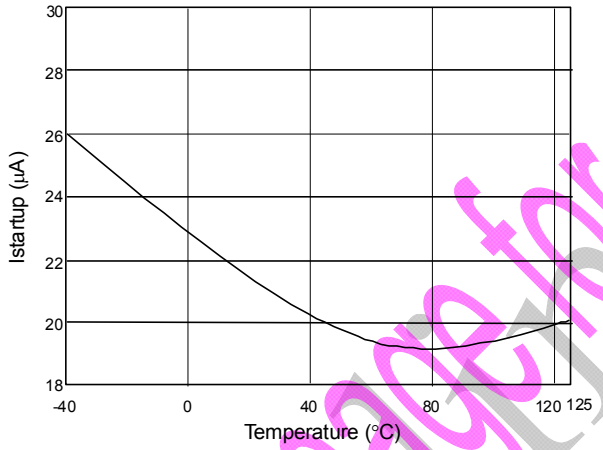


Fig. 3 Startup Current vs. Temperature

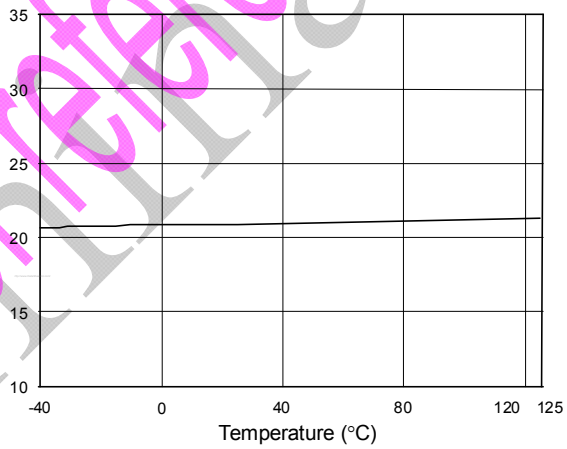


Fig. 4 VCC OVP vs. Temperature

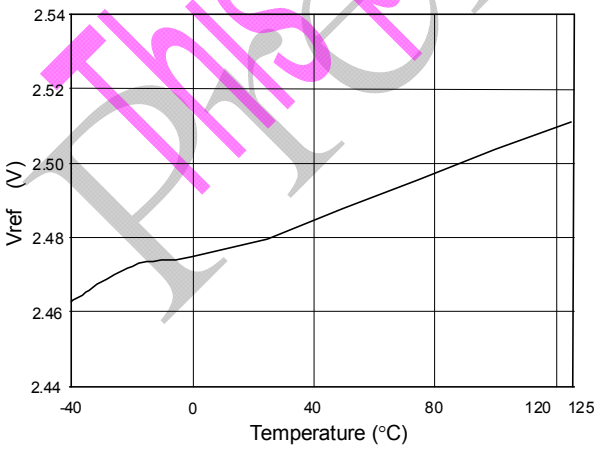


Fig. 5 Vref vs. Temperature

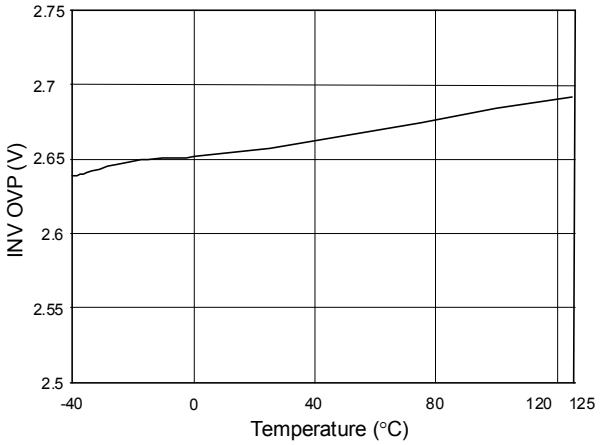


Fig. 6 INV OVP vs. Temperature

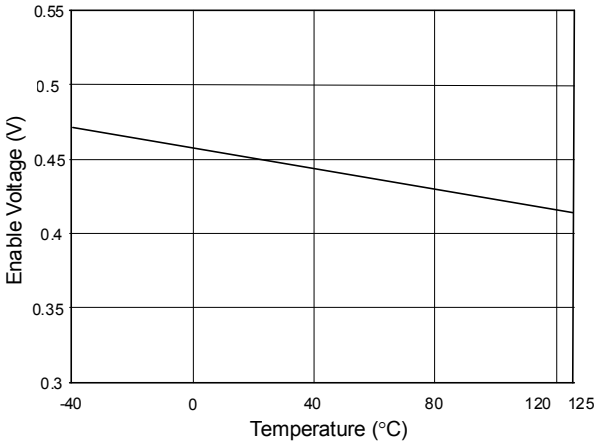


Fig. 7 Enable Voltage vs. Temperature

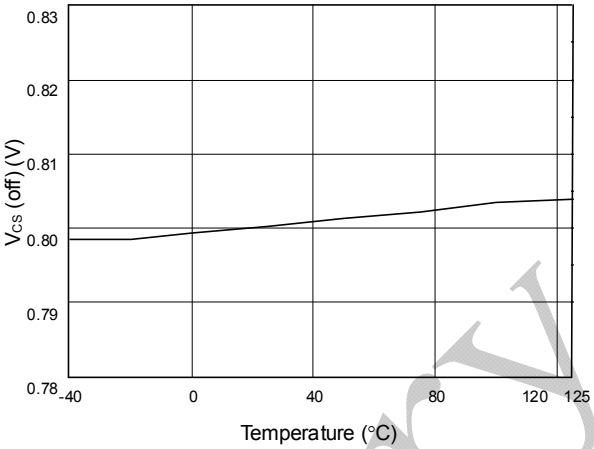


Fig. 8 V_{CS} (off) vs. Temperature

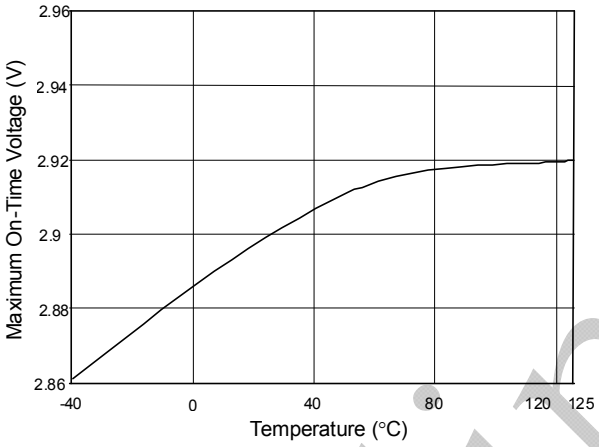


Fig. 9 Maximum On-Time Voltage vs. Temperature

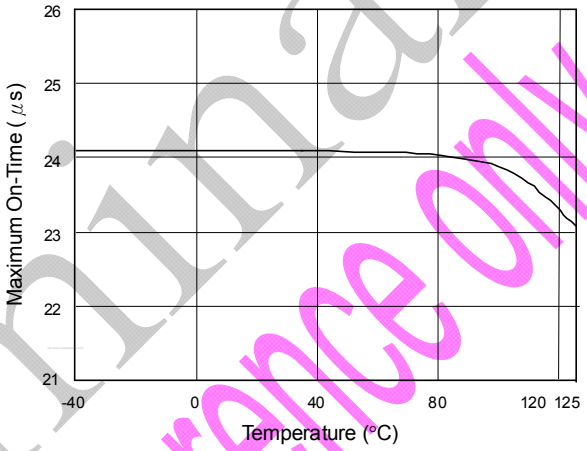


Fig. 10 Maximum On-Time vs. Temperature

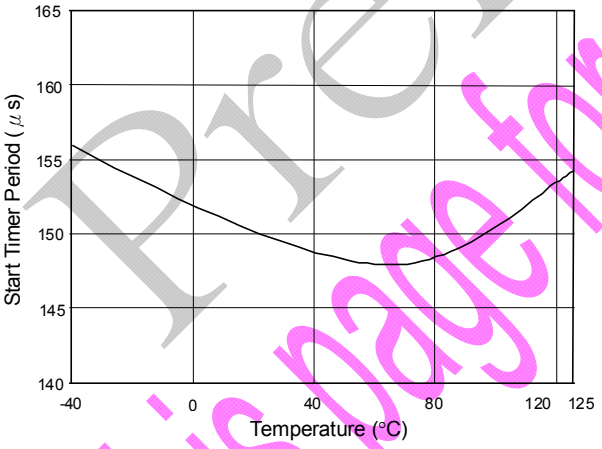


Fig. 11 Start Timer Period vs. Temperature

Application Information

Operation Overview

The LD7591 is an excellent voltage mode PFC controller. It meets the IEC61000-3-2 requirement and is intended for the use in those pre-regulator that demand low power harmonics distortion. It integrated more functions to reduce the external components counts and the size. Its major features are described as below.

Under Voltage Lockout (UVLO)

An UVLO comparator is implemented in it to detect the voltage on the VCC pin. It would assure the supply voltage enough to turn on the LD7591 PFC controllers and further to drive the power MOSFET. As shown in Fig. 12, a hysteresis is built in to prevent the shutdown from the voltage dip during start up. The turn-on and turn-off threshold level are set at 12.0V and 8.5V, respectively.

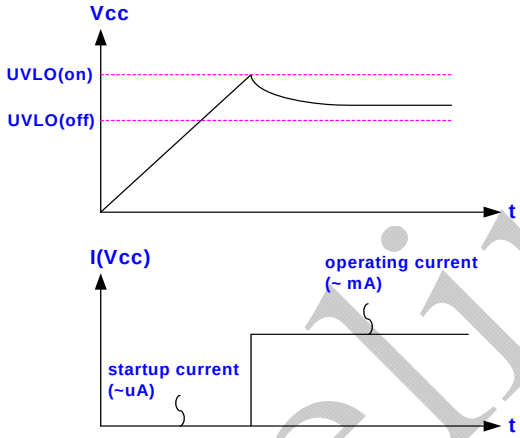


Fig. 12

Startup Current and Startup Circuit

The typical startup circuit to generate the LD7591 Vcc is shown in Fig. 13. During the startup transient, the Vcc is lower than the UVLO threshold thus there is no gate pulse produced from LD7591 to drive power MOSFET. Therefore, the current through R1 will provide the startup current and to charge the capacitor C1. Whenever the Vcc voltage is high enough to turn on the LD7591 and further to deliver the gate drive signal, the supply current is provided from the auxiliary winding of the PFC choke. Lower startup current requirement on the PFC controller will help to increase the value of R1 and then reduce the power consumption on R1. By using CMOS process and the special circuit design, the maximum startup current of LD7591 is only 30μA. If a higher resistance value of R1 is chosen, it usually takes more time to start up. To carefully select the value of R1 and C1 will optimize the power consumption and startup time.

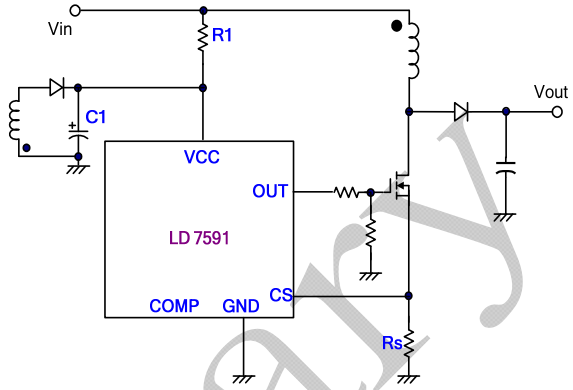


Fig. 13

Output Voltage Setting

The LD7591 monitors the output voltage signal at INV pin through a resistor divider pair Ra and Rb. A transconductance amplifier is used instead of the conventional voltage amplifier. The transconductance amplifier (voltage controlled current source) aids the implementation of OVP and disable function. The output current of the amplifier changes according to the voltage difference of the inverting and non-inverting input of the amplifier. The output voltage of the amplifier is compared with the internal ramp signal to generate the turn-off signal. The output voltage is determined by the following relationship.

$$V_{OUT} = 2.5V(1+\frac{Ra}{Rb})$$

Where Ra and Rb are top and bottom feedback resistor values (as shown in the figure 14).

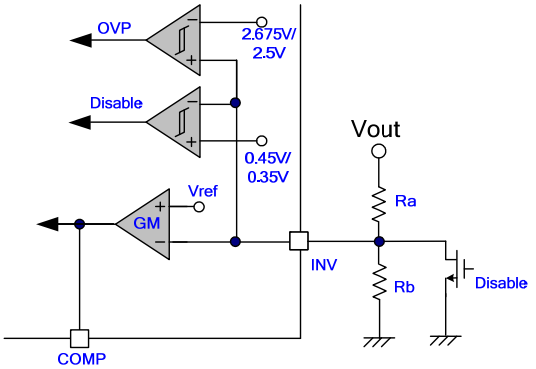


Fig. 14

OVP and Disable on INV pin

To prevent the over voltage on the output capacitor from the fault condition, LD7591 is implemented with an OVP function on INV pin. Whenever the INV voltage is higher than the OVP threshold voltage 2.675V, the output gate drive circuit will be shutdown simultaneously thus to stop the switching of the power MOSFET until the INV pin down to 2.5V. The OVP function in LD7591 is an auto-recovery type protection. The figure 15 shows its operation. On the other hand, if the OVP condition is removed, the Vcc level will get back to normal level and the output will automatically return to the normal operation.

The disable comparator disables the operation of the LD7591 when the voltage of the inverting input is lower than 0.35V and there is 100mV hysteresis. An external small signal MOSFET can be used to disable the IC, referring to figure 14. The IC operating current decreases below 65μA to reduce power consumption if the IC is disabled.

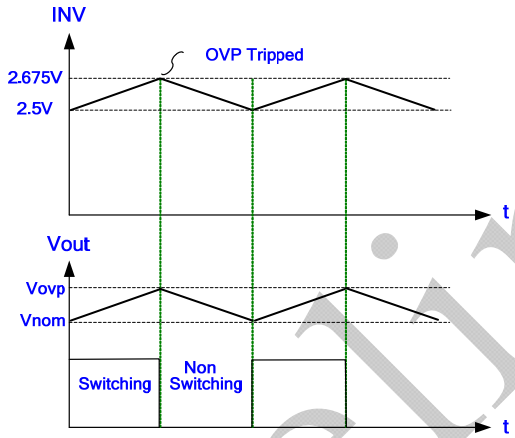


Fig. 15

Zero Current Detection (ZCD)

Figure 16 shows typical ZCD-block. The Zero Current Detection block switches on the external MOSFET as the current through the boost inductor has gone to zero using an auxiliary winding coupled with the inductor. This feature allows transition-mode operation. If the voltage of the ZCD pin goes higher than 0.2V, the ZCD comparator waits until the voltage goes below 0.1V. If the voltage goes below 0.1V, the zero current detector turns on the MOSFET. The ZCD pin is protected internally by two clamps, 6.7V-high clamp and -0.7V-low clamp. The 150us timer generates a MOSFET turn on signal if the driver output has been low for more than 150us from the falling edge of the driver output.

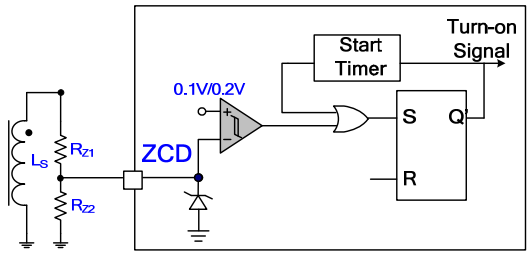


Fig. 16

Figure 17 shows typical ZCD-related waveforms. Because the ZCD pin has some capacitance, there can be some delay caused by Rz1 and the turn-on time can be delayed. Ideally, the switch must be turned on when the inductor current reaches zero; but because of the structure of the ZCD delay, it is turned on after some delay time. During this delay time, the stored charge of the COSS (MOSFET output capacitor) is discharged through the path indicated in figure18. This charge is transferred into a small filter capacitor, Cin1, which is connected to the bridge diode. Therefore, there is no current flow from the input side, meaning the input current I_{in} is zero during this period. In order to reduce the negative current flowing the internal diode, the resistance of R_{Z1} is suggested larger than 47kΩ.

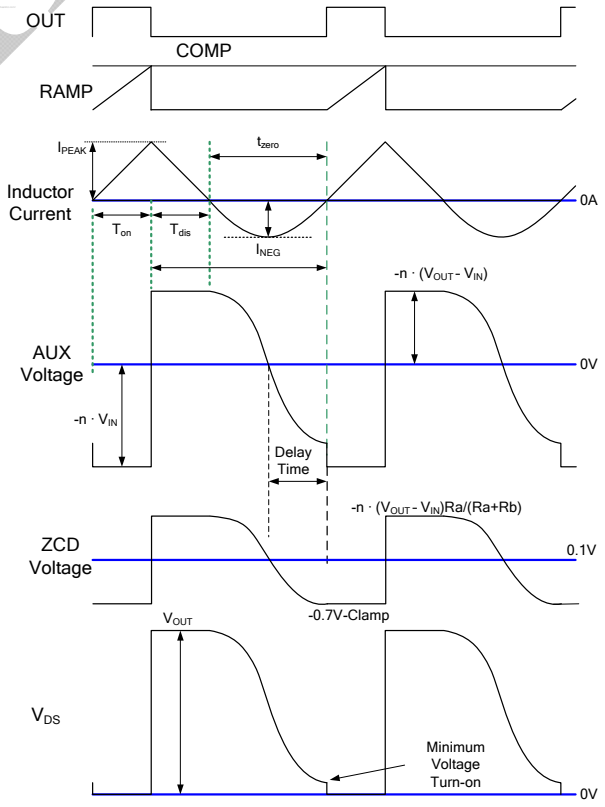


Fig. 17

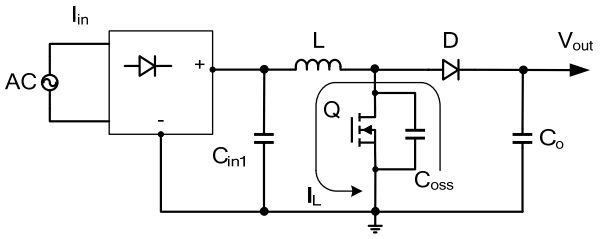


Fig. 18

Ramp Generator Block

The output of the gm error amplifier and the output of the ramp generator block are compared to determine the MOSFET on time, as shown in figure 19. The slope of the ramp is determined by an external resistor connected to the RAMP pin. The voltage of the RAMP pin is 2.9V and the slope is proportional to the current flowing out of the RAMP pin. The internal ramp signal has a 1V offset; therefore, the drive output is shut down if the voltage of the COMP pin is lower than 1V. The programmed on-time is maximum when the COMP pin is open. The COMP pin open voltage is about 5.4~6.6V. According to the slope of the internal ramp, the maximum on-time can be programmed. The necessary maximum on-time depends on the boost inductor, lowest AC line voltage, and maximum output power. The resistor value should be designed properly. The maximum on-time can be obtained from below

$$T_{ON-Time(MAX)} = \frac{R_{ramp}}{1.58 \cdot 10^{9}}$$

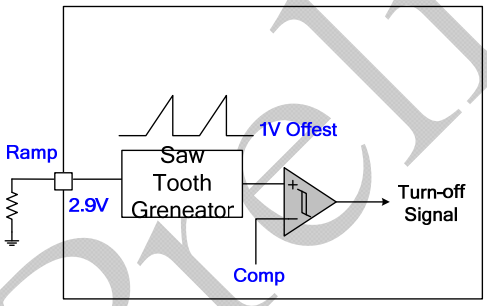


Fig. 19

Output Drive Stage

An output stage of a CMOS buffer, with typical 800mA/-1200mA driving capability, is incorporated to drive a power MOSFET directly. The output voltage is clamped at 13V to protect the MOSFET gate even when the VCC voltage is higher than 13V.

Current Sensing and Leading-edge Blanking

The typical voltage mode of PFC controller feedbacks the voltage signal to close the control loop and achieve regulation. The LD7591 detects the primary MOSFET current from the CS pin, which is for the pulse-by-pulse current limit. The maximum voltage threshold of the current sensing pin is set at 0.8V. From above, the MOSFET peak current can be obtained from below.

$$I_{PEAK(MAX)} = \frac{0.8V}{R_S}$$

A 350nS leading-edge blanking (LEB) time is included in the input of CS pin to prevent the false-trigger from the current spike. In the low power application, if the total pulse width of the turn-on spikes is less than 350nS and the negative spike on the CS pin doesn't exceed -0.3V, it could eliminated the R-C filter.

However, the total pulse width of the turn-on spike is decided by the output power, circuit design and PCB layout. It is strongly recommended to adopt a smaller R-C filter for higher power application to avoid the CS pin being damaged by the negative turn-on spike.

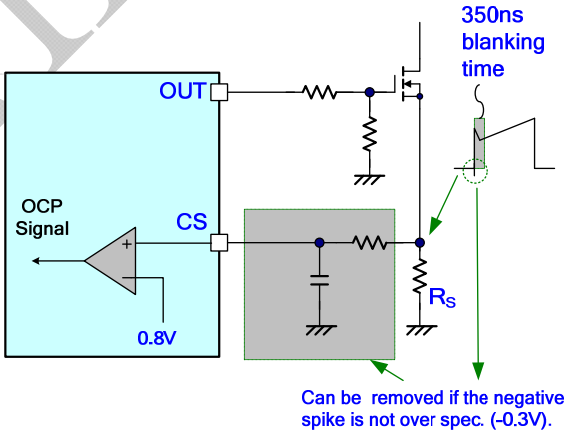


Fig. 20

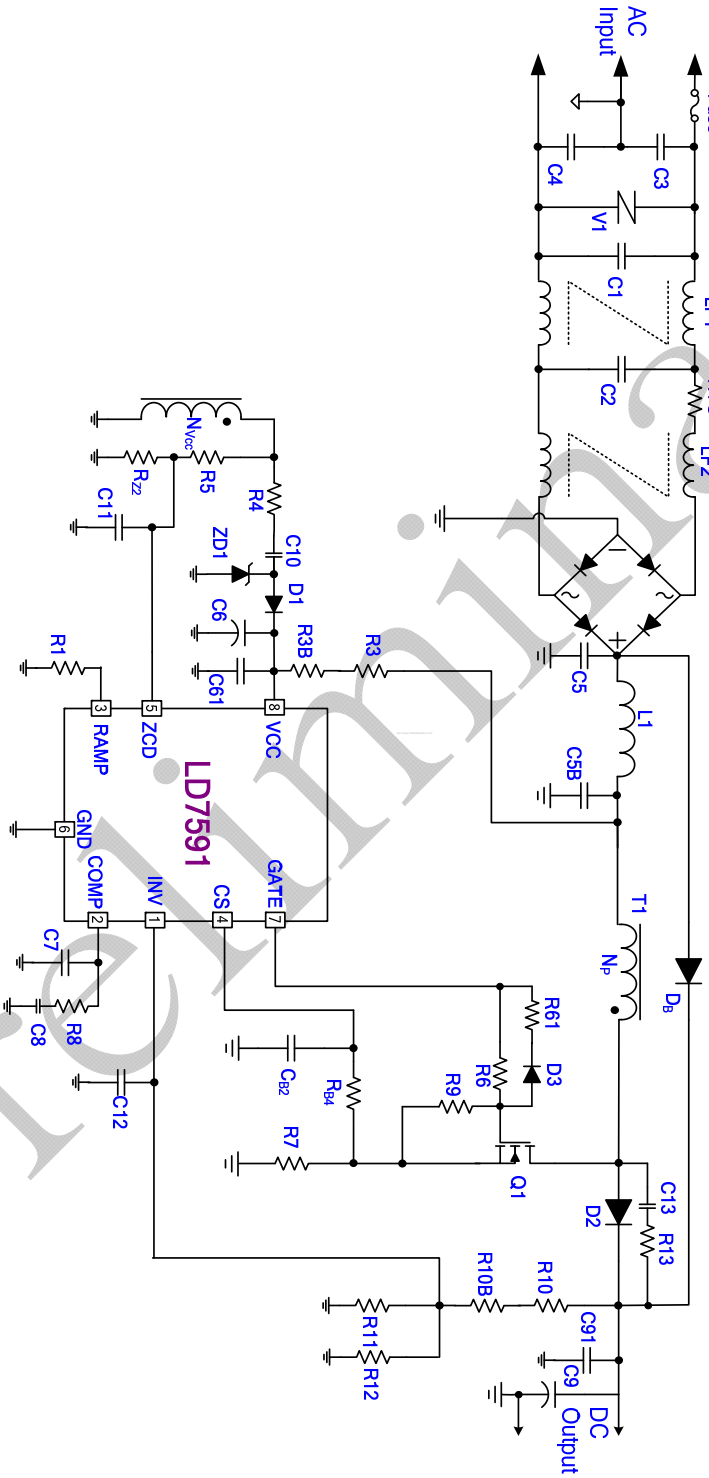
Fault Protection

There are several critical protections were integrated in the LD7591 to prevent the power supply or adapter had being damaged. Those damages usually come from open or short condition on the pins of LD7591.

Under the conditions listed below, the gate output will turn off immediately to protect the power circuit ---

1. Ramp pin short to ground
2. Ramp pin floating
3. CS pin floating

Reference Application Circuit --- 400V/100W (90~264V_{AC})

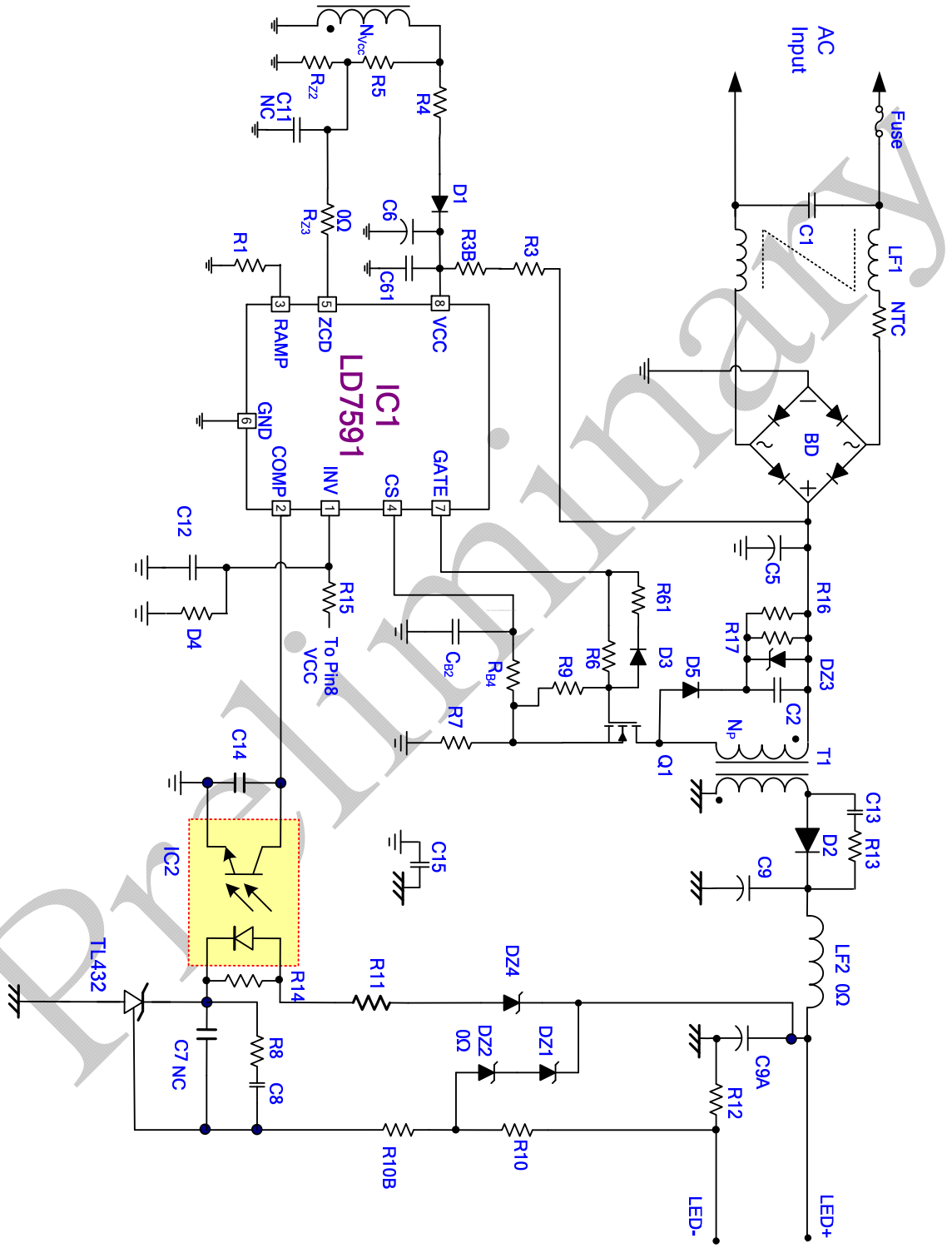


BOM

P/N	Component Value	
Fuse	250V,T2A	
NTC	3A,5Ω	
R1	24 kΩ, 0805	
R2	620 kΩ, 0805	
R3	330 kΩ, 1206	
R3B	330 kΩ, 1206	
R4	270 Ω, 1206	
R5	110 kΩ, 0805	
R6	24 Ω, 0805	
R61	24 Ω, 0805	
R7	0.18 Ω	1/2W
R8	10 kΩ, 0805	
R9	22 kΩ, 1206	
R10	2 MΩ, 1206	
R10B	2 MΩ, 1206	
R11	27 kΩ, 0805	
R12	360 kΩ, 0805	
R13	1 MΩ, 1206	
R14	1 MΩ, 1206	
R15	1 MΩ, 1206	
RZ2	11 kΩ, 0805	
RZ3	0 Ω, 0805	
RB4	200 Ω, 0805	

P/N	Component Value	Note
C1	0.1μF,X-cap	
C2	0.22μF,X-cap	
C3	2200pF,Y1-cap	
C4	2200pF,Y1-cap	
CY1	NC	
C5	0.47μF,400V	MPF
C5B	0.47μF,400V	MPF
C6	33μF, 50V	Electrolytic Capacitor
C61	100nF, 25V ,0805	
C7	100nF, 50V, 0805	
C8	220nF, 25V, 0805	
C9	100μF, 450V	Electrolytic Capacitor
C91	1000pF, 1kV, 1206	
C10	10nF, 100V, 1206	
C11	NC	
C12	100pF/ 16V, 0805	
C13	330pF/ 1kV/1206	
C14	100pF/ 1kV/1206	
CB2	100pF/16V, 0805	
D1	LL4148	SOD-80
D2	ER206	600V/ 2A, DO-15
D3	LL4148	SOD-80
DB	UF206G	600V/2A, DO-15
ZD1	GLZ18C, 18V Zener	SOD-80
BD	SBU4J or GBU4J	600V/4A
L1	Leadtrend's Design	
LF1	Leadtrend's Design	
LF2	Leadtrend's Design	
Q1	FQP13N50C	500V, 13A, TO-220
IC1	LD7591	SOP-8
V1	NC	Varistor
T1	400uH	EI30, 44/6

Reference Application Circuit --- LED -42V/350mA (90~264V_{AC})



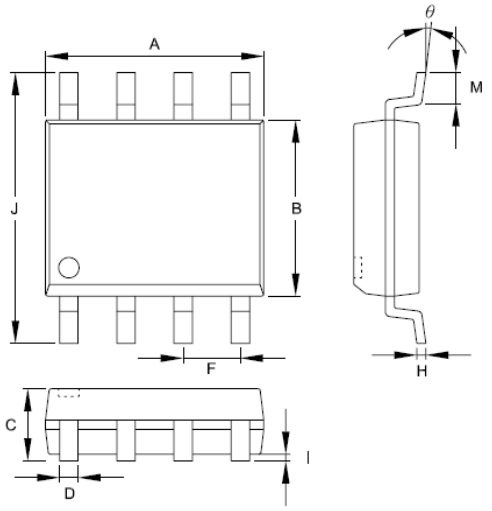
BOM

P/N	Component Value	
Fuse	2A/250V	
NTC	0Ω, 1206	
R1	18 kΩ, 0805	
R2	240 kΩ, 0805	
R3	300kΩ, 1206	
R3B	300kΩ, 1206	
R4	200 Ω, 1206	
R5	200 kΩ, 0805	
R6	51Ω, 0805	
R61	10Ω, 0805	
R7	0.6Ω	1/2W
R8	1 kΩ, 0805	
R9	22kΩ, 1206	
R10	1kΩ, 0805	
R10B	22kΩ, 0805	
R11	4.7kΩ, 0805	
R12	3.3Ω,	2W
R12B	NC,1206	
R13	NC, 1206	
R14	1 kΩ, 0805	
R15	7.5MEGΩ, 0805	
D4	600 kΩ, 0805	
R16	100kΩ, 1206	
R17	100kΩ, 1206	
RB4	220Ω, 0805	
RZ2	22 kΩ, 0805	
RZ3	0Ω, 0805	

P/N	Component Value	Note
C1	0.1μF / 275VAC	X-cap
C2	20nF/1kV,1206	
C5	0.1μF / 400V	MPF 塑膠電容
C6	33uF/ 25V	Electrolytic Capacitor
C61	104pF/25V/0805	
C7	NC uF/ 16V, 0805	
C8	0.68uF/ 16V, 0805	
C9	330μF, 50V	Electrolytic Capacitor
C9A	330μF, 50V	Electrolytic Capacitor
C10	0Ω, 1206	
C11	NC	
C12	10pF, 0805	
C13	NC	
C14	0.1μF/ 16V, 0805	
CB2	220pF/16V, 0805	
D1	LL4148	SOD-80
D2	ER502	200V/ 5A,
D3	LL4148	SOD-80
D5	PS106R	600V/1A
ZD1	NC	
DZ1	Zener, 43V	500mW
DZ2	0Ω, 0805	
DZ3	P6KE200A	DO-15
DZ4	Zener, 24V	
BD	DI106	600V/1A
T1	EF20, 1000uH	106/32/13
LF1	UU9.8	
LF2	0Ω	
Q1	FQPF5N60C	600V, 4.5A, TO-220
IC1	LD7591	SOP-8
IC2	PC817	
TL432	AHK432	

Package Information

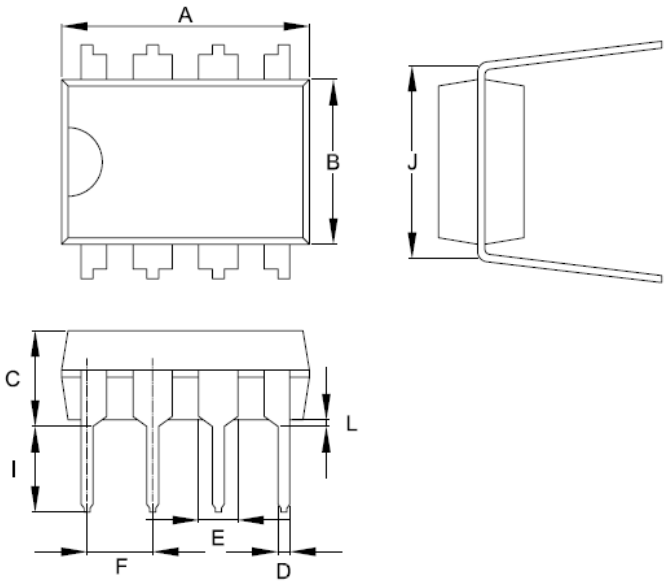
SOP-8



Symbols	Dimensions in Millimeters		Dimensions in Inch	
	MIN	MAX	MIN	MAX
A	4.801	5.004	0.189	0.197
B	3.810	3.988	0.150	0.157
C	1.346	1.753	0.053	0.069
D	0.330	0.508	0.013	0.020
F	1.194	1.346	0.047	0.053
H	0.178	0.229	0.007	0.009
I	0.102	0.254	0.004	0.010
J	5.791	6.198	0.228	0.244
M	0.406	1.270	0.016	0.050
θ	0°	8°	0°	8°

Package Information

DIP-8



Symbol	Dimension in Millimeters		Dimensions in Inches	
	Min	Max	Min	Max
A	9.017	10.160	0.355	0.400
B	6.096	7.112	0.240	0.280
C	-----	5.334	------	0.210
D	0.356	0.584	0.014	0.023
E	1.143	1.778	0.045	0.070
F	2.337	2.743	0.092	0.108
I	2.921	3.556	0.115	0.140
J	7.366	8.255	0.29	0.325
L	0.381	------	0.015	--------

Important Notice

Leadtrend Technology Corp. reserves the right to make changes or corrections to its products at any time without notice. Customers should verify the datasheets are current and complete before placing order.

Revision History

Rev.	Date	Change Notice
01	03/31/2009	Preliminary Specification
02	04/14/2009	Reverse Ton-max
03	04/30/2009	Ramp pin resistor, BOM