Stereo PDM-to-I²S or TDM Conversion IC

Data Sheet

ADAU7002

FEATURES

- 64× decimation of a stereo pulse density modulation (PDM) bit stream to pulse code modulation (PCM) audio data
- Slave I²S or time division multiplexed (TDM) output interface
- Configurable TDM slots
- I/O supply operation: 1.62 V to 3.6 V
- 64× output sample rate PDM clock
- 64×/128×/192×/256×/384×/512× output sample rate BCLK
- Automatic BCLK ratio detection
- Output sample rate: 4 kHz to 96 kHz
- Automatic PDM CLK drive at 64× the sample rate
- Automatic power down with BCLK removal
- 0.67 mA operating current at 48 kHz and 1.8 V IOVDD supply
- Shutdown current: <1 µA
- 8-ball, 1.56 mm × 0.76 mm, 0.4 mm pitch WLCSP
- Power-on reset

APPLICATIONS

- Mobile computing
- Portable electronics
- Consumer electronics

GENERAL DESCRIPTION

The ADAU7002 converts a stereo PDM bit stream into a PCM output. The source for the PDM data can be two microphones or other PDM sources. The PCM audio data is output on a serial audio interface port in either I²S or TDM format.

The ADAU7002 is specified over the commercial temperature range (−40°C to +85°C). It is available in a halide-free, 8-ball, 1.56 mm × 0.76 mm, wafer level chip scale package (WLCSP).

FUNCTIONAL BLOCK DIAGRAM

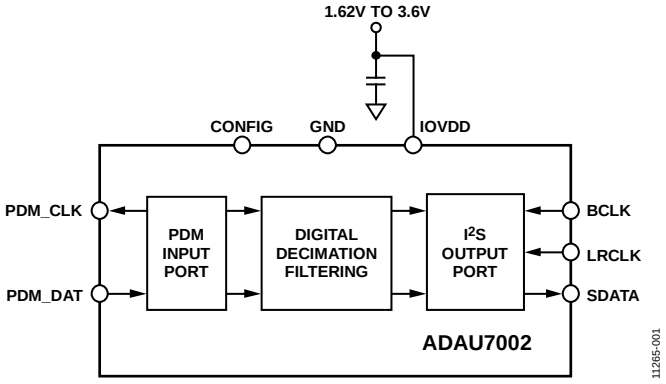

Figure 1.

Rev. 0

Document Feedback

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Technical Support
www.analog.com

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REVISION HISTORY

1/13—Revision 0: Initial Version

SPECIFICATIONS

IOVDD = 1.8 V, T_A = 25°C, BCLK = 3.072 MHz, output = 48 kHz, I^2S format, unless otherwise noted.

Table 1.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
DIGITAL INPUT/OUTPUT					
High Level Input Voltage (V_{IH})			0.7 × IOVDD		V
Low Level Input Voltage (V_{IL})			0.3 × IOVDD		V
Input Leakage, High (I_{IH})	BCLK and LRCLK pins			1	µA
Input Leakage, Low (I_{IL})	BCLK and LRCLK pins			1	µA
Input Capacitance				5	pF
SDATA			4.5		mA
PDM_CLK			9		mA
PERFORMANCE					
Dynamic Range	20 Hz to 20 kHz, −60 dB input				
With A-Weighted Filter (RMS)			110		dB
Signal-to-Noise-Ratio	A-weighted, fourth-order input		110		dB
Decimation Ratio			64×		
Frequency Response	DC to 0.45 output f_S	−0.1		+0.01	dB
Stop Band			0.566		f_S
Stop-Band Attenuation		60			dB
Group Delay	0.02 f_S input signal		3.31		LRCLK cycles
Gain	PDM to PCM		0		dB
Start-Up Time			48		LRCLK cycles
Bit Width	Internal and output		20		Bits
Interchannel Phase			0		Degrees
CLOCKING					
Output Sampling Rate	f_S LRCLK pulse rate	4	48	96	kHz
BCLK Frequency	f_{BCLK}	0.256	3.072	24.576	MHz
POWER SUPPLIES					
Supply Voltage Range	IOVDD	1.62		3.6	V
Supply Current	$IOVDD_{SY}$ = 1.8 V		0.67		mA
	IOVDD = 3.3 V		1.33		mA
	IOVDD = 1.8 V, 16 kHz output		0.21		mA
	IOVDD = 3.3 V, 16 kHz output		0.41		mA
Shutdown Current	$IOVDD_{SD}$, no input clocks		1		µA

ABSOLUTE MAXIMUM RATINGS

Absolute maximum ratings apply at 25°C, unless otherwise noted.

Table 2.

Parameter	Rating
IOVDD Supply Voltage	3.6 V
Input Voltage	3.6 V
ESD Susceptibility	4 kV
Storage Temperature Range	−65°C to +150°C
Operating Temperature Range	−40°C to +85°C
Junction Temperature Range	−65°C to +165°C
Lead Temperature (Soldering, 60 sec)	300°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL RESISTANCE

θ_{JA} (junction to air) is specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages. θ_{JA} is determined according to JESD51-9 on a 4-layer printed circuit board (PCB) with natural convection cooling.

Table 3. Thermal Resistance

Package Type	θ_{JA}	Unit
8-ball, 1.56 mm × 0.76 mm WLCSP	90	°C/W

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

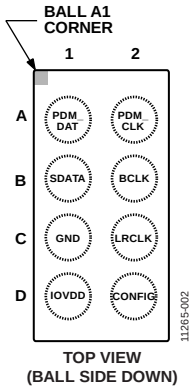

Figure 2. Pin Configuration (Top Side View)

Table 4. Pin Function Descriptions

Pin No.	Mnemonic	Type	Description
A1	PDM_DAT	Input	PDM Data Input
A2	PDM_CLK	Output	PDM Clock Output
B1	SDATA	Output	Serial Data Output for I²S/TDM
B2	BCLK	Input	Bit Clock for I²S/TDM
C1	GND	Ground	Ground
C2	LRCLK	Input	Left/Right Clock for I²S/Frame Sync for TDM
D1	IOVDD	Supply	Input/Output and Digital Supply
D2	CONFIG	Input	Configuration Pin

TYPICAL PERFORMANCE CHARACTERISTICS

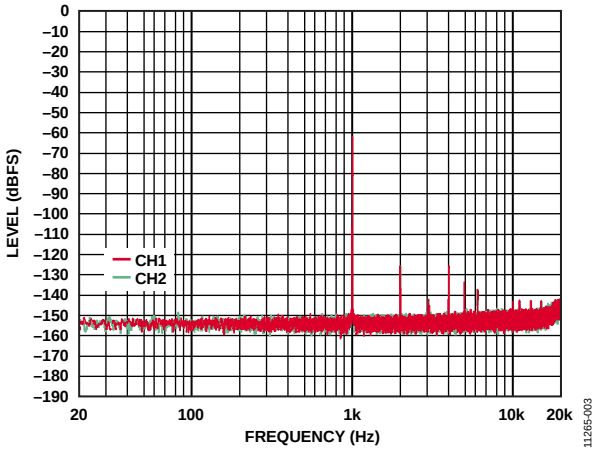

Figure 3. FFT, f_S = 48 kHz, −60 dBFS Input

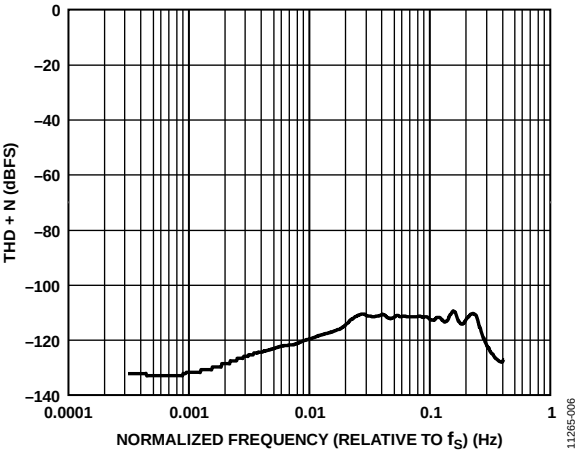

Figure 6. Total Harmonic Distortion + Noise (THD + N) vs. Normalized Frequency (Relative to f_S)

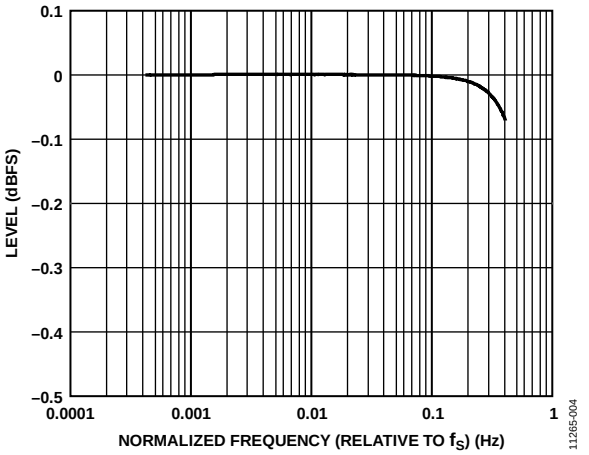

Figure 4. Frequency Response

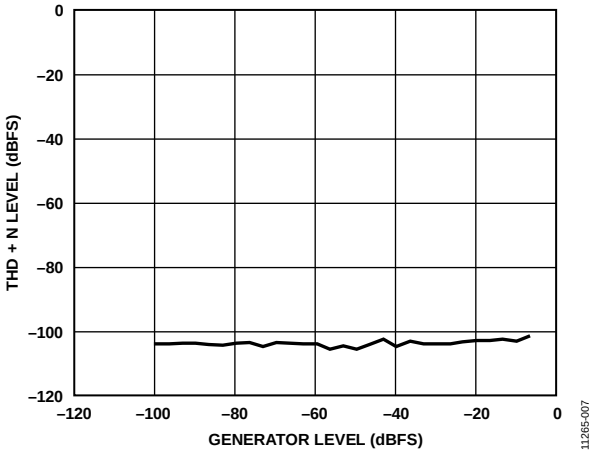

Figure 7. THD + N Level vs. Generator Level

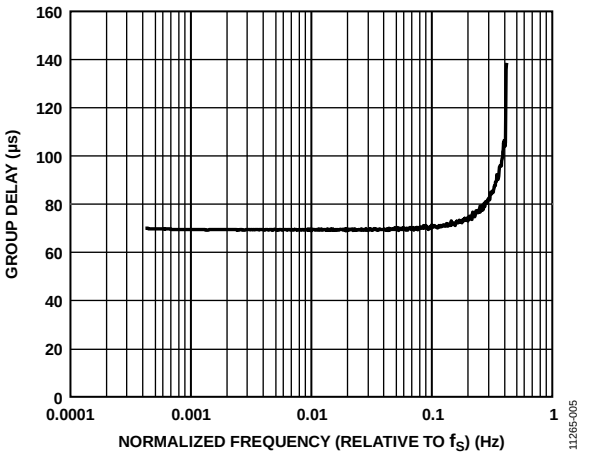

Figure 5. Group Delay vs. Normalized Frequency (Relative to f_S)

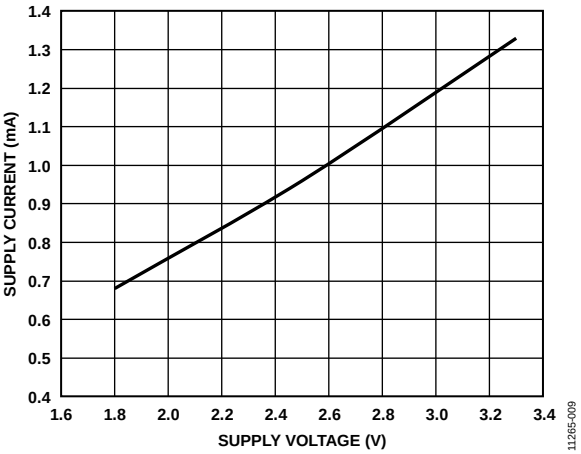

Figure 8. Supply Current vs. Supply Voltage

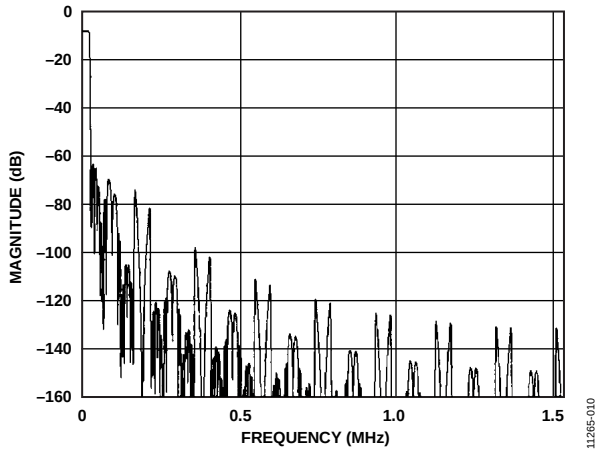

Figure 9. Out-of-Band Frequency Response (48 kHz Output)

TYPICAL APPLICATION CIRCUIT

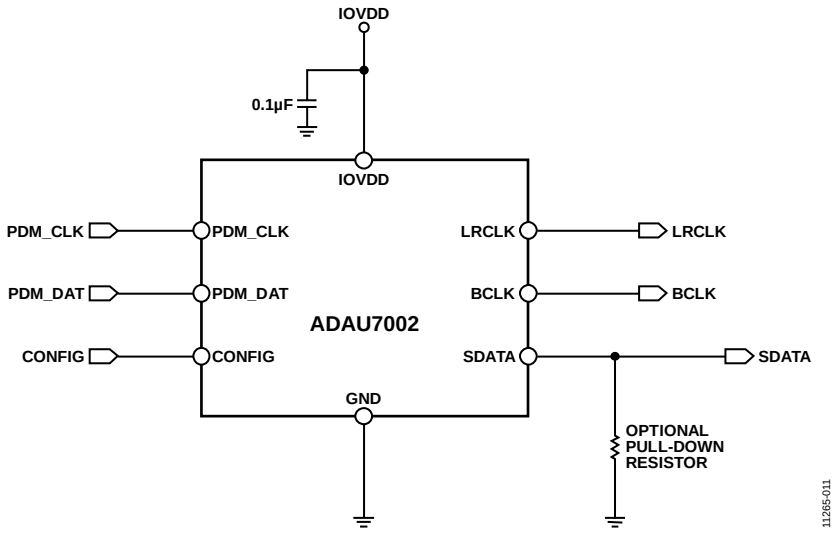

Figure 10. Typical Application Circuit

APPLICATIONS INFORMATION

OVERVIEW

The ADAU7002 provides stereo decimation from a 1-bit PDM source to a 20-bit PCM audio. The downsampling ratio is fixed at 64×. The 20-bit downsampled PCM audio is output via standard I²S or TDM formats.

The input source for the ADAU7002 can be any device that has a PDM output, such as a digital microphone like the ADMP521. The output pins of these microphones can connect directly to the input pins of the ADAU7002.

CLOCKING

The ADAU7002 requires a BCLK rate that is a minimum of 64× the LRCLK sample rate. BCLK rates of 128×, 192×, 256×, 384×, and 512× the LRCLK rate are also supported. The ADAU7002 automatically detects the ratio between BCLK and LRCLK and generates a PDM clock output at 64× the LRCLK rate. The minimum sample rate is 4 kHz, and the maximum is 96 kHz, which correspond to a PDM clock range of 256 kHz to 6.144 MHz. Internally, all processing is done at the PDM_CLK rate.

When BCLK is removed, the ADAU7002 powers down automatically. When BCLK is not present, the PDM_CLK output stops.

Table 5. PDM Timing Parameters

Parameter	t_{MIN}	t_{MAX}	Unit
Data Setup Time, t_{SETUP}	10		ns
Data Hold Time, t_{HOLD}	7		ns

PDM data is latched on both edges of the clock.

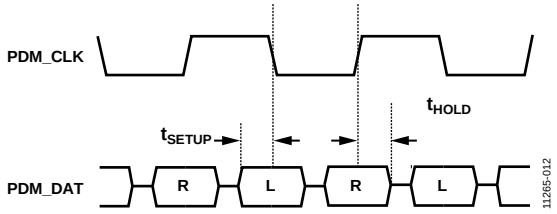

Figure 11. PDM Timing Diagram

SERIAL AUDIO OUTPUT INTERFACE

The ADAU7002 supports I²S and TDM serial output formats. Format selection and TDM slot placement is set with the CONFIG pin. The SDATA pin is in tristate mode, except when the port is driving serial data based on the CONFIG pin configuration.

Table 6. TDM Slot Selection

Device Setting	CONFIG Pin Configuration
I²S Format	Tie to IOVDD
TDM Slot 1 to Slot 2 Used/Driven, 32-Bit Slots	Tie to GND
TDM Slot 3 to Slot 4 Used/Driven, 32-Bit Slots	Open
TDM Slot 5 to Slot 6 Used/Driven, 32-Bit Slots	Tie to IOVDD through a 47 kΩ resistor
TDM Slot 7 to Slot 8 Used/Driven, 32-Bit Slots	Tie to GND through a 47 kΩ resistor

Serial Port Timing

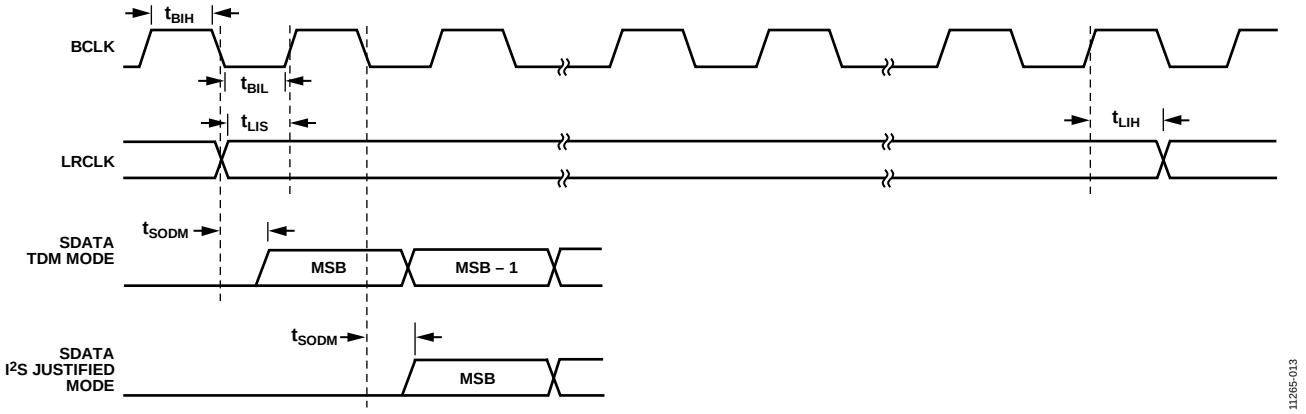

Figure 12. Serial Port Timing Diagram

Table 7. I²S/TDM Timing Parameters

Parameter	Symbol	t_{MIN}	t_{MAX}	Unit
BCLK Pulse Width High	t_{BIH}	10		ns
BCLK Pulse Width Low	t_{BIL}	10		ns
LRCLK Setup Time	t_{LIS}	10		ns
LRCLK Hold Time	t_{LIH}	10		ns
Time from BCLK Falling	t_{SODM}		10	ns

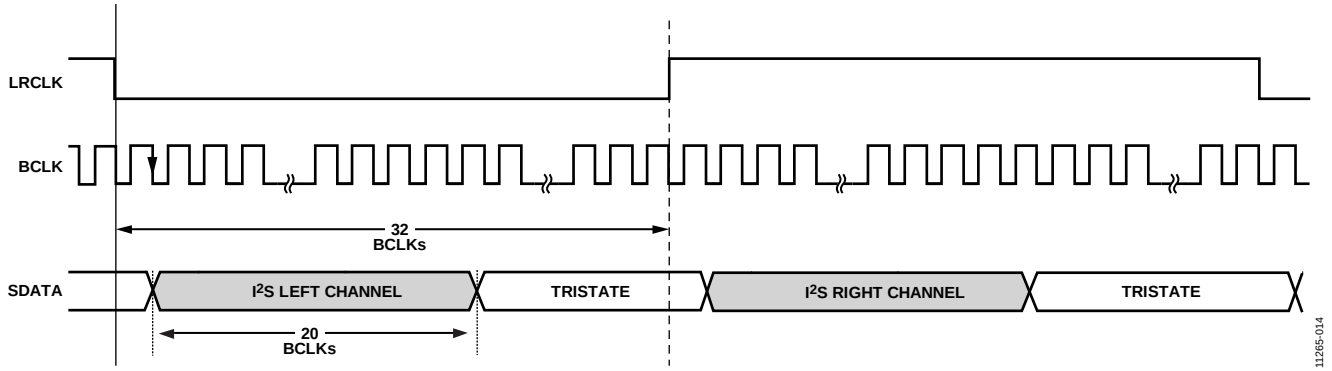

Figure 13. I²S, CONFIG Pin Tied to IOVDD

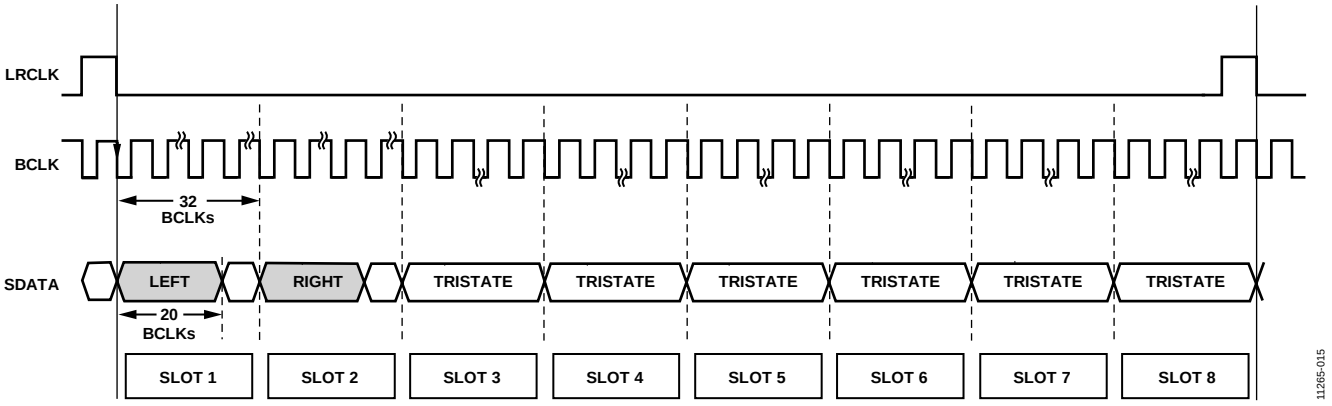

Figure 14. TDM8 Channel 1 and Channel 2, CONFIG Pin Tied to GND

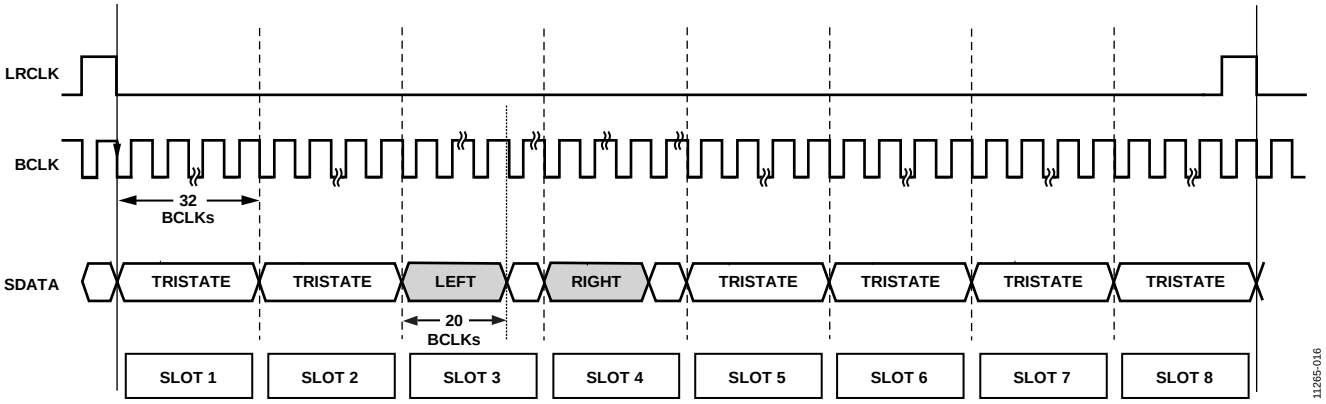

Figure 15. TDM8 Channel 3 and Channel 4, CONFIG Pin Open

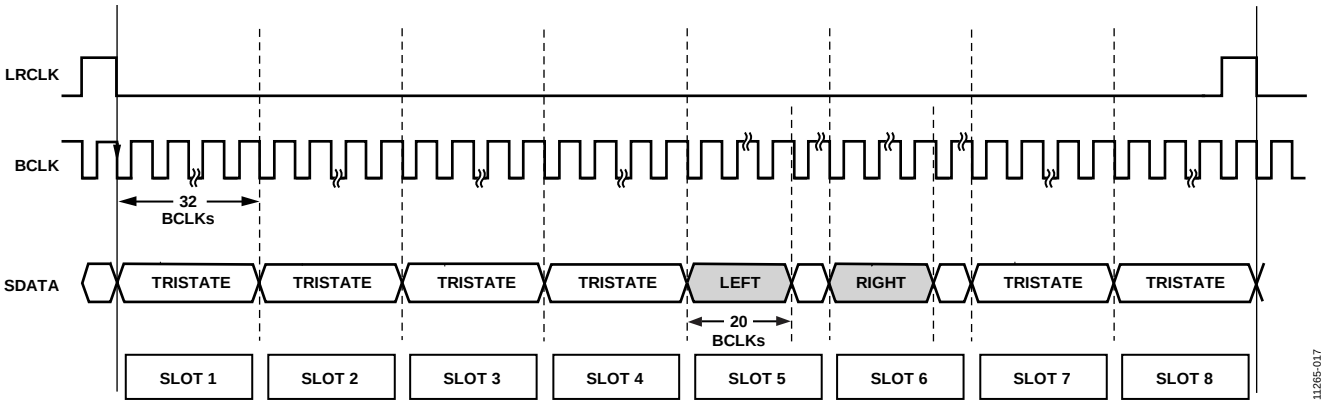

Figure 16. TDM8 Channel 5 to Channel 6, CONFIG Pin Tied to IOVDD Through a 47 kΩ Resistor

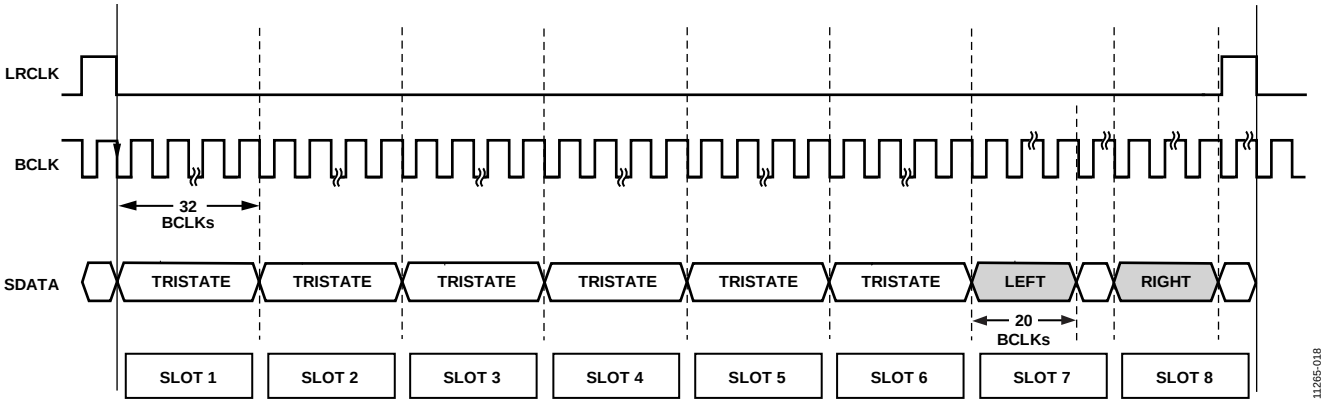

Figure 17. TDM8 Channel 7 and Channel 8, CONFIG Pin Tied to GND Through a 47 kΩ Resistor

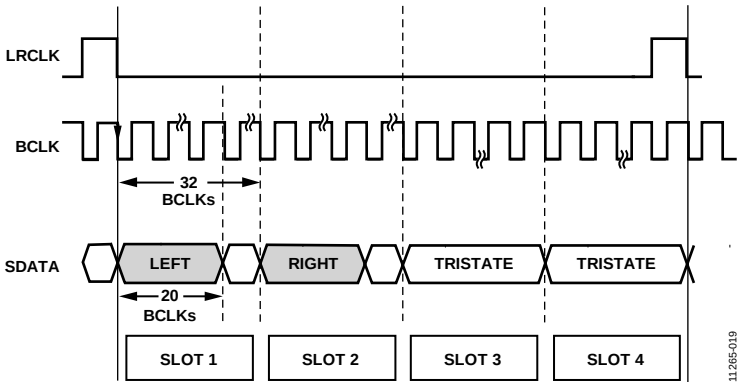

Figure 18. TDM4 Channel 1 and Channel 2, CONFIG Pin Tied to IOVDD

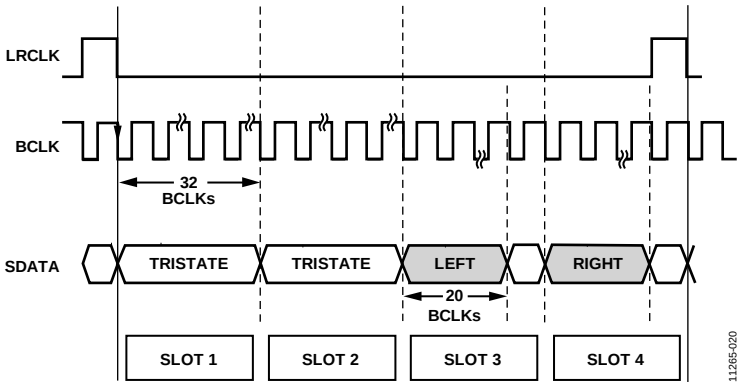

Figure 19. TDM4 Channel 3 and Channel 4, CONFIG Pin Open

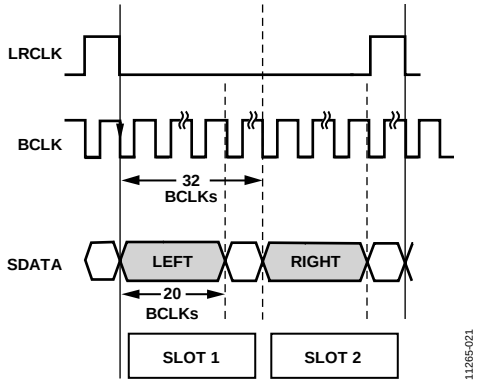

Figure 20. TDM2 Channel 1 and Channel 2, CONFIG Pin Tied to IOVDD

OUTLINE DIMENSIONS

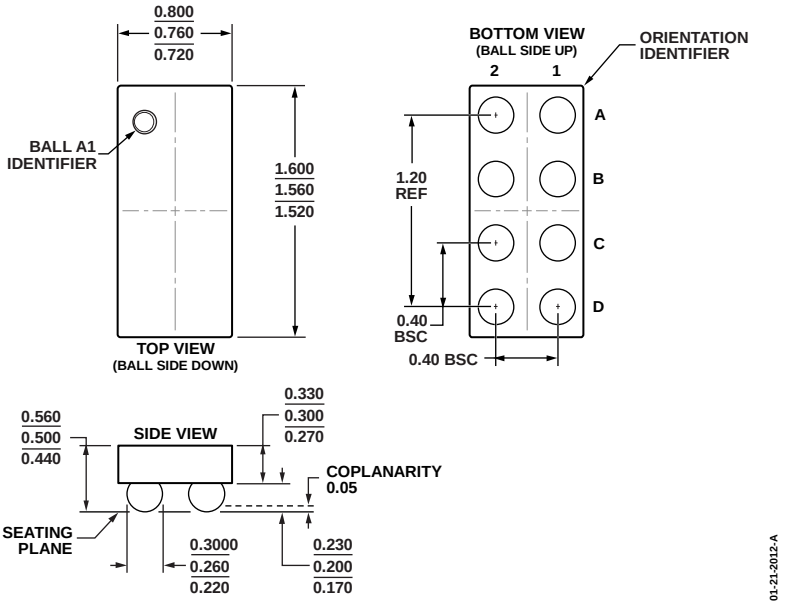

Figure 21. 8-Ball Wafer Level Chip Scale Package [WLCSP]
(CB-8-6)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option	Branding
ADAU7002ACBZ-R7	−40°C to +85°C	8-Ball Wafer Level Chip Scale Package [WLCSP], 7″ Tape and Reel	CB-8-6	BE
ADAU7002ACBZ-RL	−40°C to +85°C	8-Ball Wafer Level Chip Scale Package [WLCSP], 13″ Tape and Reel	CB-8-6	BE
EVAL-ADAU7002Z		Evaluation Board		

[1] Z = RoHS Compliant Part.

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