FlashFlex51 MCU

SST89E51RC / SST89E52RC / SST89E54RC
SST89V51RC / SST89V52RC / SST89V54RC

Preliminary Specifications

FEATURES:

- **8-bit 8051-Compatible Microcontroller (MCU) with Embedded SuperFlash Memory**
  - Fully Software Compatible
  - Development Toolset Compatible
  - Pin-for-Pin Package Compatible
- **SST89E5xRC Operation**
  - 0 to 40 MHz at 5V
- **SST89V5xRC Operation**
  - 0 to 33 MHz at 3V
- **Total 512 Byte Internal RAM (256 Byte by default + 256 Byte enabled by software)**
- **Single Block SuperFlash EEPROM**
  - SST89E/V54RC: 16 KByte primary partition + 1 KByte secondary partition
  - SST89E/V52RC: 8 KByte primary partition + 1 KByte secondary partition
  - SST89E/V51RC: 4 KByte primary partition + 1 KByte secondary partition
  - Primary Partition is divided into Four Pages
  - Secondary Partition has One Page
  - Individual Page Security Lock
  - In-System Programming (ISP)
  - In-Application Programming (IAP)
  - Small-Sector Architecture: 128-Byte Sector Size
- **Support External Address Range up to 64 KByte of Program and Data Memory**
- **Three High-Current Port 1 pins (16 mA each)**
- **Three 16-bit Timers/Counters**
- **Full-Duplex, Enhanced UART**
  - Framing error detection
  - Automatic address recognition
- **Eight Interrupt Sources at 4 Priority Levels**
- **Programmable Watchdog Timer (WDT)**
- **Programmable Counter Array (PCA)**
- **Four 8-bit I/O Ports (32 I/O Pins)**
- **Second DPTR register**
- **Low EMI Mode (Inhibit ALE)**
- **SPI Serial Interface**
- **Standard 12 Clocks per cycle, the device has an option to double the speed to 6 clocks per cycle.**
- **TTL- and CMOS-Compatible Logic Levels**
- **Low Power Modes**
  - Power-down Mode with External Interrupt Wake-up
  - Idle Mode
- **Selectable Operation Clock**
  - Divide down to 1/4, 1/16, 1/256, or 1/1024th
- **Temperature Ranges:**
  - Commercial (0°C to +70°C)
  - Industrial (-40°C to +85°C)
- **Packages Available**
  - 44-lead PLCC
  - 44-lead TQFP
- **All non-Pb (lead-free) devices are RoHS compliant**

PRODUCT DESCRIPTION

The SST89E/V54RC, SST89E/V52RC, and SST89E/V51RC are members of the FlashFlex51 family of 8-bit microcontroller products designed and manufactured with SST's patented and proprietary SuperFlash CMOS semiconductor process technology. The split-gate cell design and thick-oxide tunneling injector offer significant cost and reliability benefits for our customers.The devices use the 8051 instruction set and are pin-for-pin compatible with standard 8051 microcontroller devices.

The device comes with 17/9/5 KByte of on-chip flash EEPROM program memory which is divided into 2 independent program memory partitions. The primary partition occupies 16/8/4 KByte of internal program memory space and the secondary partition occupies 1 KByte of internal program memory space.

The flash memory can be programmed via a standard 87C5x OTP EPROM programmer fitted with a special adapter and firmware for SST's devices. During power-on reset, the devices can be configured as either a slave to an external host for source code storage or a master to an external host for an in-system programming (ISP) operation. The devices are designed to be programmed in-system on the printed circuit board for maximum flexibility. The device is pre-programmed with an example of the bootstrap loader in memory, demonstrating the initial user program code loading or subsequent user code updating via an ISP operation. A sample bootstrap loader is available for the user's reference and convenience only; SST does not guarantee its functionality or usefulness. Chip-Erase operations will erase the pre-programmed sample code.

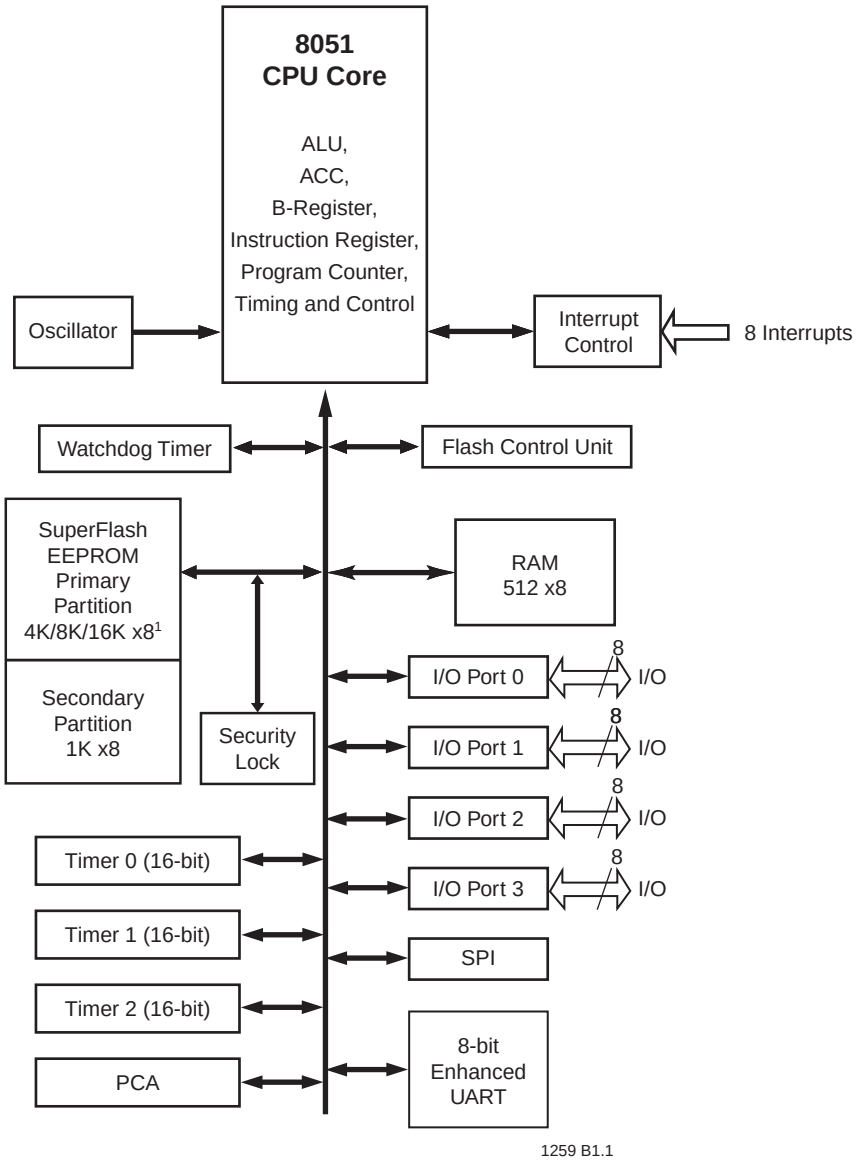
In addition to 17/9/5 KByte of SuperFlash EEPROM program memory on-chip, the device can address up to 64 KByte of external program memory. In addition to 512 x8 bits of on-chip RAM, up to 64 KByte of external RAM can be addressed.

Preliminary Specifications

SST's highly reliable, patented SuperFlash technology and memory cell architecture have a number of important advantages for designing and manufacturing flash EEPROMs. These advantages translate into significant cost and reliability benefits for our customers.

1.0 FUNCTIONAL BLOCKS

FUNCTIONAL BLOCK DIAGRAM



1. 16K x8 for SST89E/V54RC
   8K x8 for SST89E/V52RC
   4K x8 for SST89E/V51RC

2.0 PIN ASSIGNMENTS

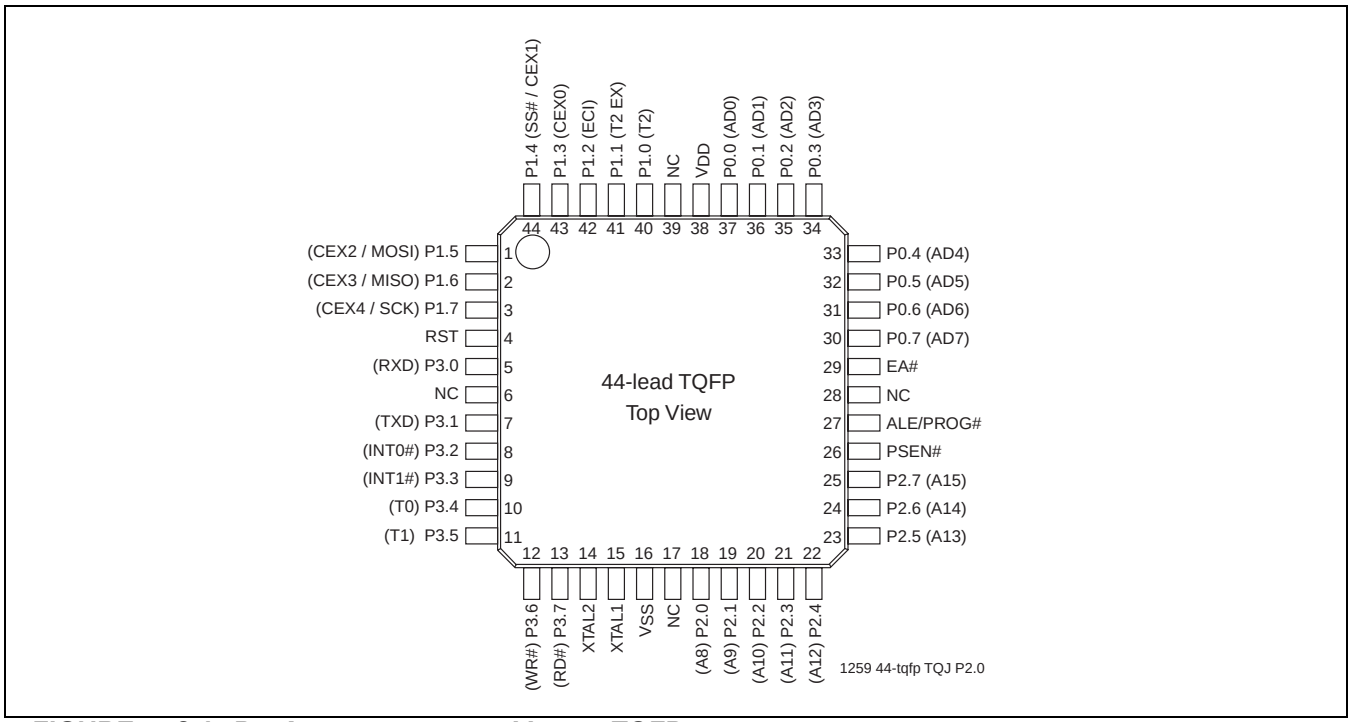


FIGURE 2-1: PIN ASSIGNMENTS FOR 44-LEAD TQFP

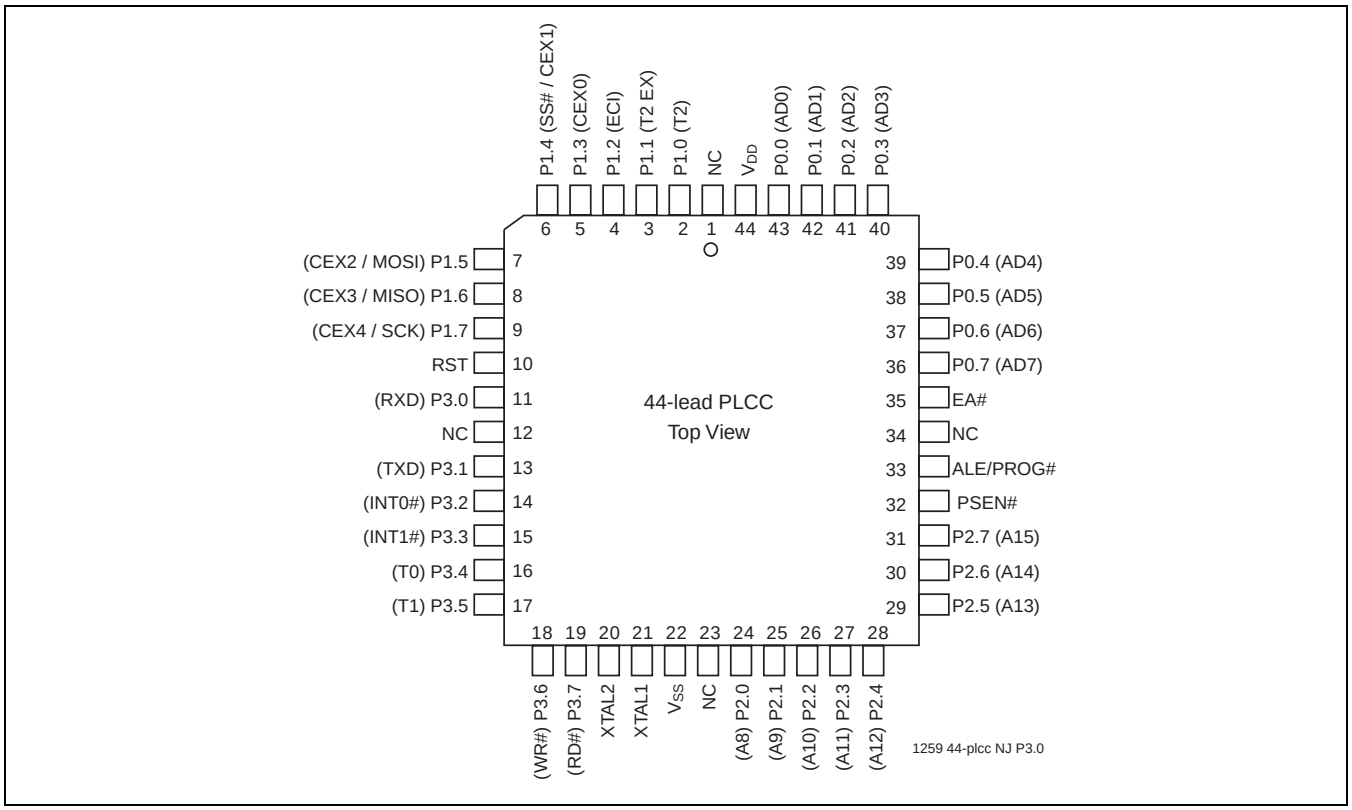


FIGURE 2-2: PIN ASSIGNMENTS FOR 44-LEAD PLCC

2.1 Pin Descriptions

TABLE 2-1: PIN DESCRIPTIONS (1 OF 2)

Symbol	Type[1]	Name and Functions
P0[7:0]	I/O	**Port 0:** Port 0 is an 8-bit open drain bi-directional I/O port. As an output port each pin can sink several LS TTL inputs. Port 0 pins that have '1's written to them float, and in this state can be used as high-impedance inputs. Port 0 is also the multiplexed low-order address and data bus during accesses to external code and data memory. In this application, it uses strong internal pull-ups when transitioning to '1's. Port 0 also receives the code bytes during the external host mode programming, and outputs the code bytes during the external host mode verification. External pull-ups are required during program verification or as a general purpose I/O port.
P1[7:0]	I/O with internal pull-up	**Port 1:** Port 1 is an 8-bit bi-directional I/O port with internal pull-ups. The Port 1 output buffers can drive LS TTL inputs. Port 1 pins are pulled high by the internal pull-ups when '1's are written to them and can be used as inputs in this state. As inputs, Port 1 pins that are externally pulled low will source current because of the internal pull-ups. P1[5, 6, 7] have high current drive of 16 mA. Port 1 also receives the low-order address byte during the external host mode programming and verification.
P1[0]	I/O	**T2:** External count input to Timer/Counter 2 or Clock-out from Timer/Counter 2
P1[1]	I	**T2EX:** Timer/Counter 2 capture/reload trigger and direction control
P1[2]	I	**ECI:** External Clock Input This signal is the external clock input for the PCA.
P1[3]	I/O	**CEX0:** Capture/Compare External I/O for PCA Module 0 Each capture/compare module connects to a Port 1 pin for external I/O. When not used by the PCA, this pin can handle standard I/O.
P1[4]	I/O	**SS#:** Slave port select input for SPI **OR** **CEX1:** Capture/Compare External I/O for PCA Module 1
P1[5]	I/O	**MOSI:** Master Output line, Slave Input line for SPI **OR** **CEX2:** Capture/Compare External I/O for PCA Module 2
P1[6]	I/O	**MISO:** Master Input line, Slave Output line for SPI **OR** **CEX3:** Capture/Compare External I/O for PCA Module 3
P1[7]	I/O	**SCK:** Master clock output, slave clock input line for SPI **OR** **CEX4:** Capture/Compare External I/O for PCA Module 4
P2[7:0]	I/O with internal pull-up	**Port 2:** Port 2 is an 8-bit bi-directional I/O port with internal pull-ups. Port 2 pins are pulled high by the internal pull-ups when '1's are written to them and can be used as inputs in this state. As inputs, Port 2 pins that are externally pulled low will source current because of the internal pull-ups. Port 2 sends the high-order address byte during fetches from external program memory and during accesses to external Data Memory that use 16-bit address (MOVX@DPTR). In this application, it uses strong internal pull-ups when transitioning to '1's. Port 2 also receives the high-order address byte during the external host mode programming and verification.
P3[7:0]	I/O with internal pull-up	**Port 3:** Port 3 is an 8-bit bidirectional I/O port with internal pull-ups. The Port 3 output buffers can drive LS TTL inputs. Port 3 pins are pulled high by the internal pull-ups when '1's are written to them and can be used as inputs in this state. As inputs, Port 3 pins that are externally pulled low will source current because of the internal pull-ups. Port 3 also receives the high-order address byte during the external host mode programming and verification.
P3[0]	I	**RXD:** Universal Asynchronous Receiver/Transmitter (UART) - Receive input
P3[1]	O	**TXD:** UART - Transmit output
P3[2]	I	**INT0#:** External Interrupt 0 Input

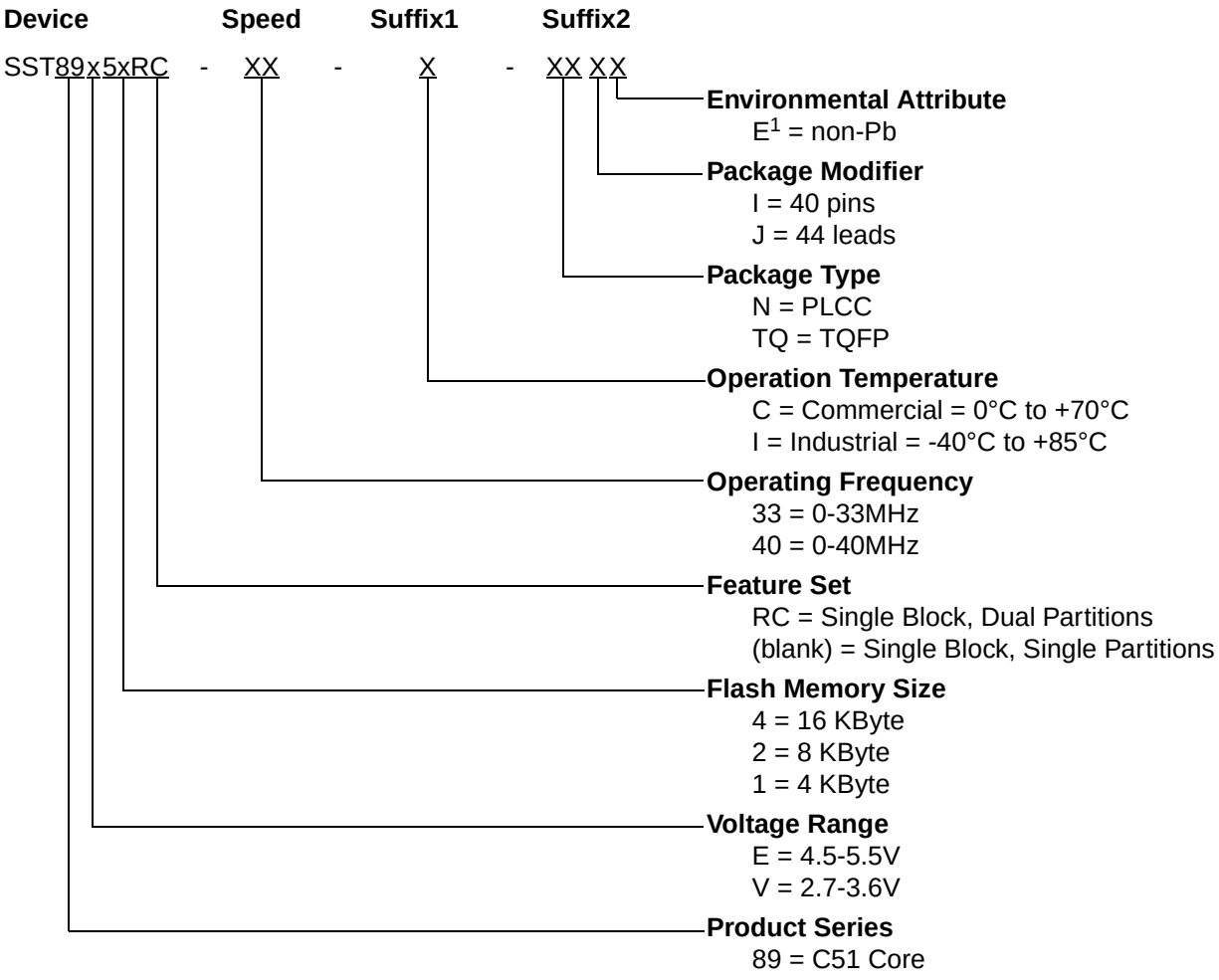
TABLE 2-1: PIN DESCRIPTIONS (CONTINUED) (2 OF 2)

Symbol	Type[1]	Name and Functions
P3[3]	I	**INT1#:** External Interrupt 1 Input
P3[4]	I	**T0:** External count input to Timer/Counter 0
P3[5]	I	**T1:** External count input to Timer/Counter 1
P3[6]	O	**WR#:** External Data Memory Write strobe
P3[7]	O	**RD#:** External Data Memory Read strobe
PSEN#	I/O	**Program Store Enable:** PSEN# is the Read strobe to external program. When the device is executing from internal program memory, PSEN# is inactive (High). When the device is executing code from external program memory, PSEN# is activated twice each machine cycle, except that two PSEN# activations are skipped during each access to external data memory. A forced high-to-low input transition on the PSEN# pin while the RST input is continually held high for more than 10 machine cycles will cause the device to enter external host mode programming.
RST	I	**Reset:** While the oscillator is running, a “high” logic state on this pin for two machine cycles will reset the device. If the PSEN# pin is driven by a high-to-low input transition while the RST input pin is held “high,” the device will enter the external host mode, otherwise the device will enter the normal operation mode.
EA#	I	**External Access Enable:** EA# must be connected to V_{SS} in order to enable the device to fetch code from the external program memory. EA# must be strapped to V_{DD} for internal program execution. However, Disable-Extern-Boot will disable EA#, and program execution is only possible from internal program memory. The EA# pin can tolerate a high voltage[2] of 12V.
ALE/PROG#	I/O	**Address Latch Enable:** ALE is the output signal for latching the low byte of the address during an access to external memory. This pin is also the programming pulse input (PROG#) for flash programming. Normally the ALE[3] is emitted at a constant rate of 1/6 the crystal frequency[4] and can be used for external timing and clocking. One ALE pulse is skipped during each access to external data memory. However, if AO is set to 1, ALE is disabled.
NC	I/O	**No Connect**
XTAL1	I	**Crystal 1:** Input to the inverting oscillator amplifier and input to the internal clock generator circuits.
XTAL2	O	**Crystal 2:** Output from the inverting oscillator amplifier.
V_{DD}	I	**Power Supply**
V_{SS}	I	**Ground**

T2-1.0 1259

1. I = Input; O = Output
2. It is not necessary to receive a 12V programming supply voltage during flash programming.
3. ALE loading issue: When ALE pin experiences higher loading (>30pf) during the reset, the MCU may accidentally enter into modes other than normal working mode. The solution is to add a pull-up resistor of 3-50 KΩ to V_{DD}, e.g. for ALE pin.
4. For 6 clock mode, ALE is emitted at 1/3 of crystal frequency.

3.0 PRODUCT ORDERING INFORMATION



1. Environmental suffix “E” denotes non-Pb solder.
SST non-Pb solder devices are “RoHS Compliant”.

3.1 Valid Combinations

Valid combinations for SST89E51RC

SST89E51RC-40-C-NJ	SST89E51RC-40-C-TQJ
SST89E51RC-40-C-NJE	SST89E51RC-40-C-TQJE
SST89E51RC-40-I-NJ	SST89E51RC-40-I-TQJ
SST89E51RC-40-I-NJE	SST89E51RC-40-I-TQJE

Valid combinations for SST89V51RC

SST89V51RC-33-C-NJ	SST89V51RC-33-C-TQJ
SST89V51RC-33-C-NJE	SST89V51RC-33-C-TQJE
SST89V51RC-33-I-NJ	SST89V51RC-33-I-TQJ
SST89V51RC-33-I-NJE	SST89V51RC-33-I-TQJE

Valid combinations for SST89E52RC

SST89E52RC-40-C-NJ	SST89E52RC-40-C-TQJ
SST89E52RC-40-C-NJE	SST89E52RC-40-C-TQJE
SST89E52RC-40-I-NJ	SST89E52RC-40-I-TQJ
SST89E52RC-40-I-NJE	SST89E52RC-40-I-TQJE

Valid combinations for SST89V52RC

SST89V52RC-33-C-NJ	SST89V52RC-33-C-TQJ
SST89V52RC-33-C-NJE	SST89V52RC-33-C-TQJE
SST89V52RC-33-I-NJ	SST89V52RC-33-I-TQJ
SST89V52RC-33-I-NJE	SST89V52RC-33-I-TQJE

Valid combinations for SST89E54RC

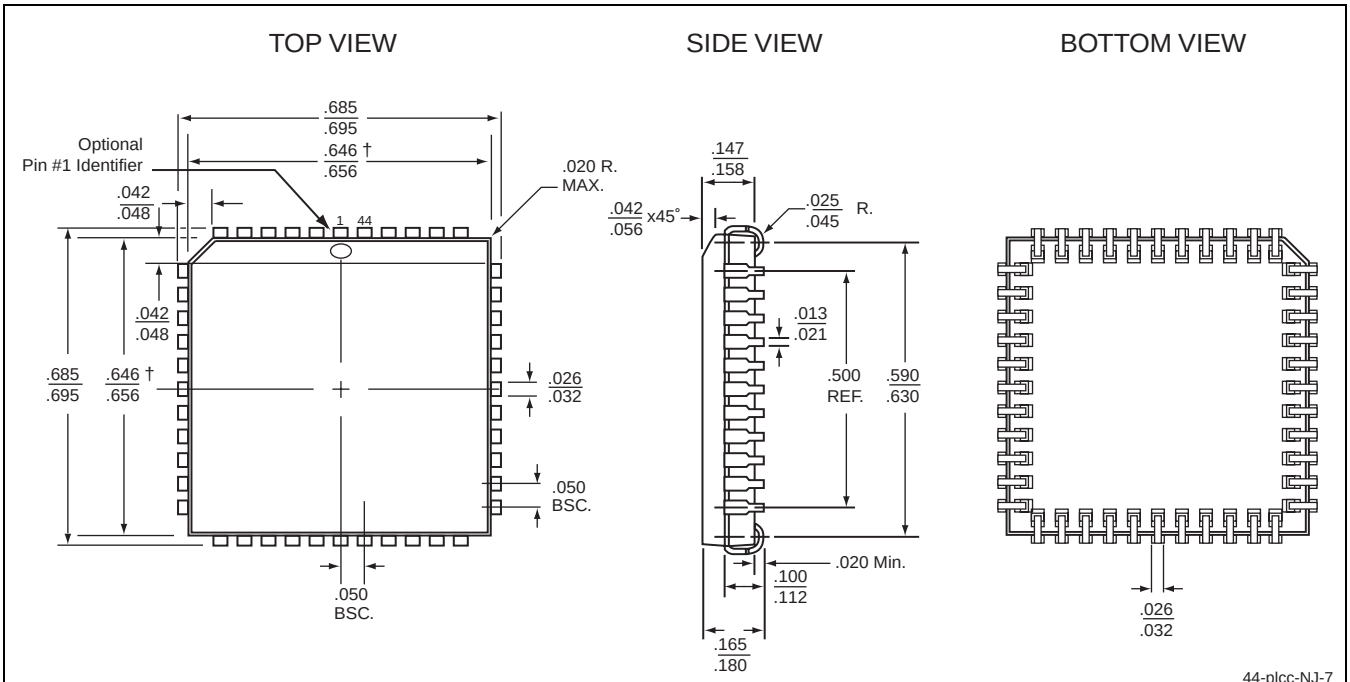
SST89E54RC-40-C-NJ	SST89E54RC-40-C-TQJ
SST89E54RC-40-C-NJE	SST89E54RC-40-C-TQJE
SST89E54RC-40-I-NJ	SST89E54RC-40-I-TQJ
SST89E54RC-40-I-NJE	SST89E54RC-40-I-TQJE

Valid combinations for SST89V54RC

SST89V54RC-33-C-NJ	SST89V54RC-33-C-TQJ
SST89V54RC-33-C-NJE	SST89V54RC-33-C-TQJE
SST89V54RC-33-I-NJ	SST89V54RC-33-I-TQJ
SST89V54RC-33-I-NJE	SST89V54RC-33-I-TQJE

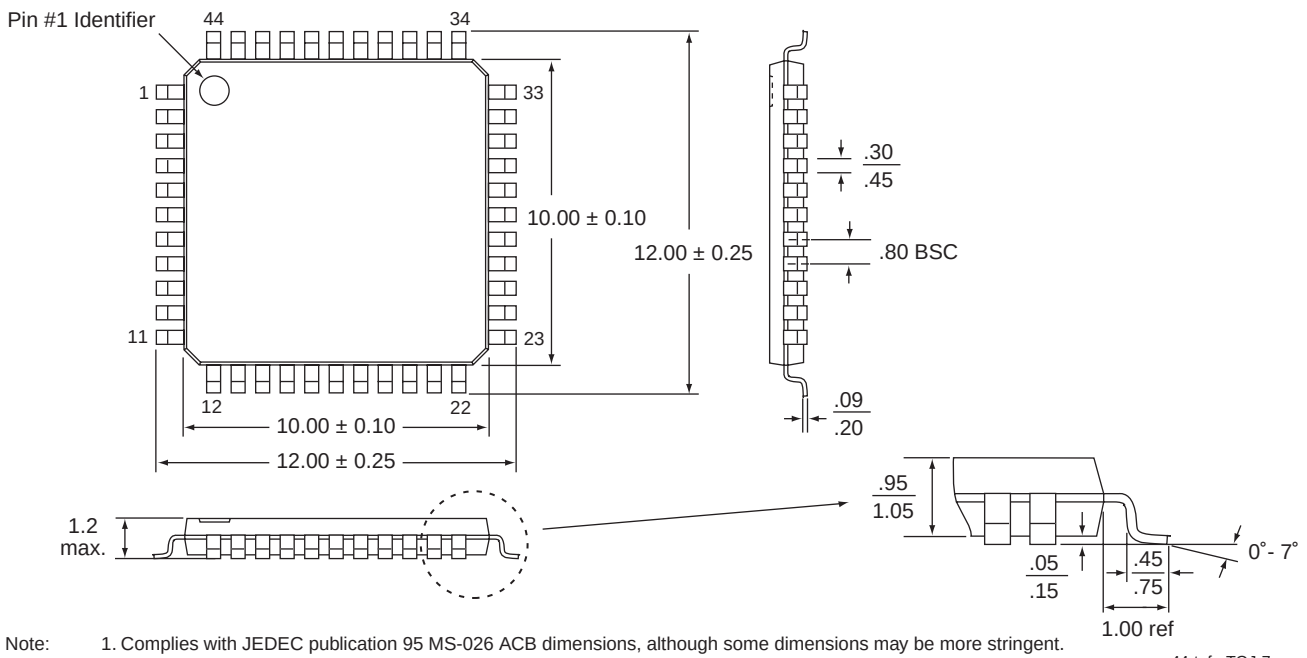
Note: Valid combinations are those products in mass production or will be in mass production. Consult your SST sales representative to confirm availability of valid combinations and to determine availability of new combinations.

4.0 PACKAGING DIAGRAMS



Note: 1. Complies with JEDEC publication 95 MS-018 AC dimensions (except as noted), although some dimensions may be more stringent.
† = JEDEC min is .650; SST min is *less* stringent
2. All linear dimensions are in inches (min/max).
3. Dimensions do not include mold flash. Maximum allowable mold flash is .008 inches.
4. Coplanarity: 4 mils.

44-LEAD PLASTIC LEAD CHIP CARRIER (PLCC)
SST PACKAGE CODE: NJ



Note:
1. Complies with JEDEC publication 95 MS-026 ACB dimensions, although some dimensions may be more stringent.
2. All linear dimensions are in millimeters (min/max).
3. Coplanarity: 0.1 (±0.05) mm.
4. Package body dimensions do not include mold flash. Maximum allowable mold flash is .25mm.

44-LEAD THIN QUAD FLAT PACK (TQFP)
SST PACKAGE CODE: TQJ