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RENESAS

MOS INTEGRATED CIRCUIT

μPD780701Y, 780702Y

8-BIT SINGLE-CHIP MICROCONTROLLER

DESCRIPTION

The μPD780701Y and 780702Y are the μPD780701Y Subseries products of the 78K/0 Series. These microcontrollers have DCAN controller (μPD780701Y), IEBus™ controller (μPD780702Y), A/D converter, timer, serial interface, interrupt control, and various other peripheral hardware.

The μPD78F0701Y which can operate in the same power supply voltage as the mask ROM version, and various development tools are under development.

Detailed function descriptions are provided in the following user's manuals. Be sure to read them before designing.

μPD780701Y Subseries User's Manual: U13781E
78K/0 Series User's Manual Instructions: U12326E

FEATURES

- DCAN (Direct Storage Controller Area Network) controller (incorporated in μPD780701Y)
- IEBus (Inter Equipment Bus™) controller (incorporated in μPD780702Y)
- Internal ROM: 60 Kbytes
- Internal high-speed RAM: 1024 bytes
- Internal expansion RAM: 2048 bytes
- Buffer RAM for DCAN: 288 bytes (μPD780701Y only)
- Minimum instruction execution time can be changed from high-speed (0.32 μs) to low-speed (5.09 μs)
- I/O ports: 67
- 8-bit resolution A/D converter: 16 channels
- Serial interface: 4 channels
- Timer: 7 channels
- Power supply voltage: V_{DD} = 3.5 to 5.5 V

APPLICATIONS

Car audio systems, etc.

ORDERING INFORMATION

Part Number	Package
μPD780701YGC-×××-8BT	80-pin plastic QFP (14 × 14 mm)
μPD780702YGC-×××-8BT	80-pin plastic QFP (14 × 14 mm)

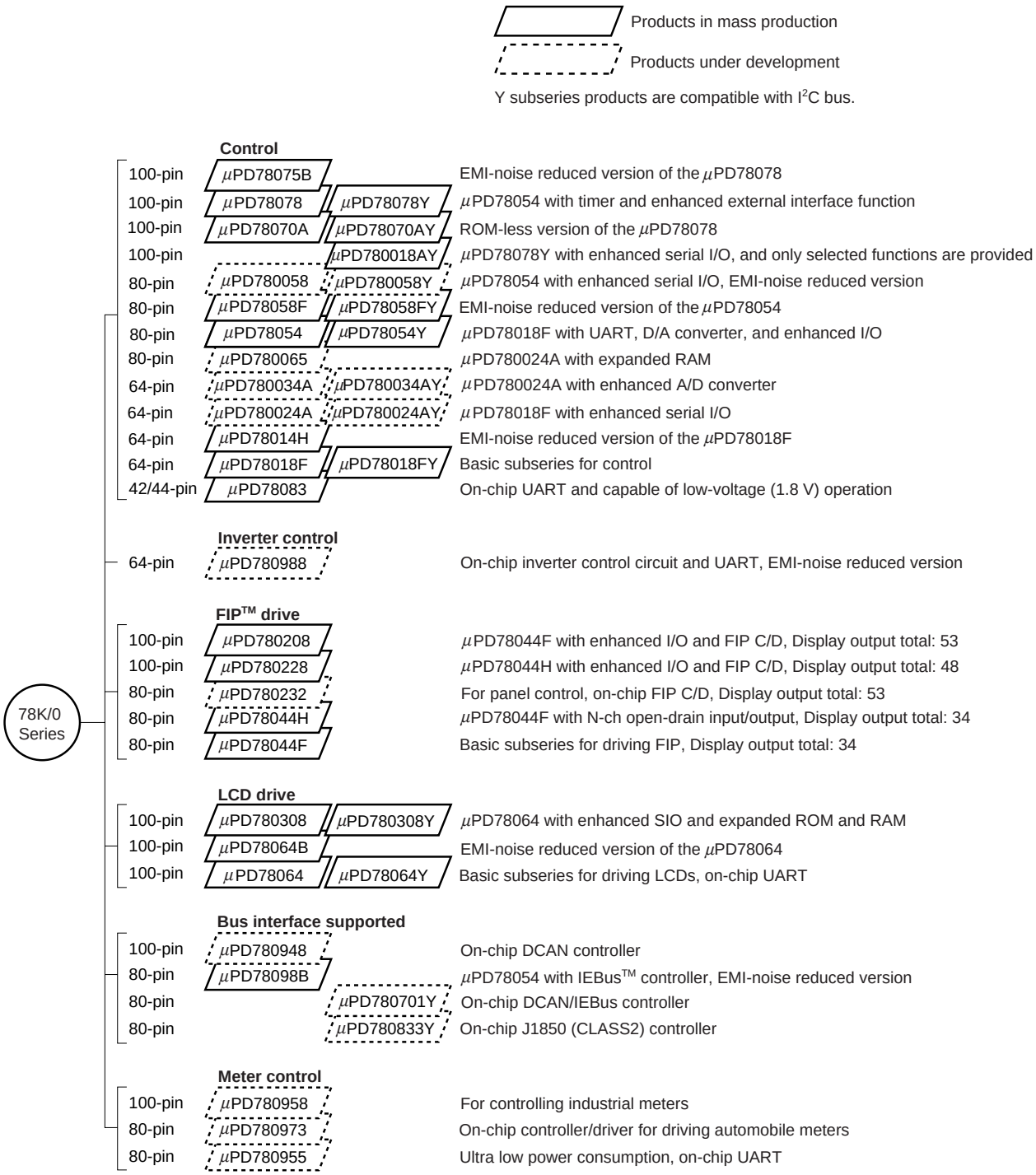
Remark ××× indicates ROM code suffix.

The information contained in this document is being issued in advance of the production cycle for the device. The parameters for the device may change before final production or NEC Corporation, at its own discretion, may withdraw the device prior to its production.

Document No. U13920EJ1V0PM00 (1st edition)
Date Published March 1999 N CP(K)
Printed in Japan

78K/0 SERIES LINEUP

The products in the 78K/0 Series are listed below. The names enclosed in boxes are subseries names.



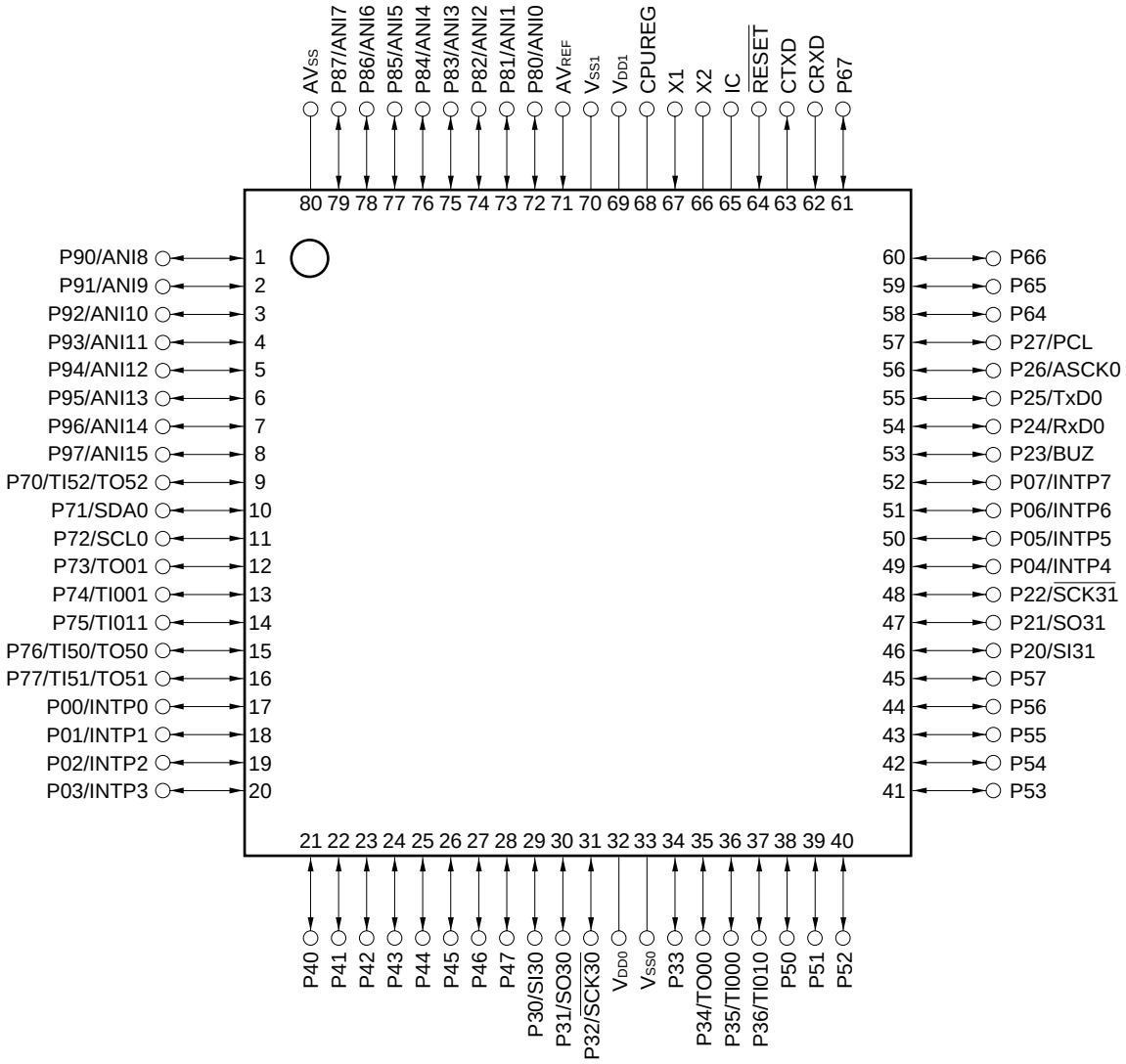
OVERVIEW OF FUNCTIONS

Item \ Part Number		μPD780701Y	μPD780702Y
Internal memory	ROM	60 Kbytes	
	High-speed RAM	1024 bytes	
	Expansion RAM	2048 bytes	
	Buffer RAM for DCAN	288 bytes	None
Minimum instruction execution time		On-chip minimum instruction execution time variable function • 0.32 μs/0.64 μs/1.27 μs/2.54 μs/5.09 μs (@ 6.29-MHz operation with system clock)	
General-purpose registers		8 bits × 32 registers (8 bits × 8 registers × 4 banks)	
Instruction set		• 16-bit operation • Multiply/divide (8 bits × 8 bits, 16 bits ÷ 8 bits) • Bit manipulation (set, reset, test, Boolean operation) • BCD adjust, etc.	
I/O ports		Total: 67 • CMOS I/O: 56 • TTL input/CMOS output: 8 • N-ch open-drain I/O: 3	
A/D converter		• 8-bit resolution × 16 channels • Power fail detection function	
Serial interface		• 3-wire serial I/O mode: 2 channels • UART mode: 1 channel • I^2C bus mode: 1 channel	
Timer		• 16-bit timer/event counter: 2 channels • 8-bit timer/event counter: 3 channels • Watch timer: 1 channel • Watchdog timer: 1 channel	
Timer output		5 (8-bit PWM output capable: 3)	
Clock output		49.2 kHz, 98.3 kHz, 197 kHz, 393 kHz, 786 kHz, 1.57 MHz, 3.15 MHz, 6.29 MHz (@ 6.29-MHz operation with system clock)	
Buzzer output		0.768 kHz, 1.54 kHz, 3.07 kHz, 6.14 kHz (@ 6.29-MHz operation with system clock)	
Bus controller		DCAN controller	IEBus controller
Vectored interrupt sources	Maskable	Internal: 20, External: 8	Internal: 19, External: 8
	Non-maskable	Internal: 1	
	Software	1	
Power supply voltage		V_{DD} = 3.5 to 5.5 V	
Operating ambient temperature		T_A = –40 to +85°C	
Package		80-pin plastic QFP (14 × 14 mm)	

PIN CONFIGURATION (Top View)

(1) μPD780701Y

- **80-pin plastic QFP (14 × 14 mm)**
  μPD780701YGC-×××-8BT



Cautions 1. Connect the IC (Internally Connected) pin directly to V_{SS0} or V_{SS1}.

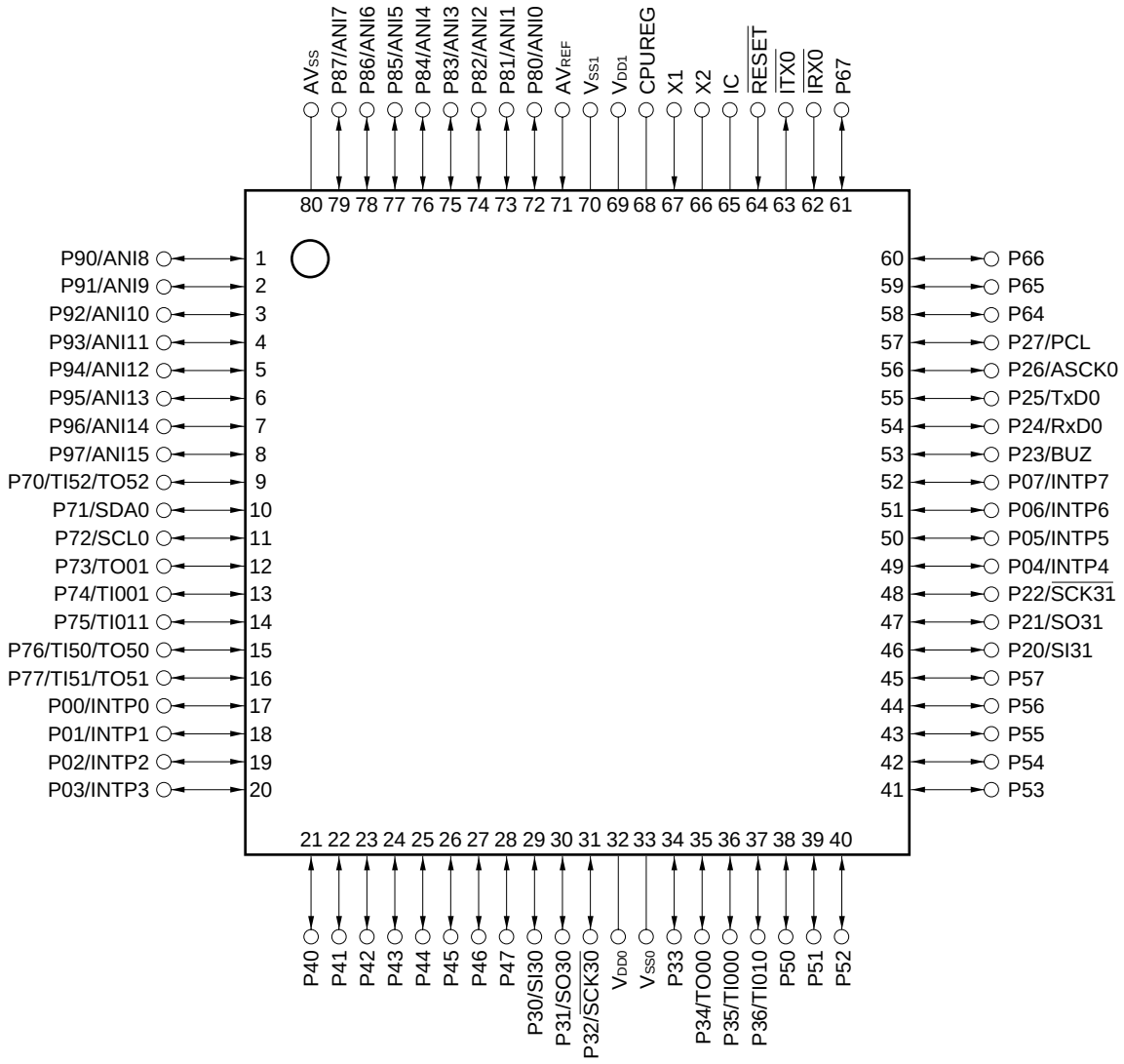
2. Connect the AV_{SS} pin to V_{SS0}.

3. Connect the AV_{REF} pin to V_{DD0}.

Remark When the μPD780701Y and 780702Y are used in applications where the noise generated inside the microcontroller needs to be reduced, the implementation of noise reduction measures, such as supplying voltage to V_{DD0} and V_{DD1} individually and connecting V_{SS0} and V_{SS1} to different ground lines, is recommended.

(2) μPD780702Y

- **80-pin plastic QFP (14 × 14 mm)**
  μPD780702YGC-×××-8BT



Cautions 1. Connect the IC (Internally Connected) pin directly to V_{SS0} or V_{SS1}.

2. Connect the AV_{SS} pin to V_{SS0}.

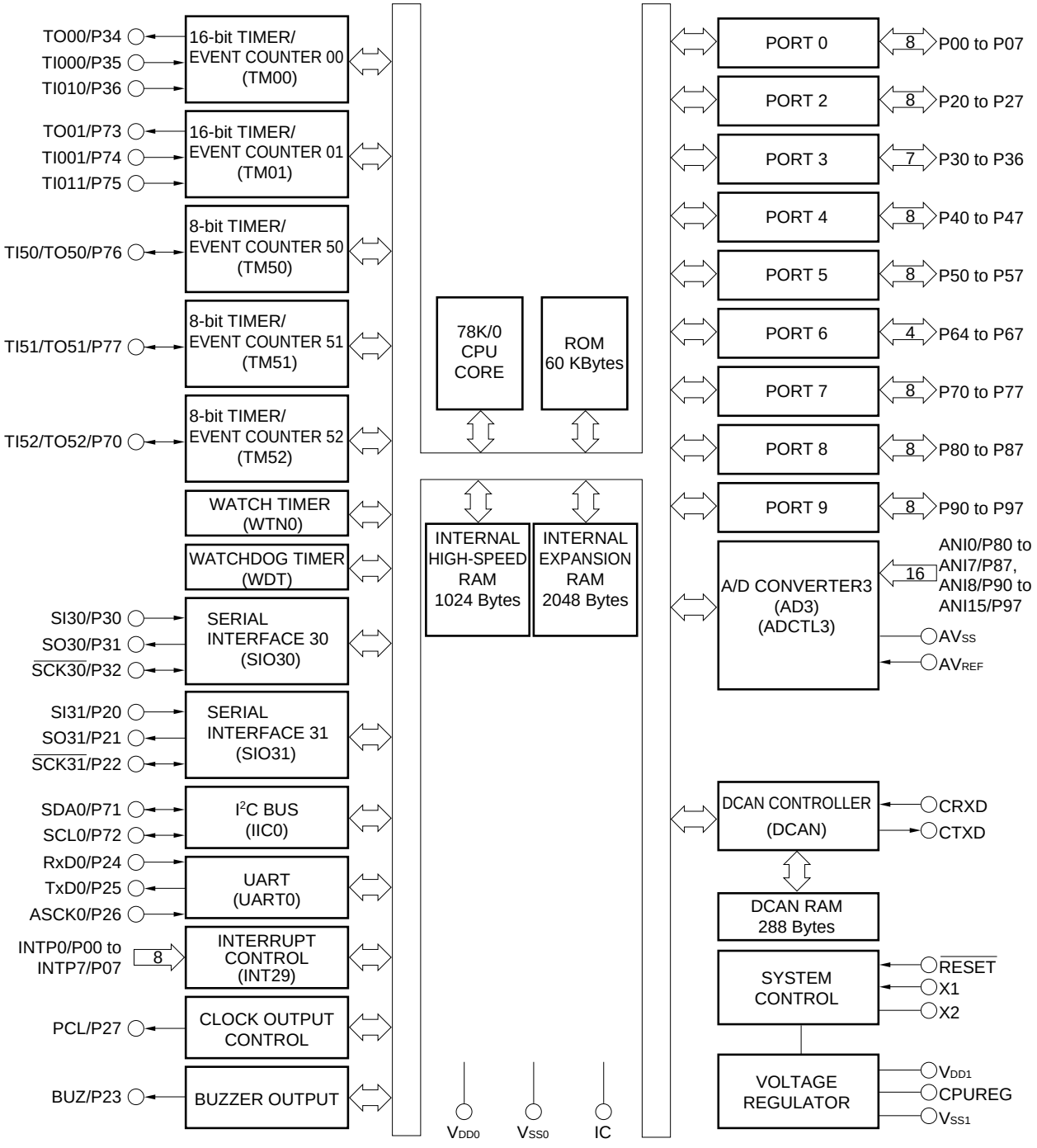
3. Connect the AV_{REF} pin to V_{DD0}.

Remark When the μPD780701Y and 780702Y are used in applications where the noise generated inside the microcontroller needs to be reduced, the implementation of noise reduction measures, such as supplying voltage to V_{DD0} and V_{DD1} individually and connecting V_{SS0} and V_{SS1} to different ground lines, is recommended.

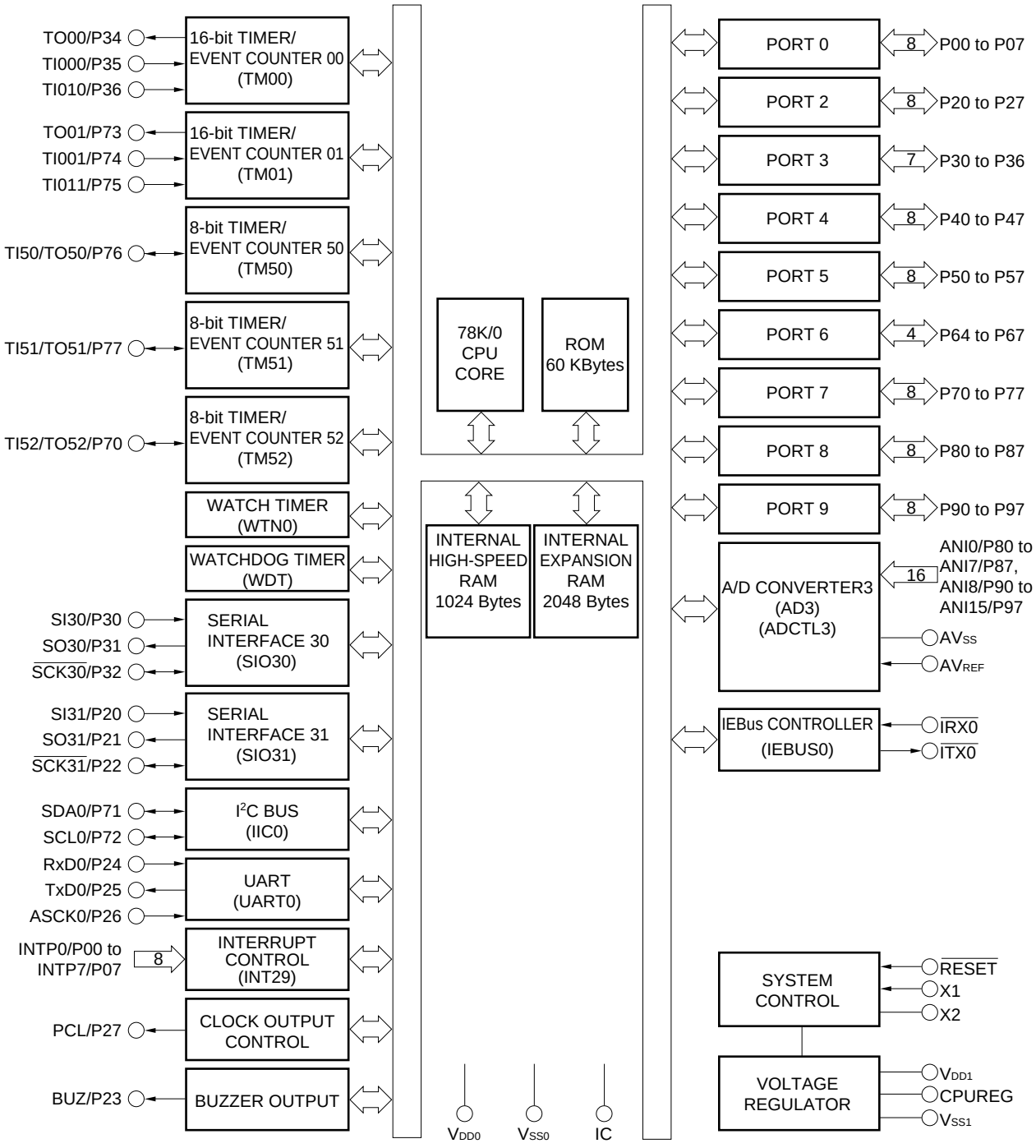
ANI0 to ANI15:	Analog Input
ASCK0:	Asynchronous Serial Clock
AV_{REF}:	Analog Reference Voltage
AV_{SS}:	Analog Ground
BUZ:	Buzzer Output
CPUREG:	Regulator for CPU Power Supply
CRXD:	CAN Receive Data
CTXD:	CAN Transmit Data
IC:	Internally Connected
INTP0 to INTP7:	Interrupt for Peripherals
$\overline{IRX0}$:	IEBus Receive Data
$\overline{ITX0}$:	IEBus Transmit Data
P00 to P07:	Port 0
P20 to P27:	Port 2
P30 to P36:	Port 3
P40 to P47:	Port 4
P50 to P57:	Port 5
P64 to P67:	Port 6
P70 to P77:	Port 7
P80 to P87:	Port 8
P90 to P97:	Port 9
PCL:	Programmable Clock
$\overline{RESET}$:	Reset
RxD0:	Receive Data (for UART0)
$\overline{SCK30}$, $\overline{SCK31}$:	Serial Clock (for SIO30, 31)
SCL0:	Serial Clock (for IIC0)
SDA0:	Serial Data
SI30, SI31:	Serial Input
SO30, SO31:	Serial Output
TI000, TI010, TI001, TI011, TI50, TI51, TI52:	Timer Input
TO00, TO01, TO50, TO51, TO52:	Timer Output
TxD0:	Transmit Data (for UART0)
V_{DD0}, V_{DD1}:	Power Supply
V_{SS0}, V_{SS1}:	Ground
X1, X2:	Crystal

BLOCK DIAGRAM

(1) μPD780701Y



(2) μPD780702Y



CONTENTS

1. DIFFERENCES BETWEEN μPD780701Y AND μPD780702Y

The essential difference between these two products is the on-chip bus controller.

The main differences between the μPD780701Y and μPD780702Y are outlined in Table 1-1.

Table 1-1. Differences between μPD780701Y and μPD780702Y

Item \ Part Number	μPD780701Y	μPD780702Y
On-chip bus controller	DCAN controller	IEBus controller
Buffer RAM for DCAN	288 bytes	None
RX Pin (Pin No.62)	CRXD	$\overline{\text{IRX0}}$
TX Pin (Pin No.63)	CTXD	$\overline{\text{ITX0}}$
Internal maskable interrupt	Total: 20 sources (3 sources via the DCAN controller)	Total: 19 sources (2 sources via the IEBus controller)

2. PIN FUNCTIONS

2.1 Port Pins (1/2)

Pin Name	I/O	Function		After Reset	Alternate Function
P00 to P07	Input/output	Port 0. 8-bit input/output port. Input/output can be specified in 1-bit units. An on-chip pull-up resistor can be specified by means of software.		Input	INTP0 to INTP7
P20	Input/output	Port 2. 8-bit input/output port. Input/output can be specified in 1-bit units. An on-chip pull-up resistor can be specified by means of software.		Input	SI31
P21					SO31
P22					$\overline{\text{SCK31}}$
P23					BUZ
P24					RxD0
P25					TxD0
P26					ASCK0
P27					PCL
P30	Input/output	Port 3. 7-bit input/output port. Input/output can be specified in 1-bit units.	An on-chip pull-up resistor can be specified by means of software.	Input	SI30
P31					SO30
P32					$\overline{\text{SCK30}}$
P33			N-ch open-drain input/output port (15-V withstand voltage). LEDs can be driven directly.		–
P34			An on-chip pull-up resistor can be specified by means of software.		TO00
P35					TI000
P36					TI010
P40 to P47	Input/output	Port 4. 8-bit input/output port. Input/output can be specified in 1-bit units. An on-chip pull-up resistor can be specified by means of software. Interrupt request flag KRIF is set to 1 by falling edge detection.		Input	–
P50 to P57	Input/output	Port 5. 8-bit input/output port. TTL level input/CMOS output. Input/output can be specified in 1-bit units. An on-chip pull-up resistor can be specified by means of software.		Input	–
P60 to P67	Input/output	Port 6. 4-bit input/output port. Input/output can be specified in 1-bit units. An on-chip pull-up resistor can be specified by means of software.		Input	–

2.1 Port Pins (2/2)

Pin Name	I/O	Function		After Reset	Alternate Function
P70	Input/output	Port 7. 8-bit input/output port. Input/output can be specified in 1-bit units.	An on-chip pull-up resistor can be specified by means of software.	Input	TI52/TO52
P71			N-ch open-drain input/output port (5-V withstand voltage).		SDA0
P72					SCL0
P73			An on-chip pull-up resistor can be specified by means of software.		TO01
P74					TI001
P75					TI011
P76					TI50/TO50
P77					TI51/TO51
P80 to P87	Input/output	Port 8. 8-bit input/output port. Input/output can be specified in 1-bit units.		Input	ANI0 to ANI7
P90 to P97	Input/output	Port 9. 8-bit input/output port. Input/output can be specified in 1-bit units.		Input	ANI8 to ANI15

2.2 Non-port Pins (1/2)

Pin Name	I/O	Function	After Reset	Alternate Function
INTP0 to INTP7	Input	External interrupt input for which the valid edge (rising edge, falling edge, or both rising and falling edges) can be specified	Input	P00 to P07
SI30	Input	Serial interface serial data input	Input	P30
SI31				P20
SO30	Output	Serial interface serial data output	Input	P31
SO31				P21
SDA0	I/O	Serial interface serial data input/output	Input	P71
$\overline{SCK30}$	I/O	Serial interface serial clock input/output	Input	P32
$\overline{SCK31}$				P22
SCL0				P72
RxD0	Input	Serial data input for asynchronous serial interface	Input	P24
TxD0	Output	Serial data output for asynchronous serial interface	Input	P25
ASCK0	Input	Serial clock input for asynchronous serial interface	Input	P26
CRXD[Note 1]	Input	Data input of DCAN controller (DCAN)	Input	–
CTXD[Note 1]	Output	Data output of DCAN controller (DCAN)	Output	–
$\overline{IRX0}$[Note 2]	Input	Data input of IEBus controller (IEBUS0)	Input	–
$\overline{ITX0}$[Note 2]	Output	Data output of IEBus controller (IEBUS0)	Output	–
TI000	Input	External count clock input to 16-bit timer (TM00)	Input	P35
TI010		External count clock input to 16-bit timer (TM00)		P36
TI001		External count clock input to 16-bit timer (TM01)		P74
TI011		External count clock input to 16-bit timer (TM01)		P75
TI50		External count clock input to 8-bit timer (TM50)		P76/TO50
TI51		External count clock input to 8-bit timer (TM51)		P77/TO51
TI52		External count clock input to 8-bit timer (TM52)		P70/TO52
TO00	Output	16-bit timer (TM00) output	Input	P34
TO01		16-bit timer (TM01) output		P73
TO50		8-bit timer (TM50) output		P76/TI50
TO51		8-bit timer (TM51) output		P77/TI51
TO52		8-bit timer (TM52) output		P70/TI52
PCL	Output	Clock output	Input	P27
BUZ	Output	Buzzer output	Input	P23
ANI0 to ANI7	Input	A/D converter (AD3) analog input	Input	P80 to P87
ANI8 to ANI15				P90 to P97
AV_{REF}	Input	A/D converter (AD3) reference voltage and analog power supply	–	–
AV_{SS}	–	A/D converter (AD3) ground potential	–	–
X1	Input	Connecting crystal resonator for system clock oscillation	–	–
X2	–		–	–

Notes 1. μPD780701Y only

2. μPD780702Y only

2.2 Non-port Pins (2/2)

Pin Name	I/O	Function	After Reset	Alternate Function
$\overline{\text{RESET}}$	Input	System reset input	Input	–
CPUREG	–	Regulator for CPU power supply. Connect to V_{SS0} or V_{SS1} via a 0.1-μF capacitor.	–	–
V_{DD0}	–	Positive power supply for ports	–	–
V_{DD1}	–	Positive power supply (except ports and analog section)	–	–
V_{SS0}	–	Ground potential for ports	–	–
V_{SS1}	–	Ground potential (except ports and analog section)	–	–
IC	–	Internally connected. Connect directly to V_{SS0} or V_{SS1}.	–	–

2.3 Pin I/O Circuits and Recommended Connection of Unused Pins

The input/output circuit type of each pin and recommended connection of unused pins are shown in Table 2-1. For the input/output circuit configuration of each type, refer to Figure 2-1.

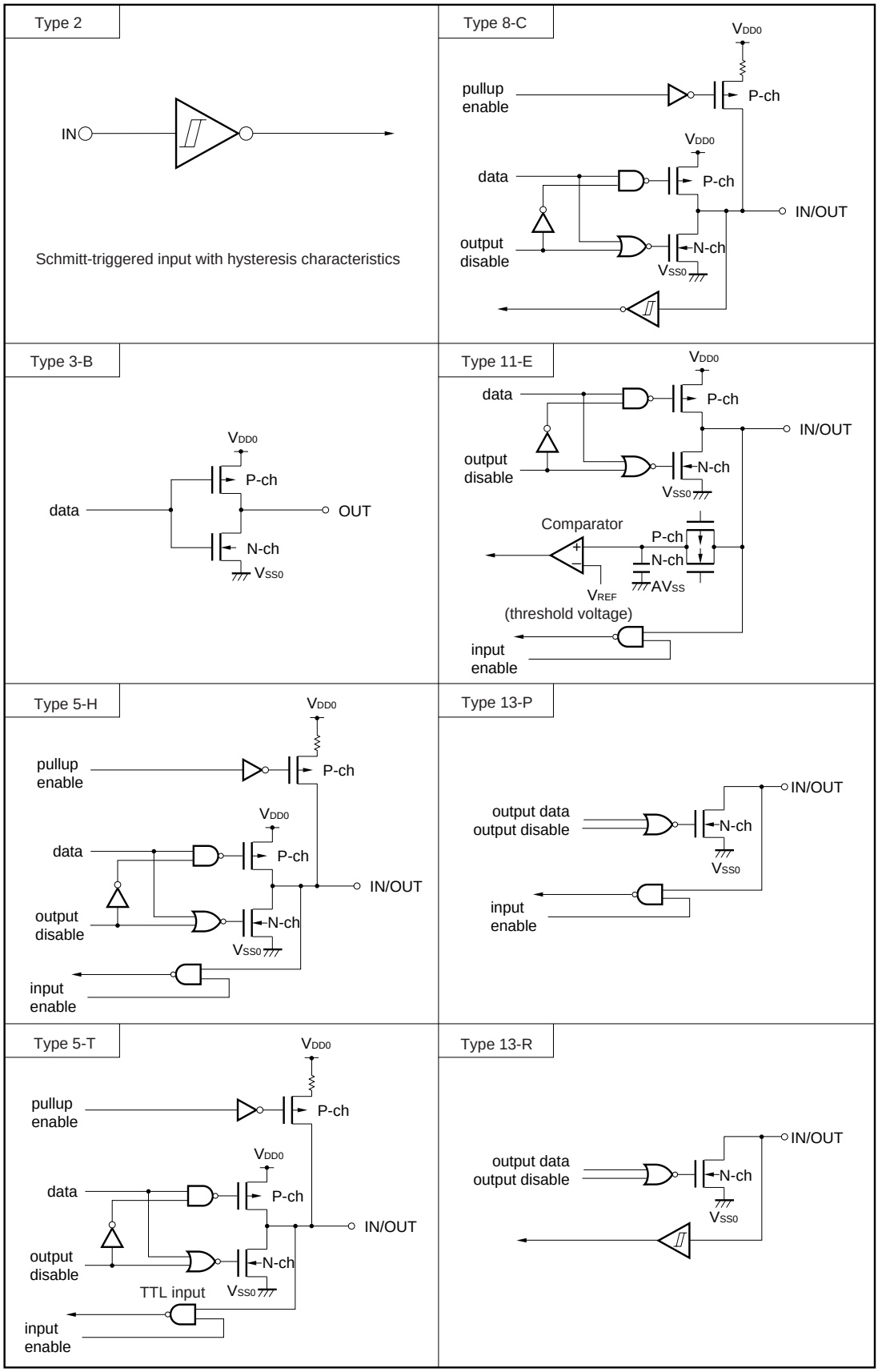
Table 2-1. Types of Pin Input/Output Circuits

Pin Name	Input/Output Circuit Type	I/O	Recommended Connection of Unused Pins
P00/INTP0 to P07/INTP7	8-C	Input/output	Independently connect to V_{SS0} via a resistor.
P20/SI31			Independently connect to V_{DD0} or V_{SS0} via a resistor.
P21/SO31	5-H		
P22/$\overline{SCK31}$	8-C		
P23/BUZ	5-H		
P24/RxD0	8-C		
P25/TxD0	5-H		
P26/ASCK0	8-C		
P27/PCL	5-H		
P30/SI30	8-C		
P31/SO30	5-H		
P32/$\overline{SCK30}$	8-C		
P33	13-P		Connect to V_{DD0} via a resistor.
P34/TO00	5-H		Independently connect to V_{DD0} or V_{SS0} via a resistor.
P35/TI000	8-C		
P36/TI010			
P40 to P47	5-H		Independently connect to V_{DD0} via a resistor.
P50 to P57	5-T		Independently connect to V_{DD0} or V_{SS0} via a resistor.
P64 to P67	5-H		
P70/TI52/TO52			
P71/SDA0	13-R		Independently connect to V_{DD0} via a resistor.
P72/SCL0			
P73/TO01	5-H		Independently connect to V_{DD0} or V_{SS0} via a resistor.
P74/TI001	8-C		
P75/TI011			
P76/TI50/TO50			
P77/TI51/TO51			
P80/ANI0 to P87/ANI7	11-E		
P90/ANI8 to P97/ANI15			
CRXD[Note 1]	2	Input	Connect to V_{DD0} or V_{SS0} via a resistor.
CTXD[Note 1]	3-B	Output	Leave open.
$\overline{IRX0}$[Note 2]	2	Input	Connect to V_{DD0} or V_{SS0} via a resistor.
$\overline{ITX0}$[Note 2]	3-B	Output	Leave open.
$\overline{RESET}$	2	Input	–
AV_{REF}	–		Connect to V_{DD0}.
AV_{SS}		–	Connect to V_{SS0}.
IC			Connect directly to V_{SS0} or V_{SS1}.

Notes 1. μPD780701Y only

2. μPD780702Y only

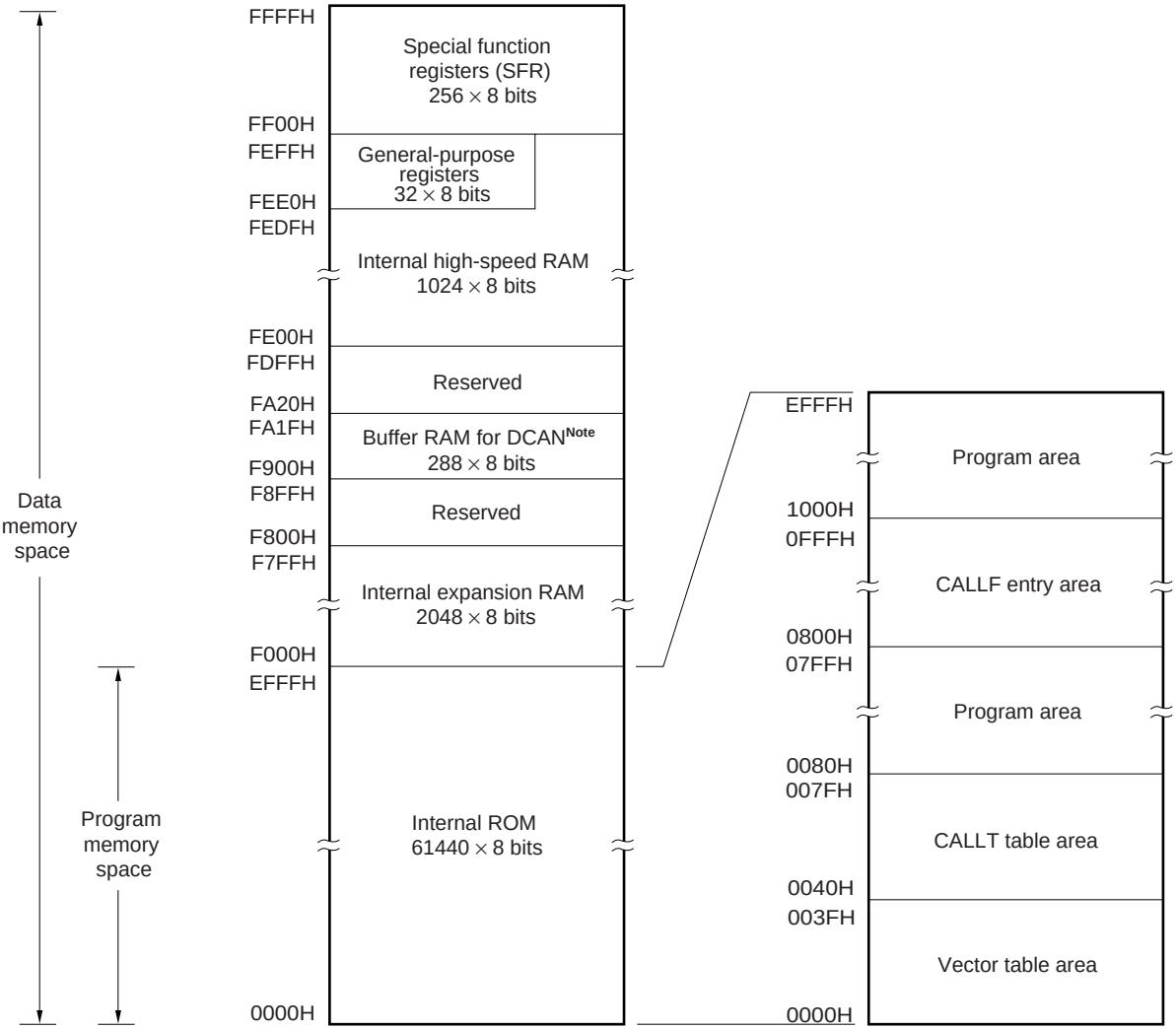
Figure 2-1. Pin Input/Output Circuits



3. MEMORY SPACE

Figure 3-1 shows the memory map of the μPD780701Y and 780702Y.

Figure 3-1. Memory Map



Note Buffer RAM for DCAN is incorporated only in the μPD780701Y. It is reserved area in the μPD780702Y.

4. PERIPHERAL HARDWARE FUNCTION FEATURES

4.1 Ports

The following three types of I/O ports are available.

- CMOS input/output (Ports 0, 2 to 4, 7 to 9 (except P33, P71, P72)): 56
- TTL input/CMOS output (Port 5): 8
- N-ch open-drain input/output (P33, P71, P72): 3

Total: 67

Table 4-1. Port Functions

Port Name	Pin Name	Function
Port 0	P00 to P07	Input/output port. Input/output can be specified in 1-bit units. An on-chip pull-up resistor can be specified by means of software.
Port 2	P20 to P27	Input/output port. Input/output can be specified in 1-bit units. An on-chip pull-up resistor can be specified by means of software.
Port 3	P30 to P32, P34 to P36	Input/output port. Input/output can be specified in 1-bit units. An on-chip pull-up resistor can be specified by means of software.
	P33	N-ch open-drain input/output port. Input/output can be specified in 1-bit units. LEDs can be driven directly.
Port 4	P40 to P47	Input/output port. Input/output can be specified in 1-bit units. An on-chip pull-up resistor can be specified by means of software. Interrupt request flag KRIF is set to 1 by falling edge detection.
Port 5	P50 to P57	TTL input/CMOS output port. Input/output can be specified in 1-bit units. An on-chip pull-up resistor can be specified by means of software.
Port 6	P64 to P67	Input/output port. Input/output can be specified in 1-bit units. An on-chip pull-up resistor can be specified by means of software.
Port 7	P70, P73 to P77	Input/output port. Input/output can be specified in 1-bit units. An on-chip pull-up resistor can be specified by means of software.
	P71, P72	N-ch open-drain input/output port. Input/output can be specified in 1-bit units.
Port 8	P80 to P87	Input/output port. Input/output can be specified in 1-bit units.
Port 9	P90 to P97	Input/output port. Input/output can be specified in 1-bit units.

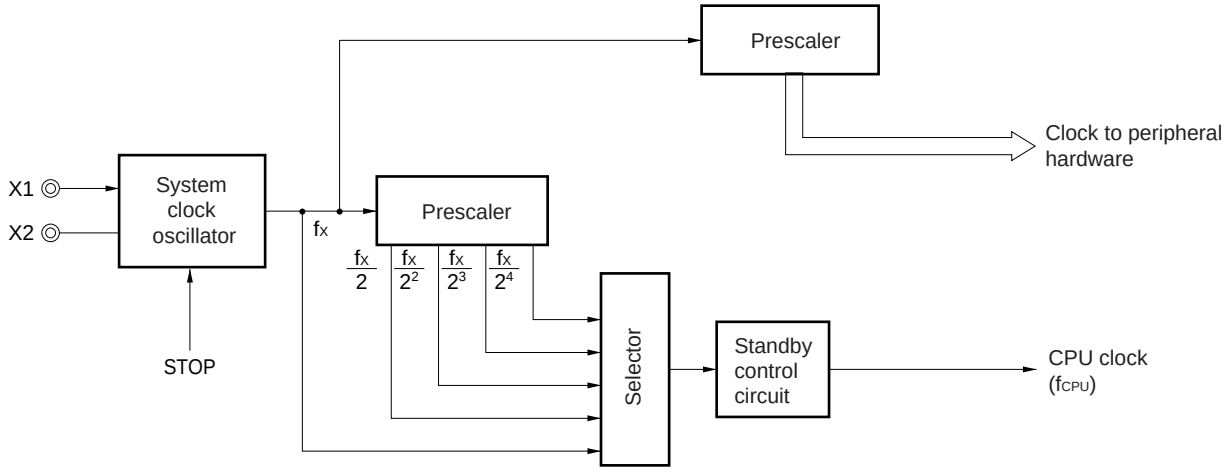
4.2 Clock Generator

A system clock generator is incorporated.

The minimum instruction execution time can be changed.

- 0.32 μs/0.64 μs/1.27 μs/2.54 μs/5.09 μs (@ 6.29-MHz operation with system clock)

Figure 4-1. Clock Generator Block Diagram



4.3 Timer/Counter

Seven timer/counter channels are incorporated.

- 16-bit timer/event counter: 2 channels
- 8-bit timer/event counter: 3 channels
- Watch timer: 1 channel
- Watchdog timer: 1 channel

Table 4-2. Operations of Timer/Event Counters

		16-bit timer/event counters TM00, TM01	8-bit timer/event counters TM50, TM51, TM52	Watch timer	Watchdog timer
Operation mode	Interval timer	2 channels	3 channels	1 channel[Note 1]	1 channel[Note 2]
	External event counter	2 channels	3 channels	–	–
Function	Timer output	2 outputs	3 outputs	–	–
	PWM output	–	3 outputs	–	–
	PPG output	2 outputs	–	–	–
	Pulse width measurement	4 inputs	–	–	–
	Square wave output	2 outputs	3 outputs	–	–
	One-shot pulse output	2 outputs	–	–	–
	Interrupt source	4	3	2	1

Notes 1. The watch timer can perform both watch timer and interval timer functions at the same time.

2. The watchdog timer has the watchdog timer and interval timer functions. However, use the watchdog timer by selecting either the watchdog timer function or the interval timer function.

Figure 4-2. Block Diagram of 16-Bit Timer/Event Counter TM00

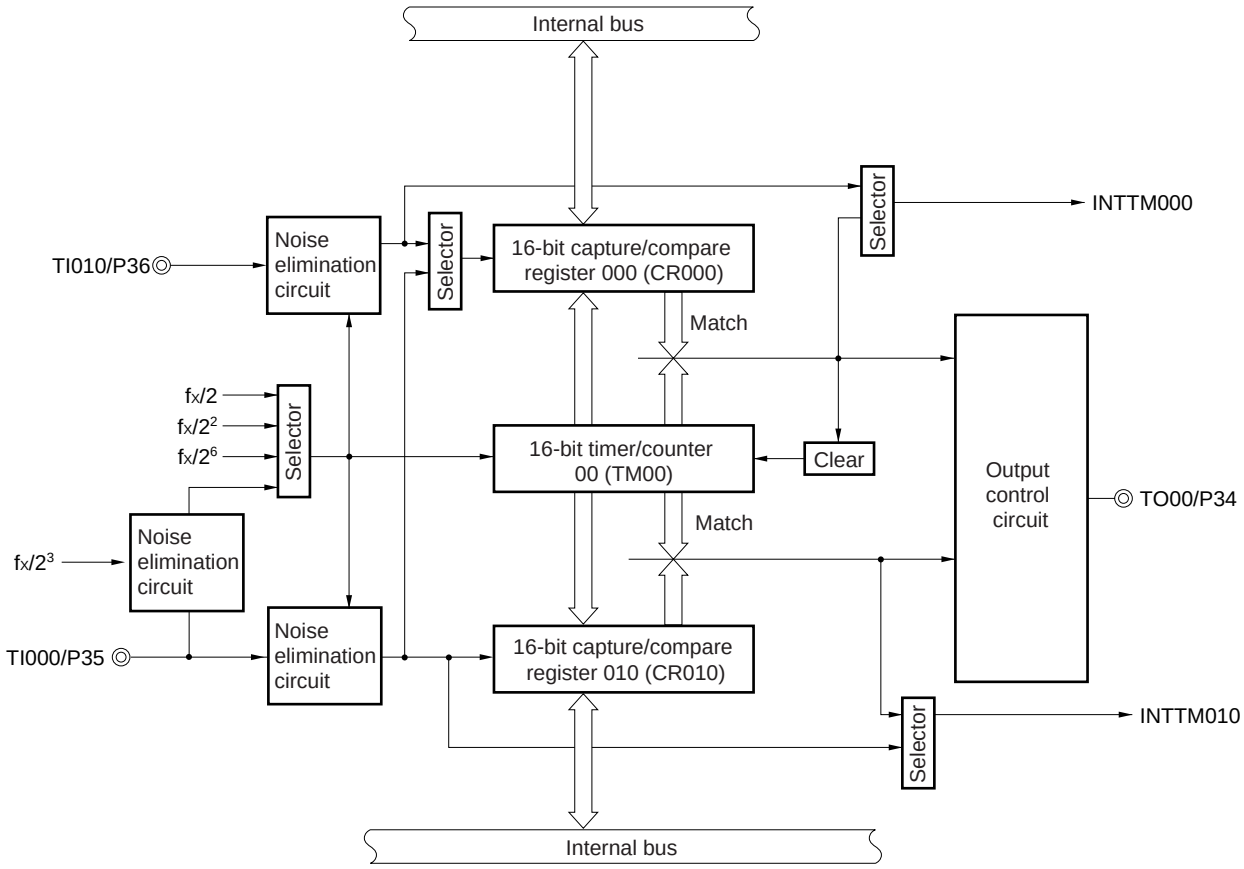


Figure 4-3. Block Diagram of 16-Bit Timer/Event Counter TM01

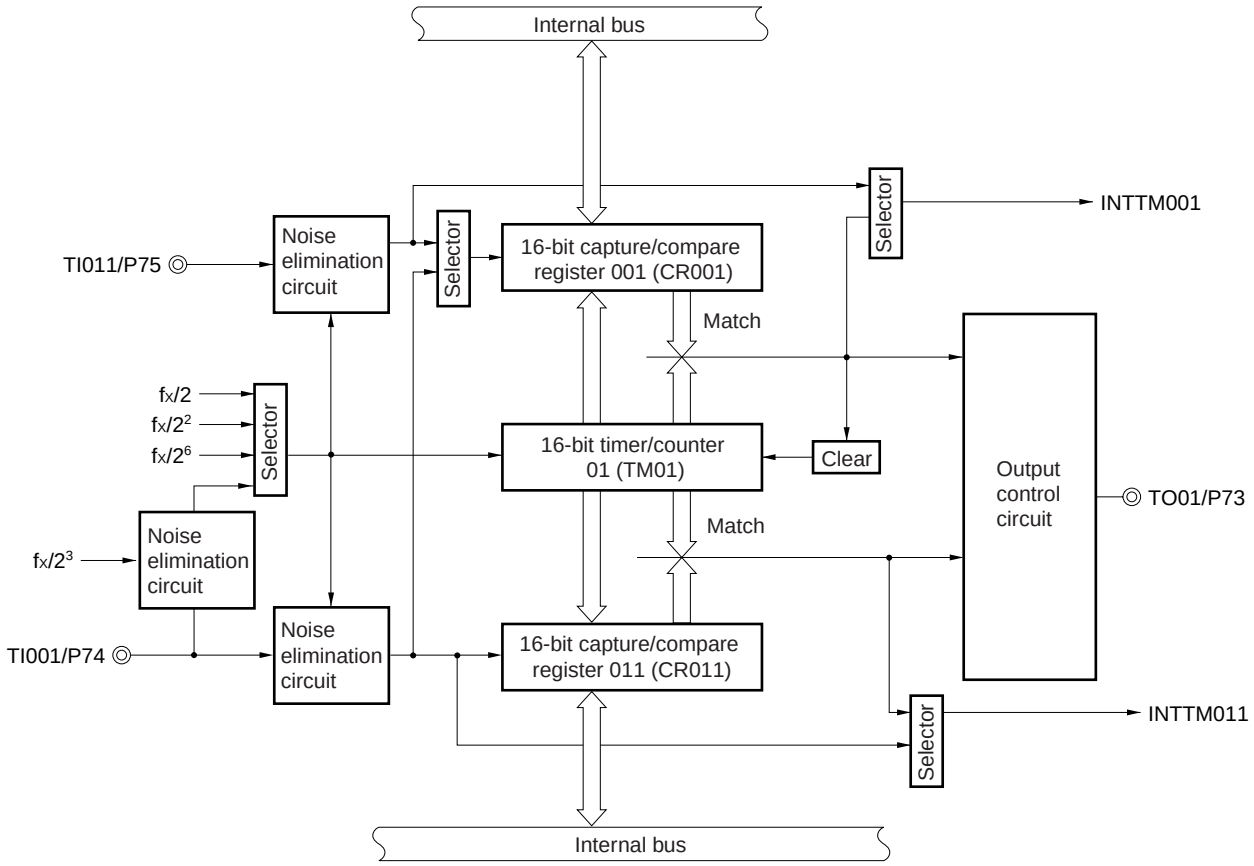


Figure 4-4. Block Diagram of 8-Bit Timer/Event Counter TM50

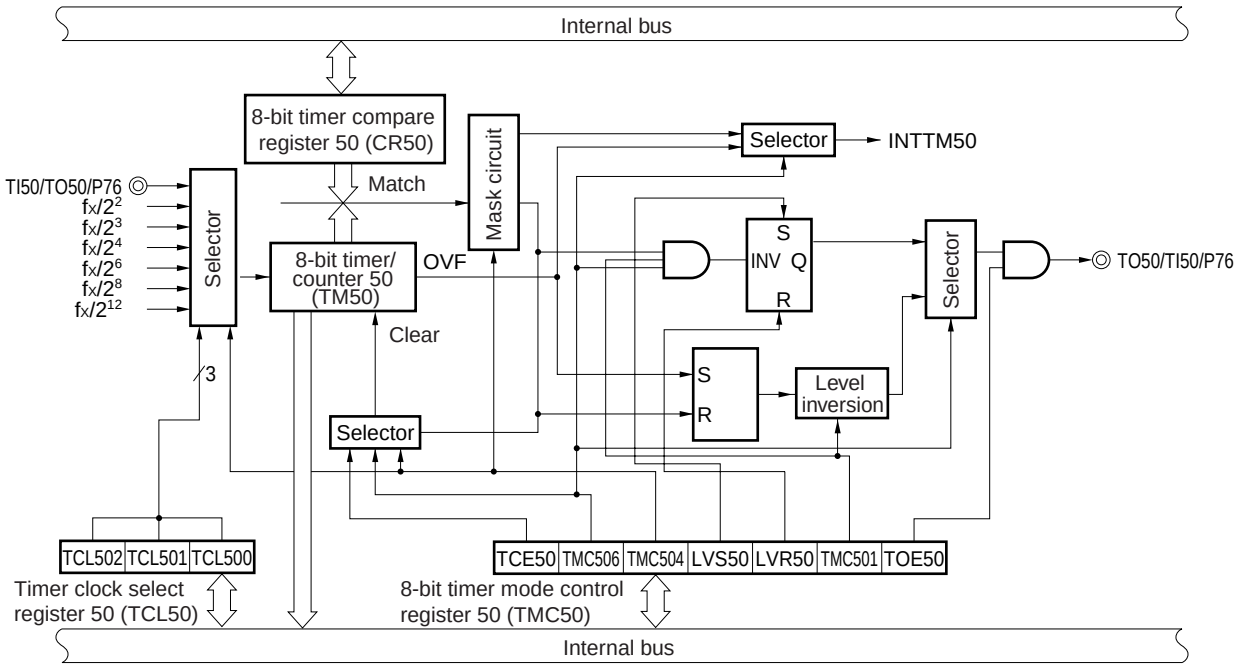


Figure 4-5. Block Diagram of 8-Bit Timer/Event Counter TM51

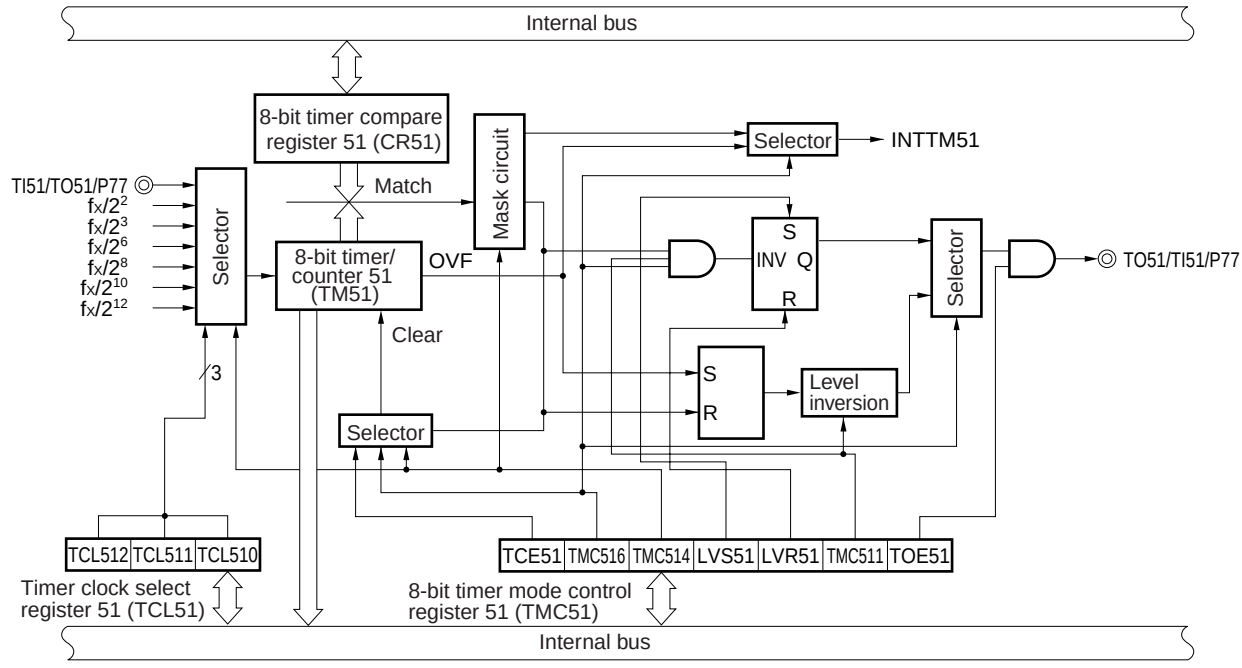


Figure 4-6. Block Diagram of 8-Bit Timer/Event Counter TM52

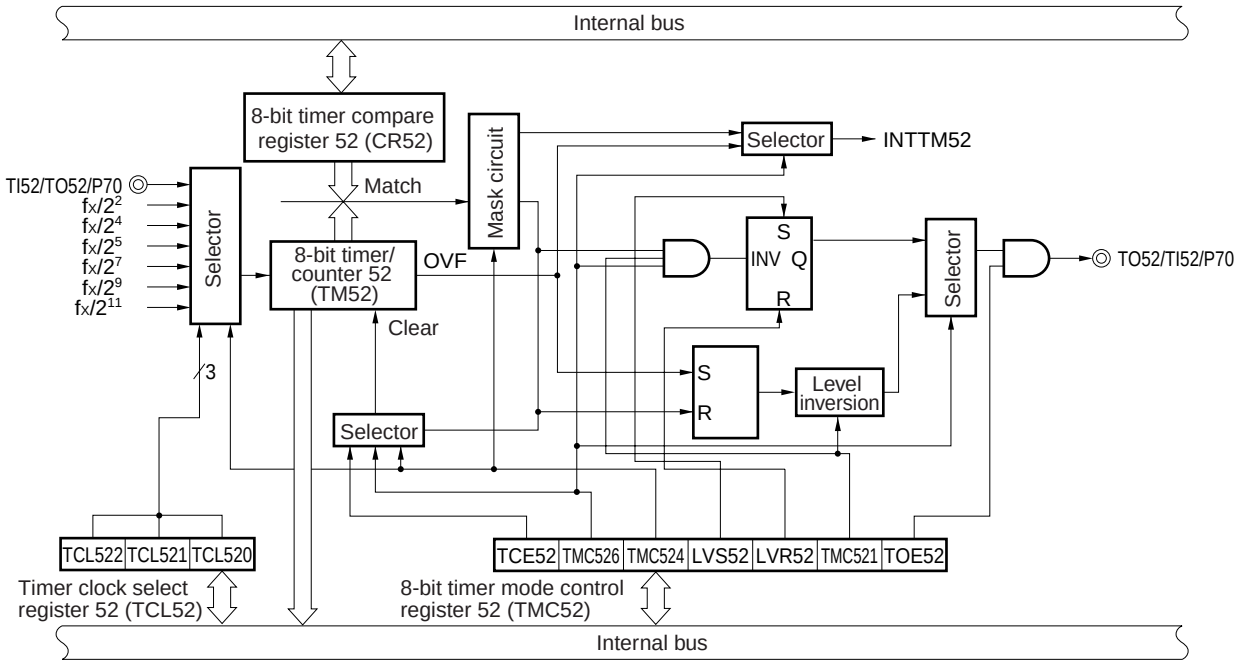
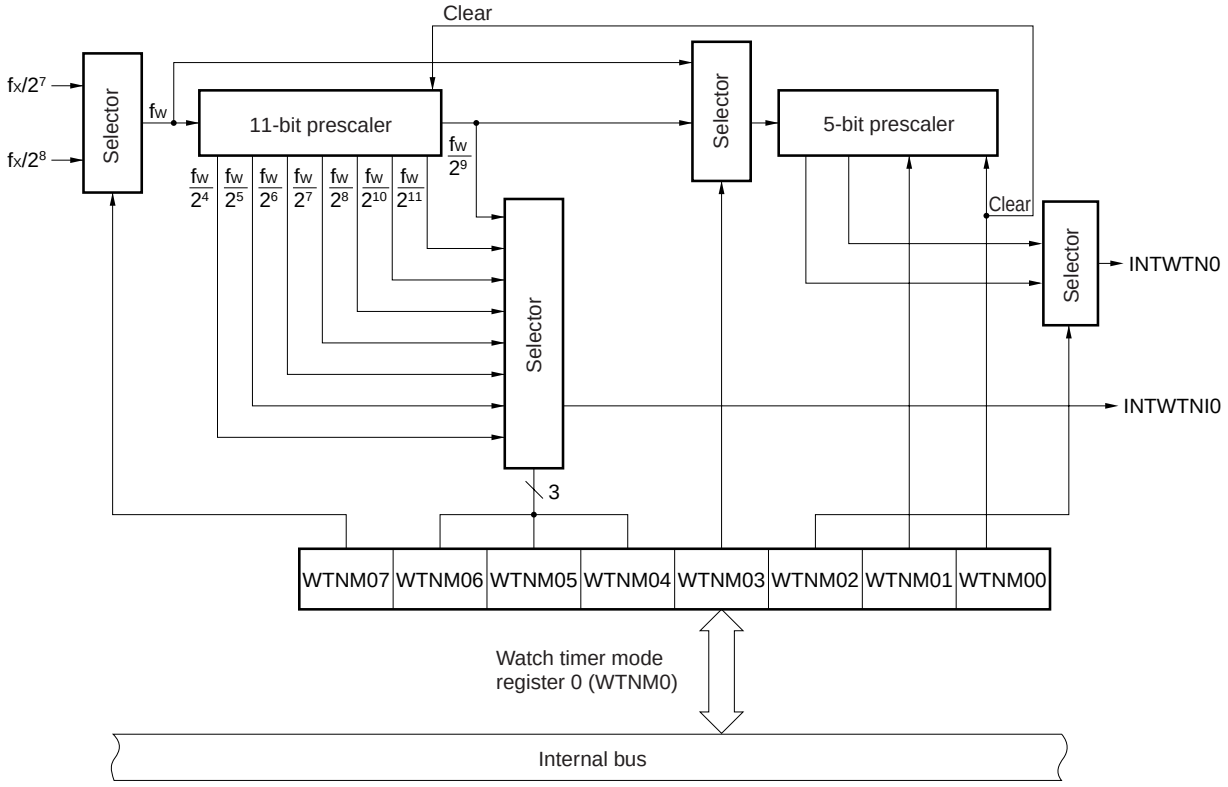
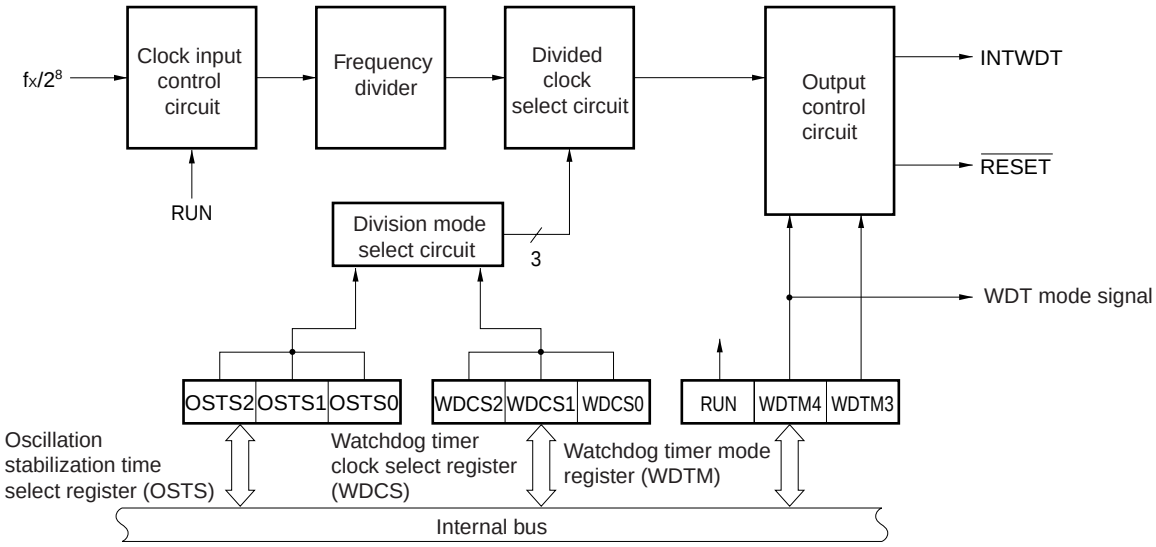


Figure 4-7. Watch Timer Block Diagram



Remark fx: System clock oscillation frequency
fw: Watch timer clock frequency

Figure 4-8. Watchdog Timer Block Diagram



4.4 Clock Output/Buzzer Output Control Circuit

A clock output/buzzer output control circuit (CKU) is incorporated.

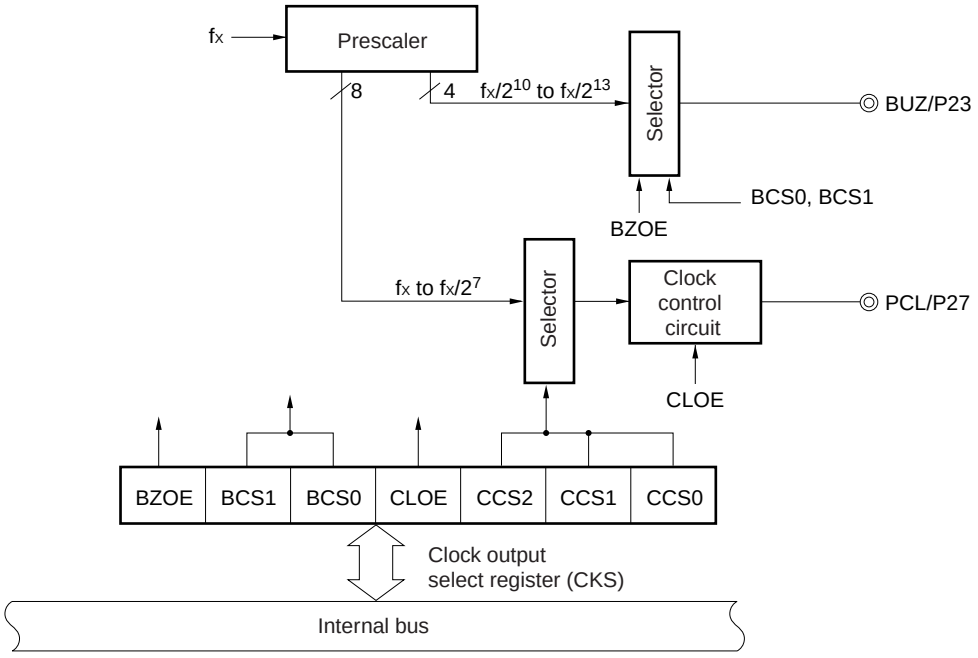
Clocks with the following frequencies can be output as clock output.

- 49.2 kHz/98.3 kHz/197 kHz/393 kHz/786 kHz/1.57 MHz/3.15 MHz/6.29 MHz (@ 6.29-MHz operation with system clock)

Clocks with the following frequencies can be output as buzzer output.

- 768 Hz/1.54 kHz/3.07 kHz/6.14 kHz (@ 6.29-MHz operation with system clock)

Figure 4-9. Block Diagram of Clock Output/Buzzer Output Control Circuit CKU



4.5 A/D Converter

An A/D converter consisting of sixteen 8-bit resolution channels is incorporated.

The A/D converter has the following two functions.

- 8-bit resolution A/D conversion
- Power fail detection function

Figure 4-10. A/D Converter Block Diagram

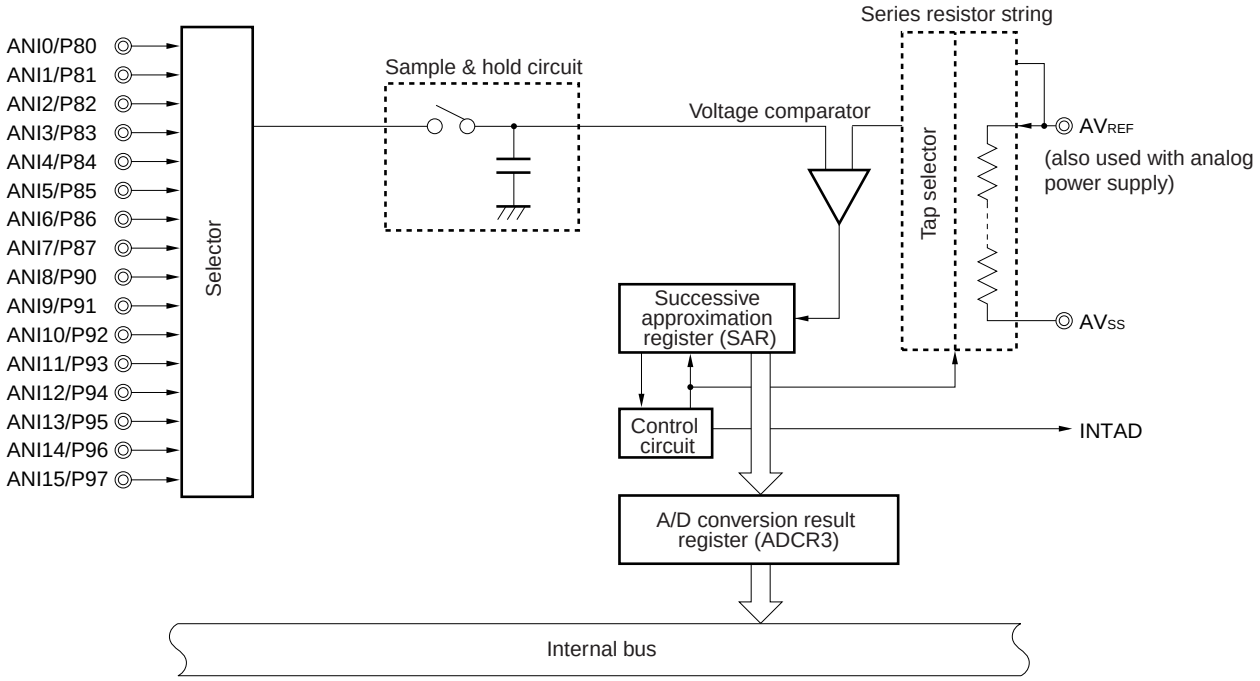
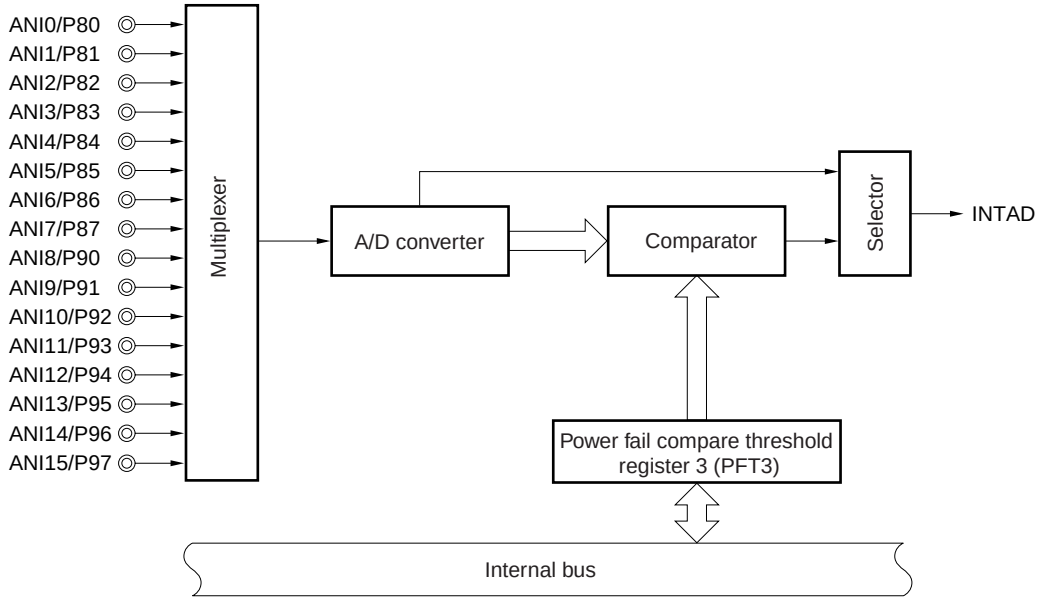


Figure 4-11. Block Diagram of Power Fail Detection Function



4.6 Serial Interfaces

Four serial interface channels are incorporated.

- Serial interface UART0
- Serial interfaces SIO30, SIO31
- Serial interface IIC0

(1) Serial interface UART0

The serial interface UART0 has the asynchronous serial interface (UART) mode.

- **Asynchronous serial interface (UART) mode**

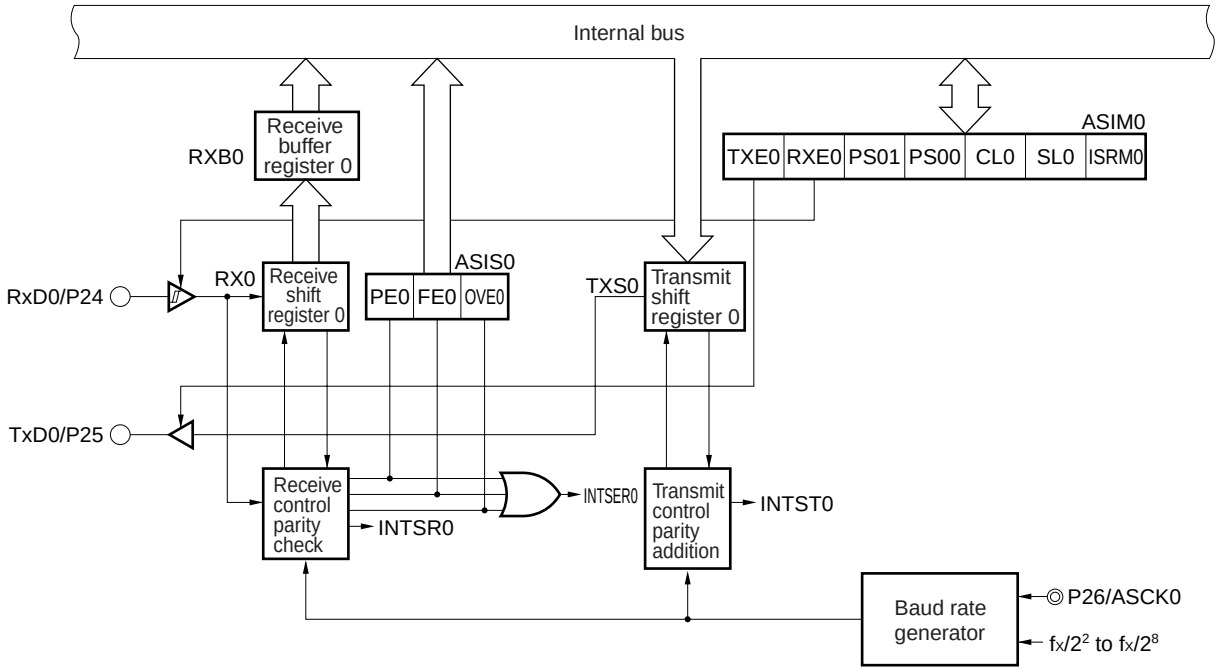
  This mode enables full-duplex operation wherein one byte of data is transmitted and received after the start bit.

  The on-chip dedicated UART baud rate generator enables communication using a wide range of selectable baud rates.

  In addition, a baud rate can also be defined by dividing the clock input to the ASCK0 pin.

  The dedicated UART baud rate generator can also be used to generate a MIDI-standard baud rate (31.25 kbps).

Figure 4-12. Block Diagram of Serial Interface UART0



(2) Serial interfaces SIO30, SIO31

The serial interfaces SIO30 and SIO31 have the 3-wire serial I/O mode.

- **3-wire serial I/O mode (fixed as MSB first)**

  This is an 8-bit data transfer mode using three lines: serial clock line ($\overline{\text{SCK3n}}$), serial output line (SO3n), and serial input line (SI3n).

  Since simultaneous transmit and receive operations are available in the 3-wire serial I/O mode, the processing time for data transfer is reduced.

  The first bit in 8-bit data in the serial transfer is fixed as MSB.

  The 3-wire serial I/O mode is useful for connection to a peripheral I/O device that includes a clocked serial interface, a display controller, etc.

Remark n = 0, 1

Figure 4-13. Block Diagram of Serial Interface SIO30

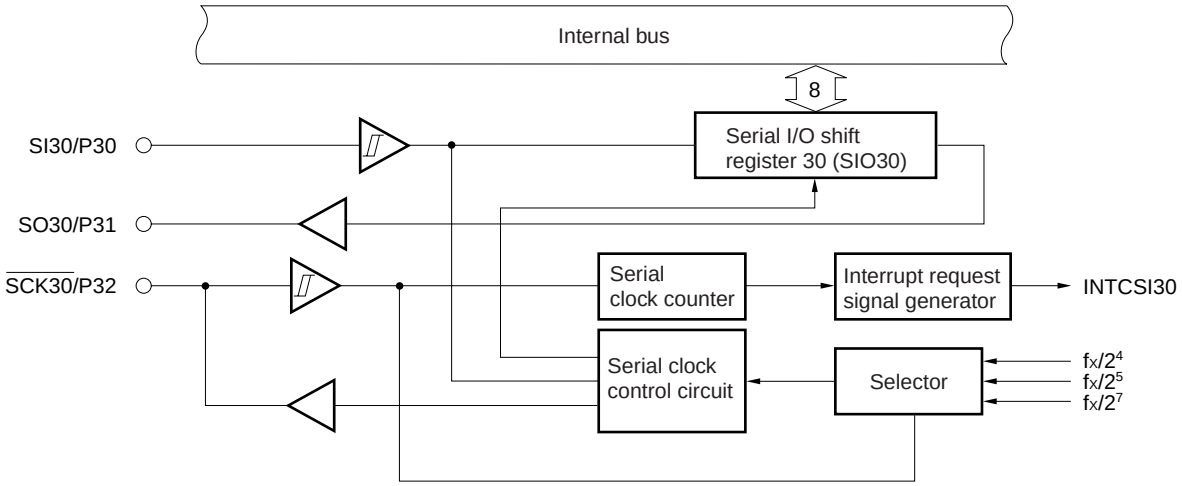
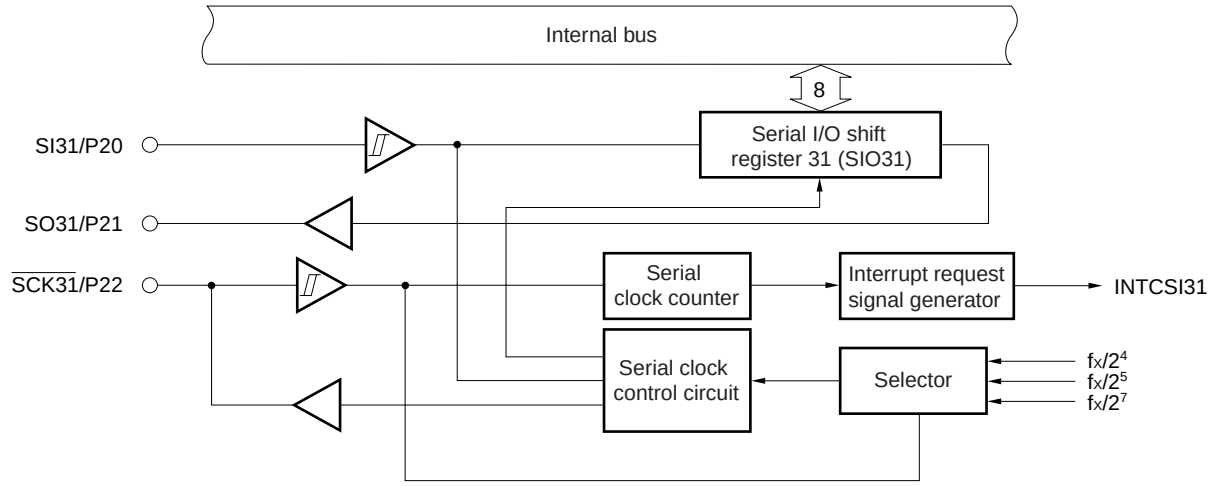


Figure 4-14. Block Diagram of Serial Interface SIO31



(3) Serial interface IIC0

The serial interface IIC0 has the I^2C (Inter IC) bus mode (multimaster supported).

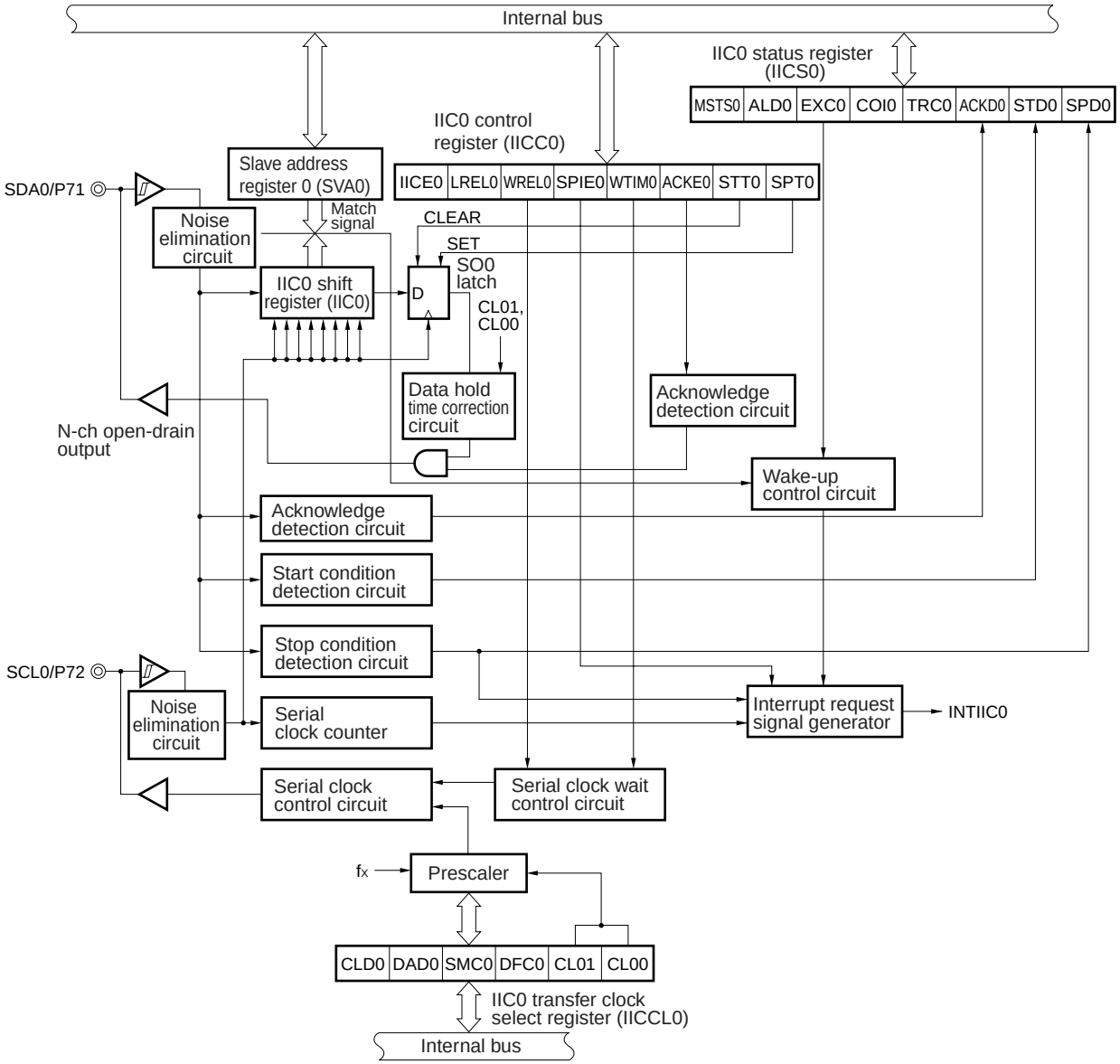
- **I^2C bus mode (multimaster supported)**

  This is an 8-bit data transfer mode between multiple devices using two lines: serial clock line (SCL0) and serial data bus line (SDA0).

  This mode complies with the I^2C bus format, and can output “start condition”, “data”, and “stop condition” during transmission via the serial data bus. These data are automatically detected by hardware during reception.

  Since the SCL0 and SDA0 are open-drain outputs in IIC0, pull-up resistors for the serial clock line and the serial data bus line are required.

Figure 4-15. Block Diagram of Serial Interface IIC0



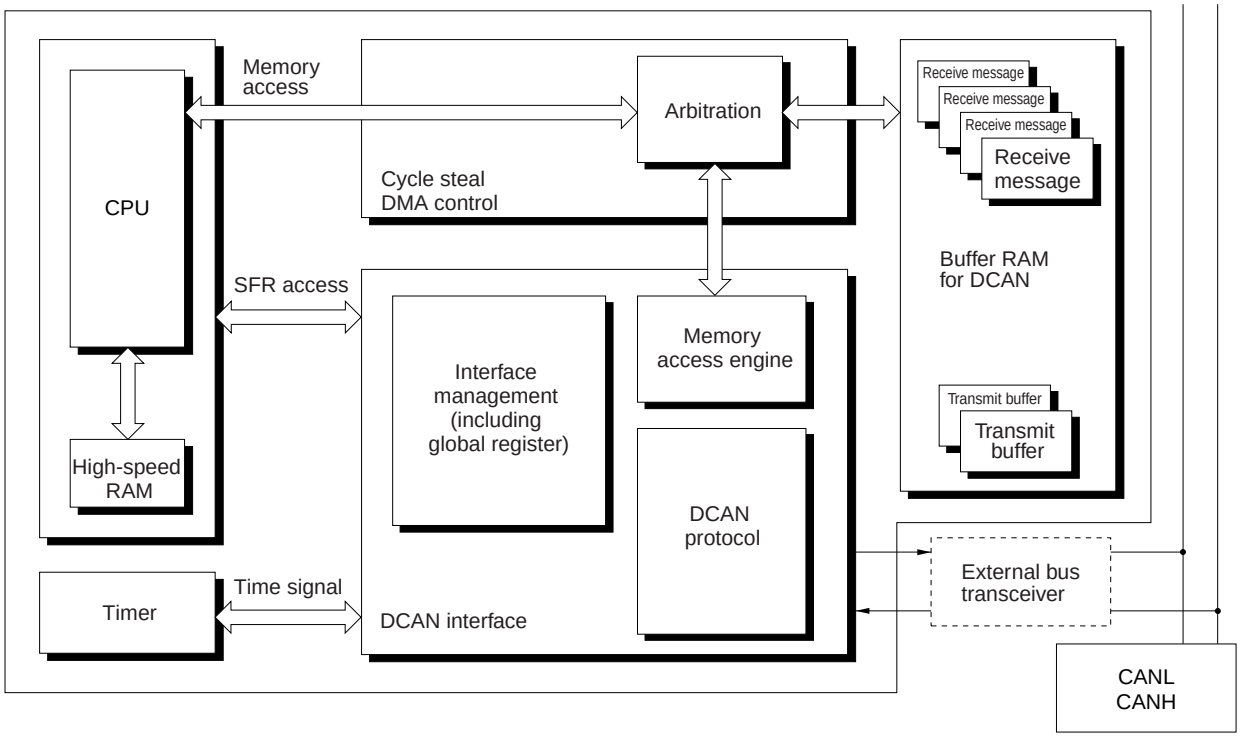
4.7 DCAN Controller (μPD780701Y only)

The μPD780701Y incorporates a DCAN (Direct storage Control Area Network) controller.

Table 4-3. DCAN Controller Functional Outline

Function	Details
Protocol	CAN2.0-supported extended frame format (Bosch specification 2.0 part B)
Baud rate	Maximum of 390 kbps (@ 6.29 MHz)
Bus line control	CMOS I/O for external transceiver
Clock	Selectable by register
Data storage	Capacity of buffer RAM for DCAN: 288 bytes (if not using for DCAN, it can be used for normal RAM)
Message configuration	Messages received via a message identifier are stored in RAM. Transmit message buffers: 2
Message number	Maximum of 16 receive messages, including 2 masks Transmit channels: 2 channels
Message sorting	Can set a separate identifier for the 16 receive messages Mask identifiers: 2 Can set a global mask for all messages
Interrupts	Transmit interrupt request: 1 Receive interrupt request: 1 Error interrupt request: 1
Time function	A time stamp function is available
Other functions	A separate transmit/receive error counter is available A flag for checking the bus connection is available A dedicated receive mode is available (use when detecting the baud rate on the bus)
Low power consumption mode	Sleep mode (can be woken up by the DCAN bus) Stop mode (cannot be woken up by the DCAN bus)

Figure 4-16. DCAN Controller Block Diagram (μPD780701Y only)



The DCAN interface section processes all protocol operations by means of the DCAN protocol section hardware.

The memory access engine either fetches the DCAN protocol data transmitted from a specific RAM area and transfers it to the DCAN protocol section, or compares and sorts the fetched data and then stores it in a predefined RAM area.

The DCAN allows direct interfacing between the DCAN and the accessible CPU area, as well as between the CPU and that area without any effect on the CPU. The DCAN section operates with the external bus transceiver that converts transmit data line and receive data line to the electrical characteristics of DCAN bus.

4.8 IEBus Controller (μPD780702Y only)

The μPD780702Y incorporates an IEBus controller. The functions of the IEBus interface are limited compared with those of previous models (i.e., those incorporated in the μPD78098B Subseries).

Table 4-4 shows a comparison of the interfaces in the μPD78098B Subseries and the μPD780702Y.

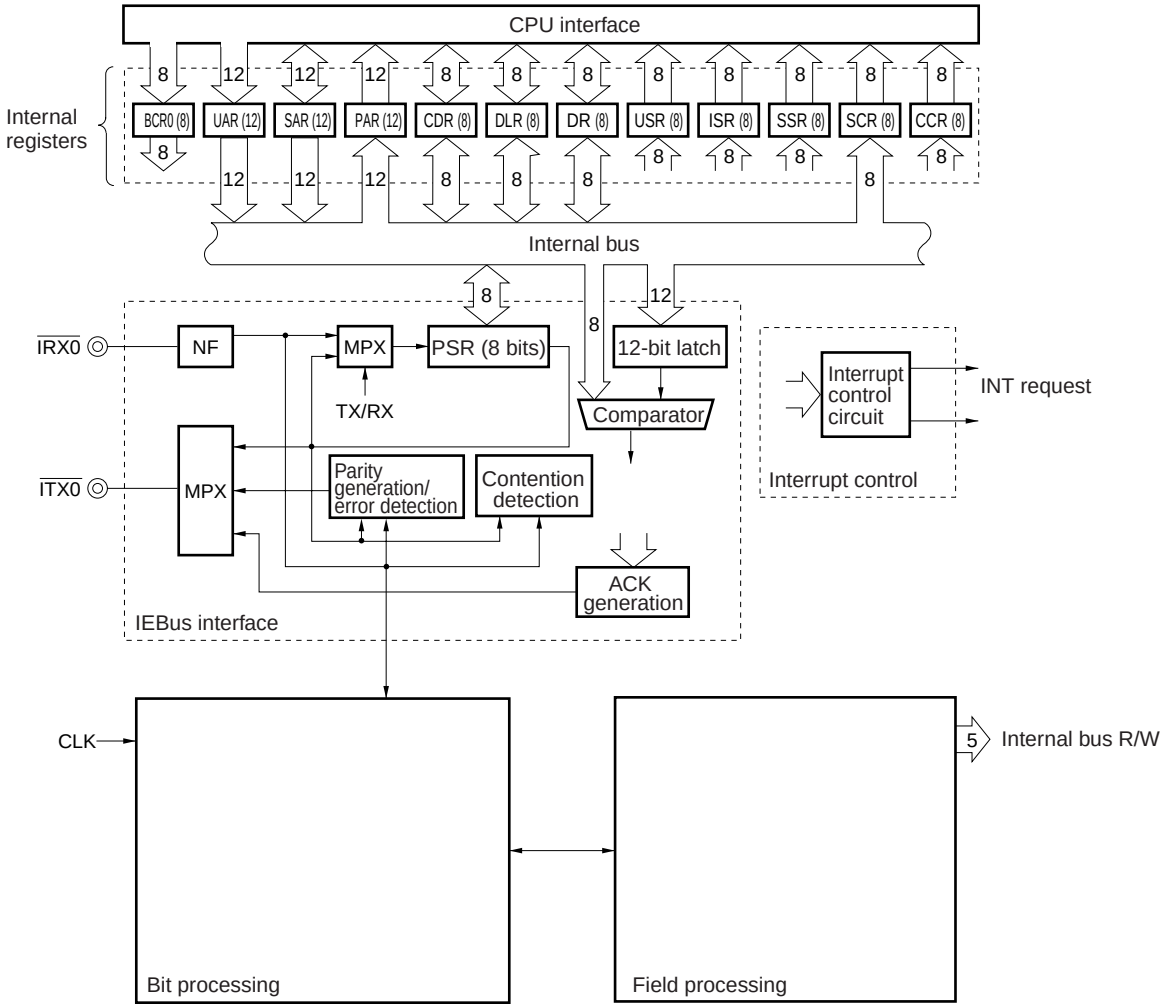
Table 4-4. IEBus Interface Comparison (μPD78098B Subseries and μPD780702Y)

Item	IEBus Incorporated in μPD78098B Subseries	IEBus Incorporated in μPD780702Y
Communication mode	Mode 0, mode 1, mode 2	Fixed at mode 1
Internal system clock	f_X = 6.0 (6.29) MHz	f_X = 6.291456 MHz[Note]
Internal buffer size	Transmit buffers: 33 bytes (FIFO) Receive buffers: 40 bytes (FIFO) Up to 4 frames receivable	Transmit buffers: 1 byte Receive buffers: 1 byte
CPU processing	Processing before start of communication (data setting) Setting, controlling each communication status Writing data to transmit buffers Reading data from receive buffers	Processing before start of communication (data setting) Setting, controlling each communication status Data write processing in one-byte units Data read processing in one-byte units Transmission control of slave status, etc. Multiple-frame control, repeat master-request processing
Hard processing	Bit processing (modem, error detection) Field processing (generation/control) Arbitration result detection Parity processing (generation/error detection) ACK/NACK automatic response Automatic retransmit-of-data processing Automatic remaster processing Automatic transmission processing of slave status, etc. Multiple-frame reception processing	Bit processing (modem, error detection) Field processing (generation/control) Arbitration result detection Parity processing (generation/error detection) ACK/NACK automatic response Automatic retransmit-of-data processing

Note The μPD780702Y only supports an IEBus controller that operates at f_X = 6.291456 MHz.

Remark f_X: System clock frequency

Figure 4-17. IEBus Controller Block Diagram (μPD780702Y only)



The IEBus is broadly configured from the following 6 blocks.

- CPU interface
- Interrupt control
- Internal registers
- Bit processing
- Field processing
- IEBus interface

<CPU interface>
This is a control block whose purpose is to interface between the CPU (78K/0) and the IEBus main unit.

<Interrupt control>
This is a control block whose purpose is to pass on interrupt request signals from the IEBus main unit to the CPU.

<Internal registers>
This block sets the control registers that control the IEBus and the data of each field.

<Bit processing>
This block performs the bit timing generation and resolution, and is mainly configured from bit sequence ROM, an 8-bit preset timer, and a determiner.

<Field processing>
This block generates each field in the communication frame, and is mainly configured from field sequence ROM, a 4-bit down counter, and a determiner.

<IEBus interface>
This is the external driver/receiver interface block, and is mainly configured from a noise filter, a shift register, a contention detector, a parity detector, a parity generation circuit, and an ACK/NACK generation circuit.

5. INTERRUPT FUNCTIONS

A total of 30 interrupt sources are provided in the μPD780701Y, and a total of 29 interrupt sources are provided in the μPD780702Y, divided into the following three types.

- Non-maskable: 1
- Maskable: 28 (μPD780701Y)
  27 (μPD780702Y)
- Software: 1

Table 5-1. Interrupt Source List (1/2)

Interrupt Type	Default Priority[Note 1]	Interrupt Source		Internal/ External	Vector Table Address	Basic Configuration Type[Note 2]
		Name	Trigger			
Non-maskable	–	INTWDT	Watchdog timer overflow (with non-maskable interrupt selected)	Internal	0004H	(A)
Maskable	0	INTWDT	Watchdog timer overflow (with interval timer selected)			(B)
	1	INTP0	Pin input edge detection	External	0006H	(C)
	2	INTP1			0008H	
	3	INTP2			000AH	
	4	INTP3			000CH	
	5	INTP4			000EH	
	6	INTP5			0010H	
	7	INTP6			0012H	
	8	INTP7			0014H	
	9	INTSER0	Occurrence of UART0 reception error	Internal	0016H	(B)
	10	INTSR0	End of UART0 reception		0018H	
	11	INTST0	End of UART0 transmission		001AH	
	12	INTCSI30	End of SIO30 transfer		001CH	
	13	INTCSI31	End of SIO31 transfer		001EH	
	14	INTIIC0	End of IIC0 transfer		0020H	
	15	INTCE[Note 3]	DCAN error		0022H	
	16	INTCR[Note 3]/ INTIE1[Note 4]	DCAN reception/ IEBus data access request		0024H	
	17	INTCT[Note 3]/ INTIE2[Note 4]	DCAN transmission buffer/ IEBus communication error and start/end of communication		0026H	
	18	INTWTNI0	Reference time interval signal from watch timer		0028H	
	19	INTTM000	Generation of matching signal of TM00 and CR000 (with compare register specified) TI000 valid edge detection (with capture register specified)		002AH	

Notes 1. Default priority is the priority order when several maskable interrupt requests are generated at the same time. 0 is the highest order and 28 is the lowest order.

2. Basic configuration types (A) to (E) correspond to (A) to (E) in Figure 5-1.

3. μPD780701Y only

4. μPD780702Y only

Table 5-1. Interrupt Source List (2/2)

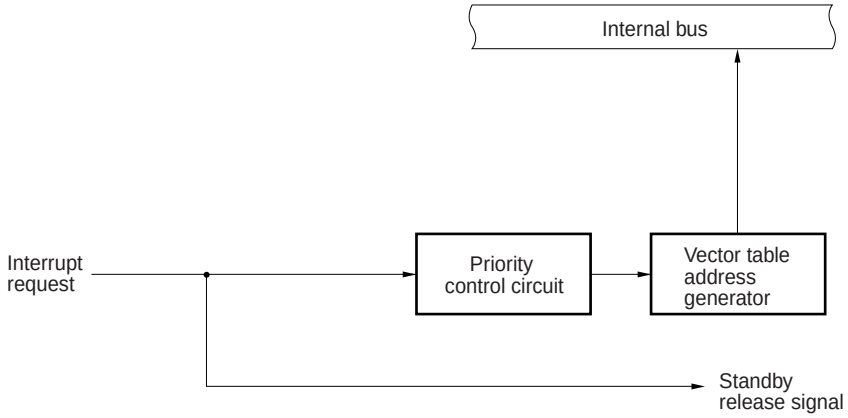
Interrupt Type	Default Priority[Note 1]	Interrupt Source		Internal/ External	Vector Table Address	Basic Configuration Type[Note 2]
		Name	Trigger			
Maskable	20	INTTM010	Generation of matching signal of TM00 and CR010 (with compare register specified) TI010 valid edge detection (with capture register specified)	Internal	002CH	(B)
	21	INTTM001	Generation of matching signal of TM01 and CR001 (with compare register specified) TI001 valid edge detection (with capture register specified)		002EH	
	22	INTTM011	Generation of matching signal of TM01 and CR011 (with compare register specified) TI011 valid edge detection (with capture register specified)		0030H	
	23	INTTM50	Generation of matching signal of TM50 and CR50		0032H	
	24	INTTM51	Generation of matching signal of TM51 and CR51		0034H	
	25	INTTM52	Generation of matching signal of TM52 and CR52		0036H	
	26	INTAD	End of conversion by A/D converter		0038H	
	27	INTWTN0	Watch timer overflow		003AH	
	28	INTKR	Port 4 falling edge detection	External	003CH	(D)
Software	–	BRK	Execution of BRK instruction	–	003EH	(E)

Notes 1. Default priority is the priority order when several maskable interrupt requests are generated at the same time. 0 is the highest order and 28 is the lowest order.

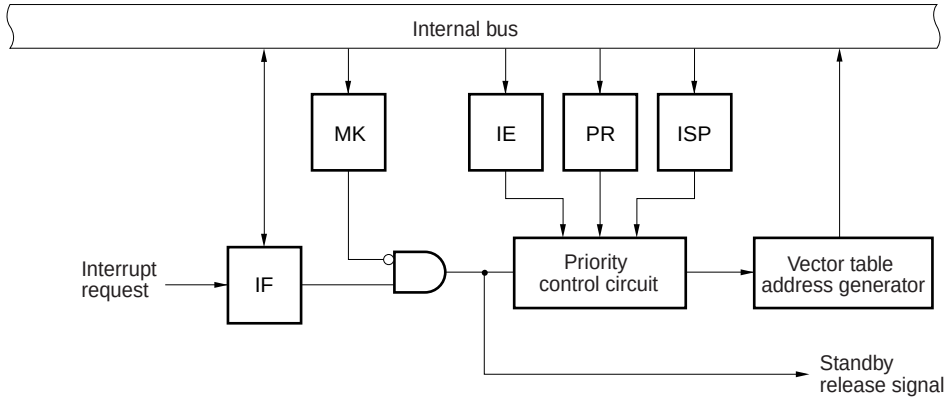
2. Basic configuration types (A) to (E) correspond to (A) to (E) in Figure 5-1.

Figure 5-1. Basic Configuration of Interrupt Function (1/2)

(A) Internal non-maskable interrupt



(B) Internal maskable interrupt



(C) External maskable interrupt (INTP0 to INTP7)

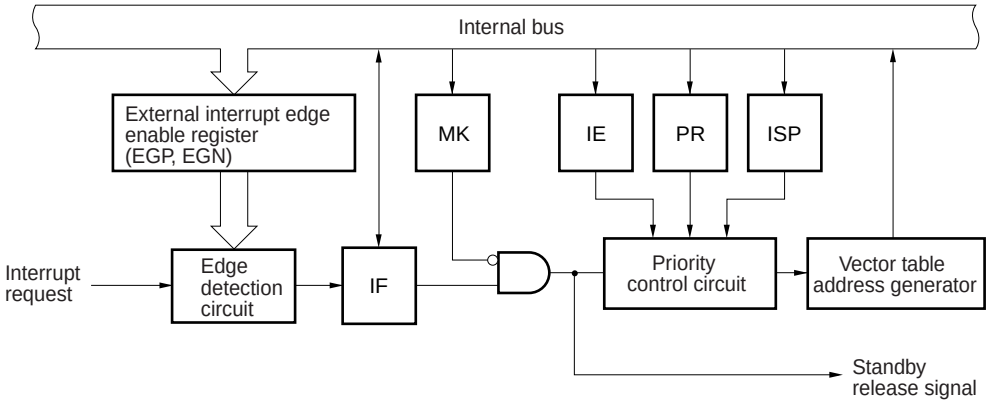
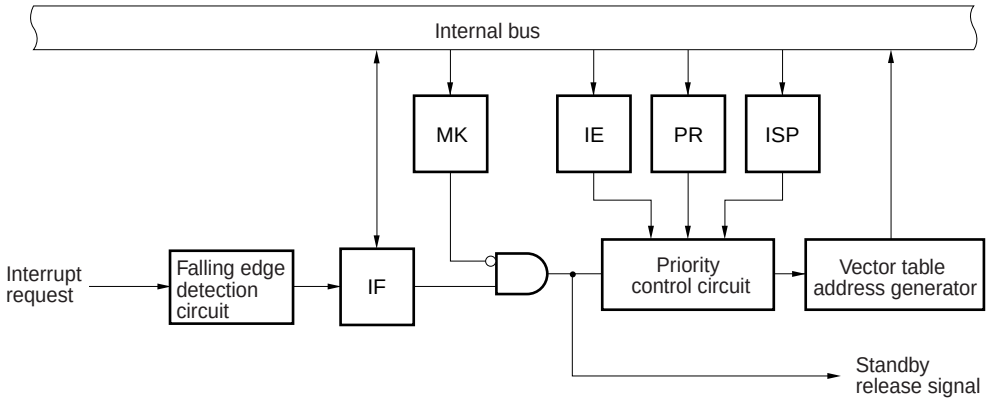
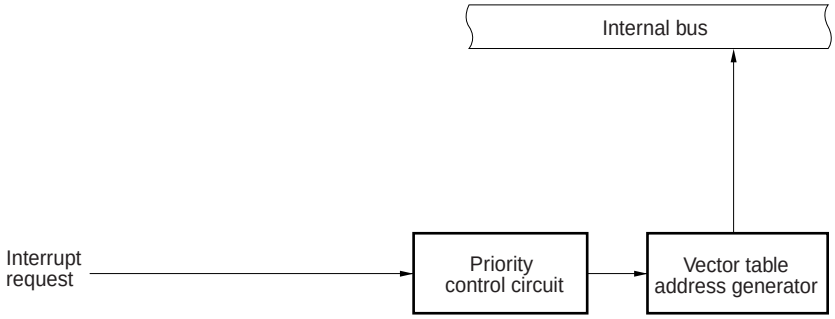


Figure 5-1. Basic Configuration of Interrupt Function (2/2)

(D) External maskable interrupt (INTKR)



(E) Software interrupt



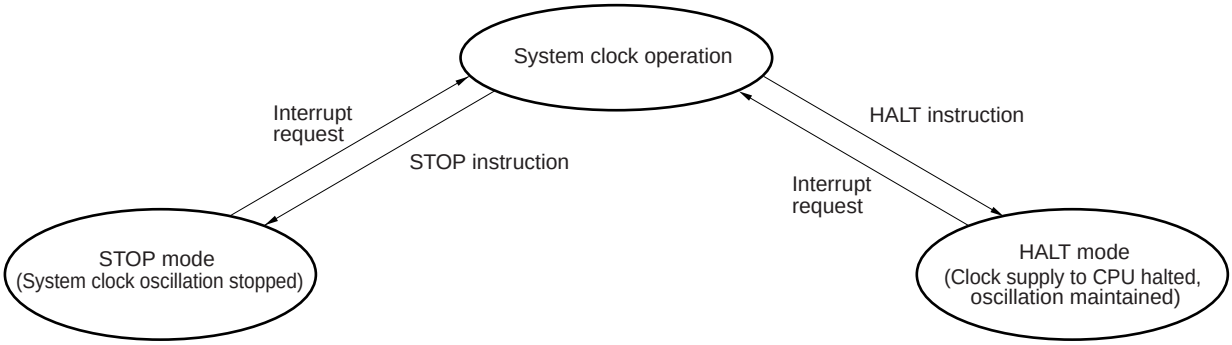
IF: Interrupt request flag
IE: Interrupt enable flag
ISP: In-service priority flag
MK: Interrupt mask flag
PR: Priority specification flag

6. STANDBY FUNCTION

The following two standby functions are available for further reduction of system current consumption.

- HALT mode: In this mode, the CPU operation clock is stopped. The average current consumption can be reduced by intermittent operation by combining this mode with the normal operation mode.
- STOP mode: In this mode, oscillation of the system clock is stopped. All the operations performed on the system clock are suspended, resulting in extremely small current consumption.

Figure 6-1. Standby Function



7. RESET FUNCTION

The following two reset methods are available.

- External reset by $\overline{\text{RESET}}$ signal input
- Internal reset by watchdog timer runaway time detection

8. INSTRUCTION SET

(1) 8-bit instructions

MOV, XCH, ADD, ADDC, SUB, SUBC, AND, OR, XOR, CMP, MULU, DIVUW, INC, DEC, ROR, ROL, RORC, ROLC, ROR4, ROL4, PUSH, POP, DBNZ

2nd operand / 1st operand	#byte	A	r[Note]	sfr	saddr	!addr16	PSW	[DE]	[HL]	[HL+byte] [HL+B] [HL+C]	$addr16	1	None
A	ADD ADDC SUB SUBC AND OR XOR CMP		MOV XCH ADD ADDC SUB SUBC AND OR XOR CMP	MOV XCH	MOV XCH ADD ADDC SUB SUBC AND OR XOR CMP	MOV XCH ADD ADDC SUB SUBC AND OR XOR CMP	MOV	MOV XCH	MOV XCH ADD ADDC SUB SUBC AND OR XOR CMP	MOV XCH ADD ADDC SUB SUBC AND OR XOR CMP		ROR ROL RORC ROLC	
r	MOV	MOV ADD ADDC SUB SUBC AND OR XOR CMP											INC DEC
B, C											DBNZ		
sfr	MOV	MOV											
saddr	MOV ADD ADDC SUB SUBC AND OR XOR CMP	MOV									DBNZ		INC DEC
!addr16		MOV											
PSW	MOV	MOV											PUSH POP
[DE]		MOV											
[HL]		MOV											ROR4 ROL4
[HL+byte] [HL+B] [HL+C]		MOV											
X													MULU
C													DIVUW

Note Except r = A

(2) 16-bit instructions

MOVW, XCHW, ADDW, SUBW, CMPW, PUSH, POP, INCW, DECW

2nd operand / 1st operand	#word	AX	rp[Note]	sfrp	saddrp	!addr16	SP	None
AX	ADDW SUBW CMPW		MOVW XCHW	MOVW	MOVW	MOVW	MOVW	
rp	MOVW	MOVW[Note]						INCW, DECW PUSH, POP
sfrp	MOVW	MOVW						
saddrp	MOVW	MOVW						
!addr16		MOVW						
SP	MOVW	MOVW						

Note Only when rp = BC, DE, HL

(3) Bit manipulation instructions

MOV1, AND1, OR1, XOR1, SET1, CLR1, NOT1, BT, BF, BTCLR

2nd operand / 1st operand	A.bit	sfr.bit	saddr.bit	PSW.bit	[HL].bit	CY	$addr16	None
A.bit						MOV1	BT BF BTCLR	SET1 CLR1
sfr.bit						MOV1	BT BF BTCLR	SET1 CLR1
saddr.bit						MOV1	BT BF BTCLR	SET1 CLR1
PSW.bit						MOV1	BT BF BTCLR	SET1 CLR1
[HL].bit						MOV1	BT BF BTCLR	SET1 CLR1
CY	MOV1 AND1 OR1 XOR1	MOV1 AND1 OR1 XOR1	MOV1 AND1 OR1 XOR1	MOV1 AND1 OR1 XOR1	MOV1 AND1 OR1 XOR1			SET1 CLR1 NOT1

(4) Call instructions/branch instructions

CALL, CALLF, CALLT, BR, BC, BNC, BZ, BNZ, BT, BF, BTCLR, DBNZ

2nd operand / 1st operand	AX	!addr16	!addr11	[addr5]	$addr16
Basic instruction	BR	CALL BR	CALLF	CALLT	BR, BC, BNC BZ, BNZ
Compound instruction					BT, BF BTCLR, DBNZ

(5) Other instructions

ADJBA, ADJBS, BRK, RET, RETI, RETB, SEL, NOP, EI, DI, HALT, STOP

9. ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings (T_A = 25°C)

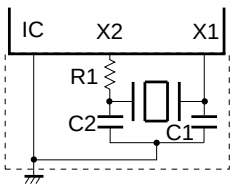
Parameter	Symbol	Conditions		Ratings	Unit
Power supply voltage	V_{DD}	$V_{DD} = AV_{REF}$		–0.3 to +6.5	V
	AV_{REF}				
	AV_{SS}			–0.3 to +0.3	V
Input voltage	V_{I1}	P00 to P07, P20 to P27, P30 to P32, P34 to P36, P40 to P47, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P90 to P97, CRXD, $\overline{IRX0}$, X1, X2, $\overline{RESET}$		–0.3 to V_{DD} + 0.3	V
	V_{I2}	P33	N-ch open drain	–0.3 to +16	V
Output voltage	V_O	P00 to P07, P20 to P27, P30 to P36, P40 to P47, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P90 to P97, CTXD, $\overline{ITX0}$		–0.3 to V_{DD} + 0.3	V
Analog input voltage	V_{AN}	P80 to P87, P90 to P97	Analog input pin	AV_{SS} – 0.3 to AV_{REF} + 0.3 and –0.3 to V_{DD} + 0.3	V
Output current, high	I_{OH}	Per pin for P00 to P07, P20 to P27, P30 to P32, P34 to P36, P40 to P47, P50 to P57, P64 to P67, P70, P73 to P77, P80 to P87, P90 to P97, CRXD, $\overline{IRX0}$		–10	mA
		Total for all pins		–30	mA
Output current, low	I_{OL} Note	Per pin for P00 to P07, P20 to P27, P30 to P32, P34 to P36, P40 to P47, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P90 to P97, CTXD, $\overline{ITX0}$	Peak value	20	mA
			rms value	10	mA
		P33	Peak value	30	mA
			rms value	15	mA
		Total for all pins	Peak value	100	mA
			rms value	60	mA
Operating ambient temperature	T_A			–40 to +85	°C
Storage temperature	T_{stg}			–65 to +150	°C

Note The rms value should be calculated as follows: [rms value] = [Peak value] $\times \sqrt{\text{Duty}}$

Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of port pins.

System Clock Oscillator Characteristics (T_A = –40 to +85°C, V_{DD} = 3.5 to 5.5 V)

Resonator	Recommended Circuit	Parameter	Conditions	MIN.	TYP.	MAX.	Unit
Crystal resonator		Oscillation frequency (f_X)[Note 1]			6.29[Note 2]		MHz
		Oscillation stabilization time[Note 3]				30	ms

Notes 1. Indicates only oscillator characteristics.

2. 6.29 = 6.291456 (MHz)

3. Time required to stabilize oscillation after reset or STOP mode release.

Caution When using the system clock oscillator, wire as follows in the area enclosed by the broken lines in the above figure to avoid an adverse effect from wiring capacitance.

- **Keep the wiring length as short as possible.**
- **Do not cross the wiring with the other signal lines.**
- **Do not route the wiring near a signal line through which a high fluctuating current flows.**
- **Always make the ground point of the oscillator capacitor the same potential as V_{SS1}.**
- **Do not ground the capacitor to a ground pattern through which a high current flows.**
- **Do not fetch signals from the oscillator.**

DC Characteristics (T_A = –40 to +85°C, V_{DD} = 3.5 to 5.5 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Input voltage, high	V_{IH1}	P21, P23, P25, P27, P31, P34, P40 to P47, P64 to P67, P73, P80 to P87, P90 to P97		0.7V_{DD}		V_{DD}	V
	V_{IH2}	P00 to P07, P20, P22, P24, P26, P30, P32, P35, P36, P70 to P72, P74 to P77, CRXD, $\overline{IRX0}$, $\overline{RESET}$		0.8V_{DD}		V_{DD}	V
	V_{IH3}	P50 to P57		2.3		V_{DD}	V
	V_{IH4}	P33	N-ch open drain	0.7V_{DD}		15	V
	V_{IH5}	X1, X2		V_{DD} – 0.5		V_{DD}	V
Input voltage, low	V_{IL1}	P21, P23, P25, P27, P31, P34, P40 to P47, P64 to P67, P73, P80 to P87, P90 to P97		0		0.3V_{DD}	V
	V_{IL2}	P00 to P07, P20, P22, P24, P26, P30, P32, P35, P36, P70 to P72, P74 to P77, CRXD, $\overline{IRX0}$, $\overline{RESET}$		0		0.2V_{DD}	V
	V_{IL3}	P50 to P57		0		0.75	V
	V_{IL4}	P33	N-ch open drain	0		0.3V_{DD}	V
	V_{IL5}	X1, X2		0		0.4	V
Output voltage, high	V_{OH1}	I_{OH} = –1 mA	P00 to P07, P20 to P27, P30 to P32, P34 to P36, P40 to P47, P50 to P57, P64 to P67, P70, P73 to P77, P80 to P87, P90 to P97, CTXD, $\overline{ITX0}$	V_{DD} – 1.0		V_{DD}	V
	V_{OH2}	I_{OH} = –100 μA		V_{DD} – 0.5		V_{DD}	V
Output voltage, low	V_{OL1}	I_{OL} = 15 mA	P33		0.4	2.0	V
	V_{OL2}	I_{OL} = 1.6 mA	P71, P72			0.4	V
	V_{OL3}	I_{OL} = 1 mA	P00 to P07, P20 to P27, P30 to P32, P34 to P36, P40 to P47, P50 to P57, P64 to P67, P70, P73 to P77, P80 to P87, P90 to P97, CTXD, $\overline{ITX0}$			1.0	V
	V_{OL4}	I_{OL} = 100 μA				0.5	V
Input leakage current, high	I_{LIH1}	V_{IN} = V_{DD}	P00 to P07, P20 to P27, P30 to P32, P34 to P36, P40 to P47, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P90 to P97, CRXD, $\overline{IRX0}$, $\overline{RESET}$			3	μA
	I_{LIH2}		X1, X2			20	μA
	I_{LIH3}	V_{IN} = 15 V	P33			80	μA
Input leakage current, low	I_{LIL1}	V_{IN} = 0 V	P00 to P07, P20 to P27, P30 to P32, P34 to P36, P40 to P47, P50 to P57, P64 to P67, P80 to P87, P90 to P97, CRXD, $\overline{IRX0}$, $\overline{RESET}$			–3	μA
	I_{LIL2}		X1, X2			–20	μA
	I_{LIL3}		P33 (except executing input instruction[Note])			–3	μA

Note During input instruction execution, a low-level input leakage current of –200 μA (MAX.) flows only for 1 clock (without wait).

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of port pins.

DC Characteristics (T_A = –40 to +85°C, V_{DD} = 3.5 to 5.5 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Output leakage current, high	I_{LOH}	$V_{OUT} = V_{DD}$	P00 to P07, P20 to P27, P30 to P36, P40 to P47, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P90 to P97, CTXD, $\overline{ITX0}$			3	μA
Output leakage current, low	I_{LOL}	V_{OUT} = 0 V	P00 to P07, P20 to P27, P30 to P36, P40 to P47, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P90 to P97, CTXD, $\overline{ITX0}$			–3	μA
Software pull-up resistor	R_1	V_{IN} = 0 V	P00 to P07, P20 to P27, P30 to P32, P34 to P36, P40 to P47, P50 to P57, P64 to P67, P70, P73 to P77	15	30	90	kΩ
Power supply current[Note 1]	I_{DD1}	6.29-MHz crystal oscillation operating mode			4.0	20	mA
	I_{DD2}	6.29-MHz crystal oscillation HALT mode[Note 2]			500	1000	μA
	I_{DD3}	STOP mode			0.1	30	μA

Notes 1. Refers to the current flowing to the V_{DD1} pin. The current flowing to the A/D converter and on-chip pull-up resistor is not included.

2. Low-speed mode operation (when processor clock control register (PCC) is set to 04H). The current for peripheral circuit operation is not included.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of port pins.

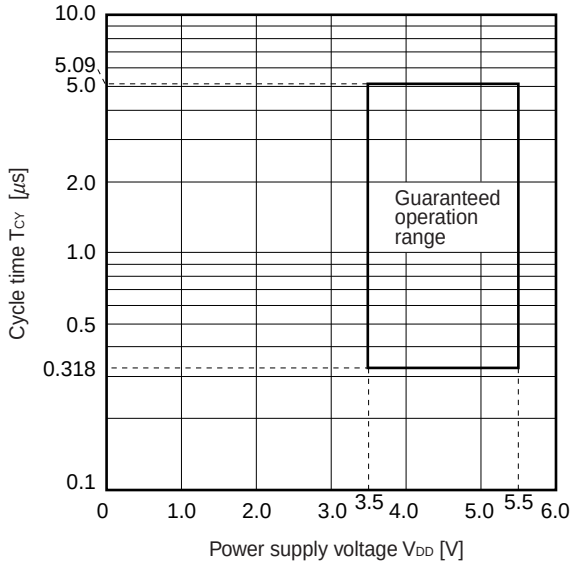
AC Characteristics

(1) Basic operation (T_A = –40 to +85°C, V_{DD} = 3.5 to 5.5 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Cycle time (Min. instruction execution time)	T_{CY}	Operating with system clock (f_X = 6.291456 MHz)	0.318		5.09	μs
TI000, TI010, TI001, TI011 input high-/low-level width	t_{TIH0} t_{TIL0}		$4/f_{sam}$ + 0.25[Note]			μs
TI50, TI51, TI52 input frequency	f_{TI5}				2	MHz
TI50, TI51, TI52 input high-/low-level width	t_{TIH5} t_{TIL5}		200			ns
Interrupt request input high-/low-level width	t_{INTH} t_{INTL}	INTP0 to INTP7, P40 to P47	10			μs
$\overline{\text{RESET}}$ low-level width	t_{RSL}		10			μs

Note Selection of $f_{sam} = f_X/2$, $f_X/4$, $f_X/64$ is possible with bits 0 and 1 (PRM0n0, PRM0n1) of prescaler mode register 0n (PRM0n). However, if the TI00n valid edge is selected as the count clock, the value becomes $f_{sam} = f_X/8$ (n = 0, 1).

T_{CY} vs V_{DD} (At system clock operation)



(2) Serial interface (T_A = –40 to +85°C, V_{DD} = 3.5 to 5.5 V)

(a) 3-wire serial I/O mode ($\overline{SCK30}$ ... Internal clock output)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
$\overline{SCK30}$ cycle time	t_{KCY1}		1.9			μs
$\overline{SCK30}$ high-/low-level width	t_{KH1} t_{KL1}		t_{KCY1}/2 – 50			ns
SI30 setup time (to $\overline{SCK30}$↑)	t_{SIK1}		100			ns
SI30 hold time (from $\overline{SCK30}$↑)	t_{KSI1}		400			ns
SO30 output delay time from $\overline{SCK30}$↓	t_{KSO1}	C = 100 pF[Note]			300	ns

Note C is the load capacitance of the $\overline{SCK30}$ and SO30 output lines.

(b) 3-wire serial I/O mode ($\overline{SCK30}$ ... External clock input)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
$\overline{SCK30}$ cycle time	t_{KCY2}		800			ns
$\overline{SCK30}$ high-/low-level width	t_{KH2} t_{KL2}		400			ns
SI30 setup time (to $\overline{SCK30}$↑)	t_{SIK2}		100			ns
SI30 hold time (from $\overline{SCK30}$↑)	t_{KSI2}		400			ns
SO30 output delay time from $\overline{SCK30}$↓	t_{KSO2}	C = 100 pF[Note]			300	ns

Note C is the load capacitance of the SO30 output line.

(c) 3-wire serial I/O mode ($\overline{SCK31}$ ... Internal clock output)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
$\overline{SCK31}$ cycle time	t_{KCY3}		1.9			μs
$\overline{SCK31}$ high-/low-level width	t_{KH3} t_{KL3}		t_{KCY1}/2 – 50			ns
SI31 setup time (to $\overline{SCK31}$↑)	t_{SIK3}		100			ns
SI31 hold time (from $\overline{SCK31}$↑)	t_{KSI3}		400			ns
SO31 output delay time from $\overline{SCK31}$↓	t_{KSO3}	C = 100 pF[Note]			300	ns

Note C is the load capacitance of the $\overline{SCK31}$ and SO31 output lines.

(d) 3-wire serial I/O mode ($\overline{SCK31}$ ... External clock input)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
$\overline{SCK31}$ cycle time	t_{KCY4}		800			ns
$\overline{SCK31}$ high-/low-level width	t_{KH4} t_{KL4}		400			ns
SI31 setup time (to $\overline{SCK31}$↑)	t_{SIK4}		100			ns
SI31 hold time (from $\overline{SCK31}$↑)	t_{KSI4}		400			ns
SO31 output delay time from $\overline{SCK31}$↓	t_{KSO4}	C = 100 pF[Note]			300	ns

Note C is the load capacitance of the SO31 output line.

(e) UART mode (Dedicated baud rate generator output)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Transfer rate					38836	bps

(f) UART mode (External clock input)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
ASCK0 cycle time	t_{KCY3}		800			ns
ASCK0 high-/low-level width	t_{KH3}, t_{KL3}		400			ns
Transfer rate					39063	bps

(g) I^2C bus mode

Parameter		Symbol	Standard Mode		High-speed Mode		Unit
			MIN.	MAX.	MIN.	MAX.	
SCL0 clock frequency		f_{SCL}	0	100	0	400	kHz
Bus free time (between stop and start conditions)		t_{BUF}	4.7	–	1.3	–	μs
Hold time[Note 1]		$t_{HD:STA}$	4.0	–	0.6	–	μs
SCL0 clock low-level width		t_{LOW}	4.7	–	1.3	–	μs
SCL0 clock high-level width		t_{HIGH}	4.0	–	0.6	–	μs
Start/restart condition setup time		$t_{SU:STA}$	4.7	–	0.6	–	μs
Data hold time	CBUS compatible master	$t_{HD:DAT}$	5.0	–	–	–	μs
	I^2C bus		0[Note 2]	–	0[Note 2]	0.9[Note 3]	μs
Data setup time		$t_{SU:DAT}$	250	–	100[Note 4]	–	ns
SDA0 and SCL0 signal rise time		t_R	–	1000	–	300	ns
SDA0 and SCL0 signal fall time		t_F	–	300	–	300	ns
Stop condition setup time		$t_{SU:STO}$	4.0	–	0.6	–	μs
Spike pulse width controlled by input filter		t_{SP}	–	–	0	50	ns
Capacitive load of each bus line		Cb	–	400	–	400	pF

Notes 1. On start condition, the first clock pulse is generated after this period.

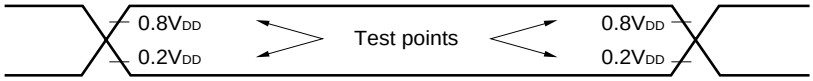
2. To fulfill undefined area of the SCL0 falling edge, it is necessary for the device to provide internally SDA0 signal (on $V_{IHmin.}$ of SCL0 signal) with at least 300 ns of hold time.

3. If the device does not extend the SCL0 signal low hold time (t_{LOW}), only maximum data hold time $t_{HD:DAT}$ needs to be fulfilled.

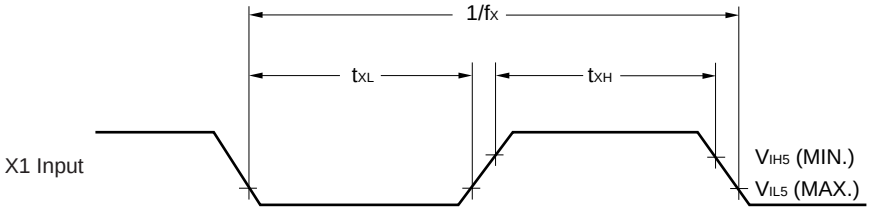
4. The high-speed mode I^2C bus is available in the standard mode I^2C bus system. At this time, the conditions described below must be satisfied.

- If the device does not extend the SCL0 signal low state hold time
  $t_{SU:DAT} \geq 250$ ns
- If the device extends the SCL0 signal low state hold time
  Be sure to transmit the next data bit to the SDA0 line before the SCL0 line is released ($t_{Rmax.} + t_{SU:DAT}$ = 1000 + 250 = 1250 ns by standard mode I^2C bus specification).

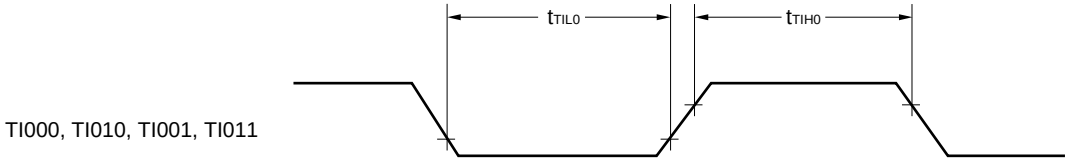
AC Timing Test Points (excluding X1 input)

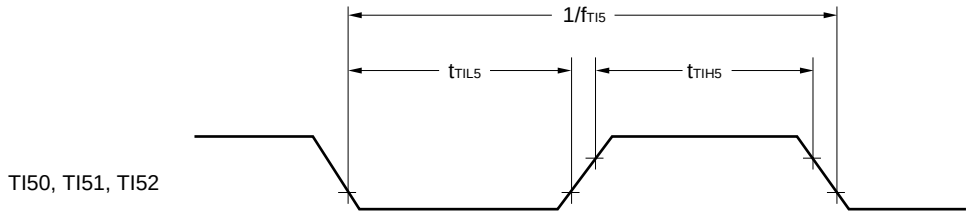


Clock Timing



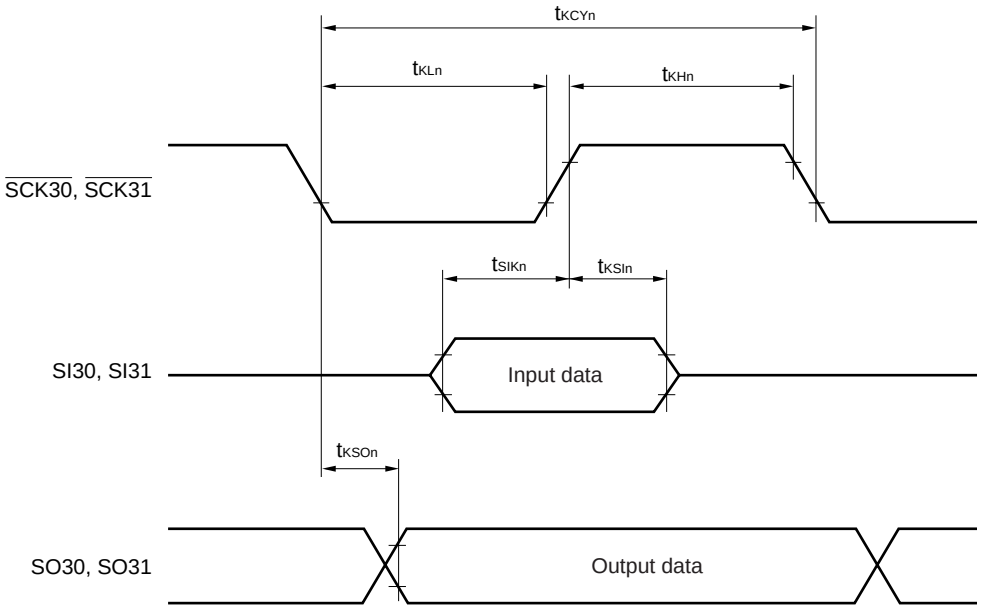
TI Timing





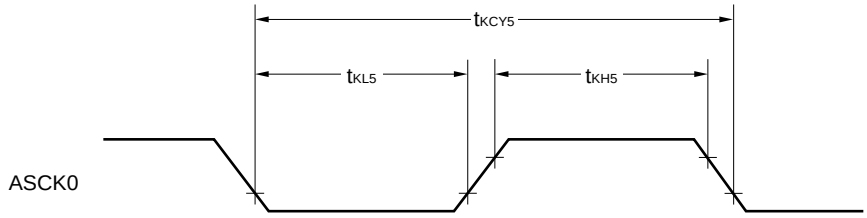
Serial Transfer Timing

3-wire serial I/O mode:

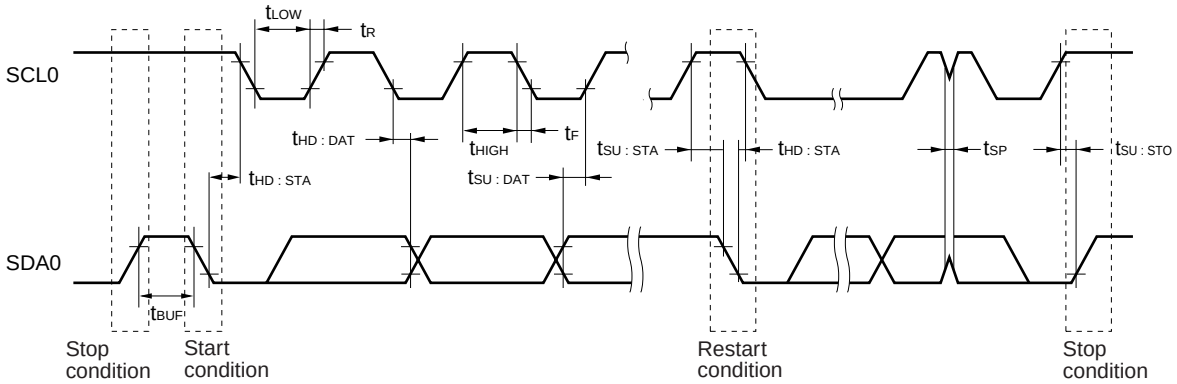


n = 1 to 4

UART mode (external clock input):



I²C bus mode:



IEBus0 Controller Characteristics (T_A = –40 to +85°C, V_{DD} = 3.5 to 5.5 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
IEBus system clock frequency	f_S	Fixed at mode 1		6.29		MHz
Driver delay time (Bus line from $\overline{ITX0}$ output)	t_{DTX}	C = 50 pF[Note] The μPC2590 is used as a driver/receiver			1.5	μs
Receiver delay time ($\overline{IRX0}$ input from bus line)	t_{DRX}	The μPC2590 is used as a driver/receiver			0.7	μs
Propagation delay time on bus	t_{DBUS}	The μPC2590 is used as a driver/receiver			0.85	μs

Note C is the load capacitance of the $\overline{ITX0}$ output line.

Remarks 1. Although the standard system clock frequency for the IEBus is 6.0 MHz, the μPD780702Y guarantees normal operation of the IEBus controller at 6.29 MHz.

2. f_S: IEBus controller system clock frequency

A/D Converter Characteristics (T_A = –40 to +85°C, V_{DD} = AV_{REF} = 3.5 to 5.5 V, V_{SS} = AV_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Resolution			8	8	8	bit
Overall error[Note]					±0.6	%
Conversion time	t_{CONV}		14		100	μs
Analog input voltage	V_{IAN}		AV_{SS}		AV_{REF}	V
AV_{REF} resistance	R_{AIREF}		T.B.D	28	T.B.D	kΩ

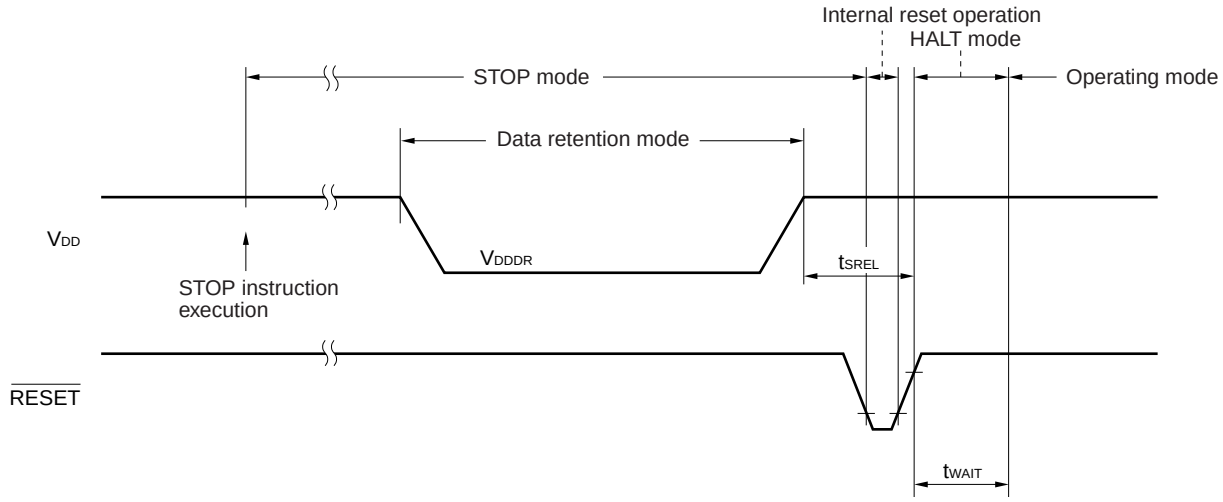
Note Excludes quantization error (±0.2%). It is indicated as a ratio to the full-scale value.

Data Memory STOP Mode Low Supply Voltage Data Retention Characteristics (T_A = –40 to +85°C)

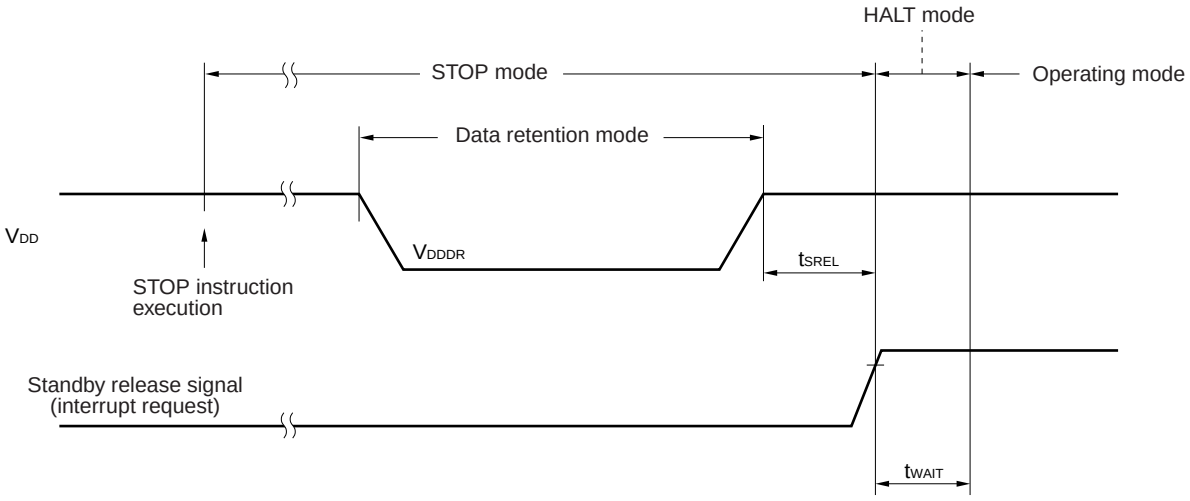
Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Data retention power supply voltage	V_{DDDR}		2.0		5.5	V
Data retention power supply current	I_{DDDR}	V_{DDDR} = 2.0 V		0.1	10	μA
Release signal set time	t_{SREL}		0			μs
Oscillation stabilization wait time	t_{WAIT}	Release by $\overline{RESET}$		$2^{17}/f_X$		ms
		Release by interrupt request		**Note**		ms

Note Selection of $2^{12}/f_X$, $2^{14}/f_X$, $2^{19}/f_X$, and $2^{21}/f_X$ is possible with bits 0 to 2 (OSTS0 to OSTS2) of the oscillation stabilization time select register (OSTS).

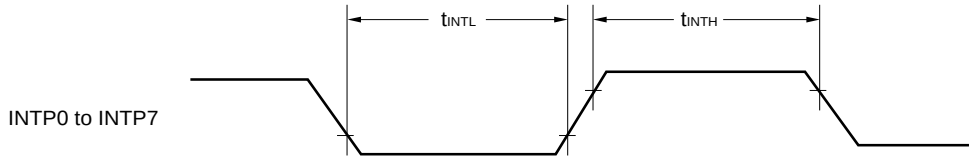
Data Retention Timing (STOP mode release by $\overline{RESET}$)



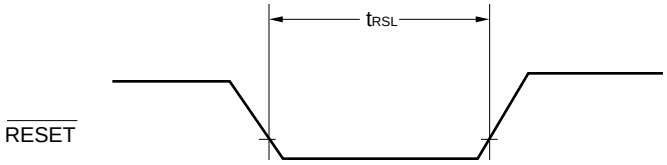
Data Retention Timing (Standby release signal: STOP mode release by interrupt request signal)



Interrupt Request Input Timing

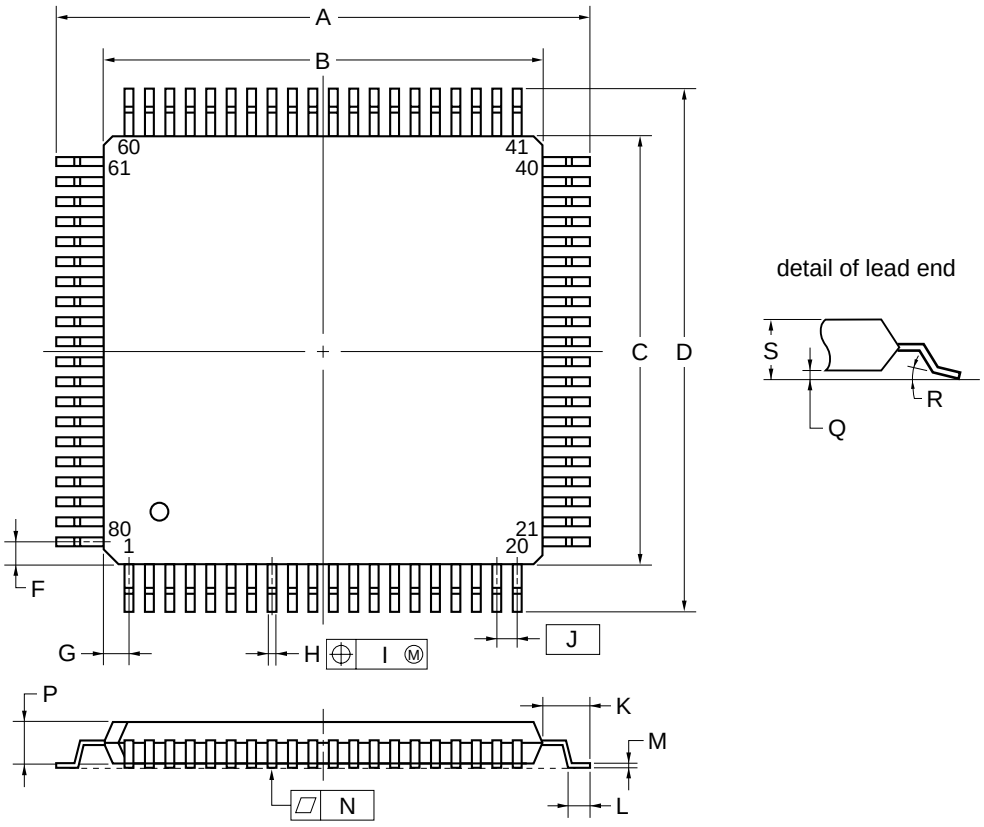


$\overline{\text{RESET}}$ Input Timing



10. PACKAGE DRAWING

80 PIN PLASTIC QFP (14×14)



NOTE

Each lead centerline is located within 0.13 mm (0.005 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	17.20±0.20	0.677±0.008
B	14.00±0.20	$0.551^{+0.009}_{-0.008}$
C	14.00±0.20	$0.551^{+0.009}_{-0.008}$
D	17.20±0.20	0.677±0.008
F	0.825	0.032
G	0.825	0.032
H	0.32±0.06	$0.013^{+0.002}_{-0.003}$
I	0.13	0.005
J	0.65 (T.P.)	0.026 (T.P.)
K	1.60±0.20	0.063±0.008
L	0.80±0.20	$0.031^{+0.009}_{-0.008}$
M	$0.17^{+0.03}_{-0.07}$	$0.007^{+0.001}_{-0.003}$
N	0.10	0.004
P	1.40±0.10	0.055±0.004
Q	0.125±0.075	0.005±0.003
R	$3^{\circ}{}^{+7^{\circ}}_{-3^{\circ}}$	$3^{\circ}{}^{+7^{\circ}}_{-3^{\circ}}$
S	1.70 MAX.	0.067 MAX.

P80GC-65-8BT

APPENDIX A. DEVELOPMENT TOOLS

The following development tools are available for system development using the μPD780701Y Subseries. Also refer to **(5) Cautions on Using Development Tools**.

(1) Language Processing Software

RA78K/0	Assembler package common to 78K/0 Series
CC78K/0	C compiler package common to 78K/0 Series
DF780701[Note]	Device file for μPD780701Y Subseries
CC78K/0-L	C compiler library source file common to 78K/0 Series

Note Under development

(2) Flash Memory Writing Tools

Flashpro II (Part No. FL-PR2), Flashpro III (Part No. FL-PR3, PG-FP3)	Dedicated flash programmer for microcomputers incorporating flash memory
FA-80GC	Adapter for writing to flash memory for use in an 80-pin plastic QFP (GC-8BT type). An adjusting connection to the target product is necessary.
Flashpro II controller, Flashpro III controller	Program that is controlled from a PC and comes together with Flashpro II and Flashpro III. It operates in environments such as Windows™ 95.

(3) Debugging Tools

- **When IE-78K0-NS in-circuit emulator is used**

IE-78K0-NS	In-circuit emulator common to 78K/0 Series
IE-70000-MC-PS-B	Power supply unit for IE-78K0-NS
IE-70000-98-IF-C	Interface adapter necessary when using PC-9800 series PC (except notebook type) as host machine (C bus supported)
IE-70000-CD-IF-A	PC card and interface cable necessary when using notebook PC as host machine (PCMCIA socket supported)
IE-70000-PC-IF-C	Interface adapter necessary when using IBM PC/AT™ compatible as host machine (ISA bus supported)
IE-70000-PCI-IF	Adapter necessary when using personal computer incorporating PCI bus as host machine
IE-780701-NS-EM1[Note]	Emulation board to emulate μPD780701Y Subseries
NP-80GC	Emulation probe for 80-pin plastic QFP (GC-8BT type)
EV-9200GC-80	Conversion socket to connect the NP-80GC and a target system board on which an 80-pin plastic QFP (GC-8BT type) can be mounted
ID78K0-NS	Integrated debugger for IE-78K0-NS
SM78K0	System simulator common to 78K/0 Series
DF780701[Note]	Device file for μPD780701Y Subseries

Note Under development

- **When IE-78001-R-A in-circuit emulator is used**

IE-78001-R-A	In-circuit emulator common to 78K/0 Series
IE-70000-98-IF-C	Interface adapter necessary when using PC-9800 series PC (except notebook type) as host machine (C bus supported)
IE-70000-PC-IF-C	Interface adapter necessary when using IBM PC/AT compatible as host machine (ISA bus supported)
IE-70000-PCI-IF	Adapter necessary when using personal computer incorporating PCI bus as host machine
IE-78000-R-SV3	Interface adapter and cable necessary when using EWS as host machine
IE-780701-NS-EM1[Note]	Emulation board to emulate μPD780701Y Subseries
IE-78K0-R-EX1	Emulation probe conversion board necessary when using IE-780701-NS-EM1 on IE-78001-R-A
EP-78230GC-R	Emulation probe for 80-pin plastic QFP (GC-8BT type)
EV-9200GC-80	Conversion socket to connect the EP-78230GC-R and a target system board on which an 80-pin plastic QFP (GC-8BT type) can be mounted
ID78K0	Integrated debugger for IE-78001-R-A
SM78K0	System simulator common to 78K/0 Series
DF780701[Note]	Device file for μPD780701Y Subseries

Note Under development

(4) Real-time OS

RX78K/0	Real-time OS for 78K/0 Series
MX78K0	OS for 78K/0 Series

(5) Cautions on Using Development Tools

- The ID78K0-NS, ID78K0, and SM78K0 are used in combination with the DF780701.
- The CC78K/0 and RX78K/0 are used in combination with the RA78K/0 and DF780701.
- The FL-PR2, FL-PR3, FA-80GC, and NP-80GC are products made by Naitou Densei Machidaseisakusho Co., Ltd. (TEL +81-44-822-3813). Contact an NEC distributor regarding the purchase of these products.
- For third party development tools, see the **78K/0 Series Selection Guide (U11126E)**.
- The host machine and OS suitable for each software are as follows:

Software \ Host Machine [OS]	PC PC-9800 series [Windows™] IBM PC/AT and compatibles [Japanese/English Windows]	EWS HP9000 series 700™ [HP-UX™] SPARCstation™ [SunOS™, Solaris™] NEWS™ (RISC) [NEWS-OS™]
RA78K/0	√[Note]	√
CC78K/0	√[Note]	√
ID78K0-NS	√	–
ID78K0	√	√
SM78K0	√	–
RX78K/0	√[Note]	√
MX78K0	√[Note]	√

Note DOS-based software

APPENDIX B. RELATED DOCUMENTS

- **Documents Related to Devices**

Document Name	Document No.	
	English	Japanese
μPD780701Y Subseries User's Manual	Under preparation	U13781J
μPD780701Y, 780702Y Preliminary Product Information	This document	U13920J
μPD78F0701Y Preliminary Product Information	U13563E	U13563J
78K/0 Series User's Manual Instructions	U12326E	U12326J

- **Documents Related to Development Tools (User's Manuals)**

Document Name		Document No.	
		English	Japanese
RA78K0 Assembler Package	Operation	U11802E	U11802J
	Language	U11801E	U11801J
	Structured Assembly Language	U11789E	U11789J
RA78K Series Structured Assembler Preprocessor		EEU-1402	U12323J
CC78K0 C Compiler	Operation	U11517E	U11517J
	Language	U11518E	U11518J
CC78K/0 C Compiler Application Note	Programming Know-How	U13034E	U13034J
IE-78K0-NS		To be prepared	To be prepared
IE-78001-R-A		To be prepared	To be prepared
IE-78K0-R-EX1		To be prepared	To be prepared
IE-780701-NS-EM1		To be prepared	To be prepared
EP-780230		EEU-1515	EEU-985
SM78K0 System Simulator Windows Based	Reference	U10181E	U10181J
SM78K Series System Simulator	External Part User Open Interface Specifications	U10092E	U10092J
ID78K0-NS Integrated Debugger Windows Based	Reference	U12900E	U12900J
ID78K0 Integrated Debugger EWS Based	Reference	–	U11151J
ID78K0 Integrated Debugger Windows Based	Guide	U11649E	U11649J
ID78K0 Integrated Debugger PC Based	Reference	U11539E	U11539J

- **Documents Related to Embedded Software (User's Manuals)**

Document Name		Document No.	
		English	Japanese
78K/0 Series Real-Time OS	Fundamental	U11537E	U11537J
	Installation	U11536E	U11536J
78K/0 Series OS MX78K0	Fundamental	U12257E	U12257J

- **Other Related Documents**

Document Name	Document No.	
	English	Japanese
SEMICONDUCTORS SELECTION GUIDE Products & Packages (CD-ROM)	X13769X	
Semiconductor Device Mounting Technology Manual	C10535E	C10535J
Quality Grades on NEC Semiconductor Devices	C11531E	C11531J
NEC Semiconductor Device Reliability/Quality Control System	C10983E	C10983J
Guide to Prevent Damage for Semiconductor Devices by Electrostatic Discharge (ESD)	C11892E	C11892J
Guide to Microcomputer-Related Products by Third Party	–	U11416J

Caution The related documents listed above are subject to change without notice. Be sure to use the latest version of each document for designing.

NOTES FOR CMOS DEVICES

① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

Note:

Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS

Note:

No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note:

Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

Purchase of NEC I^2C components conveys a license under the Philips I^2C Patent Rights to use these components in an I^2C system, provided that the system conforms to the I^2C Standard Specification as defined by Philips.

Regional Information

Some information contained in this document may vary from country to country. Before using any NEC product in your application, please contact the NEC office in your country to obtain a list of authorized representatives and distributors. They will verify:

- Device availability
- Ordering information
- Product release schedule
- Availability of related technical literature
- Development environment specifications (for example, specifications for third-party tools and components, host computers, power plugs, AC supply voltages, and so forth)
- Network requirements

In addition, trademarks, registered trademarks, export restrictions, and other legal issues may also vary from country to country.

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