Switching Regulator IC for Buck Converter

Current Mode Control w/ 40V/2.5A MOSFET

■ GENERAL DESCRIPTION

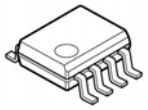
The **NJW4128** is a buck converter with **40V/2.5A** MOSFET. It corresponds to high oscillating frequency, and Low ESR Output Capacitor (MLCC) within wide input range from 4.5V to 40V.

Therefore, the **NJW4128** can realize downsizing of applications with a few external parts so that adopts current mode control.

Also, it has a soft start function, external clock synchronization, over current protection and thermal shutdown circuit.

It is suitable for supplying power to a Car Accessory, Office Automation Equipment, Industrial Instrument and so on.

■ PACKAGE OUTLINE



NJW4128GM1

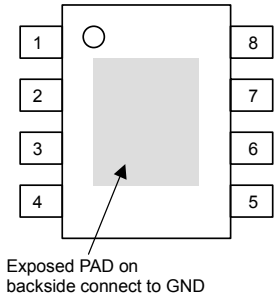
■ FEATURES

- Current Mode Control
- External Clock Synchronization
- Wide Operating Voltage Range 4.5V to 40V
- Switching Current 3.6A min.
- PWM Control
- Built-in Compensation Circuit
- Correspond to Ceramic Capacitor (MLCC)
- Oscillating Frequency 450kHz typ. (A ver.)
  300kHz typ. (B ver.)
- Soft Start Function 4ms typ.
- UVLO (Under Voltage Lockout)
- Over Current Protection (Hiccup type)
- Thermal Shutdown Protection
- Power Good Function
- Standby Function
- Package Outline NJW4128GM1 : HSOP8

■ PRODUCT CLASSFICATION

Part Number	Version	Oscillation Frequency	Power Good	Package	Operating Temperature Range
NJW4128GM1-A	A	450kHz typ.	√	HSOP8	-40°C to +85°C
NJW4128GM1-B	B	300kHz typ.	√	HSOP8	-40°C to +85°C

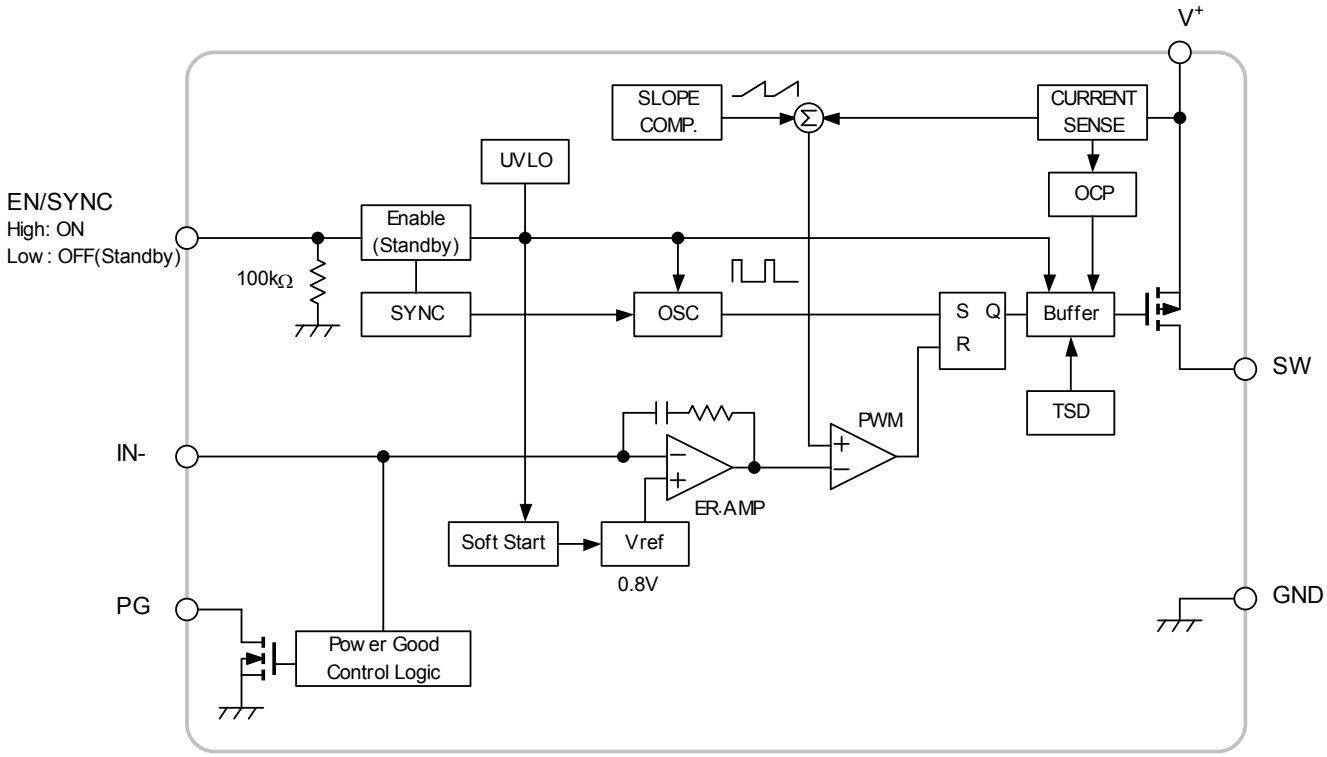
■ PIN CONFIGURATION



PIN FUNCTION
1. SW
2. SW
3. GND
4. PG
5. IN-
6. EN/SYNC
7. V^+
8. V^+

NJW4128GM1-A
NJW4128GM1-B

■ BLOCK DIAGRAM



■ ABSOLUTE MAXIMUM RATINGS (Ta=25°C)

PARAMETER	SYMBOL	MAXIMUM RATINGS	UNIT
Supply Voltage	V^+	+45	V
V^+- SW pin Voltage	V_{V-SW}	+45	V
EN/SYNC pin Voltage	$V_{EN/SYNC}$	+45	V
IN- pin Voltage	V_{IN-}	-0.3 to +6	V
Power Good pin Voltage (*1)	V_{PG}	-0.3 to +6	V
Power Dissipation	P_D	HSOP8 790 (*1) 2,500 (*2)	mW
Junction Temperature Range	Tj	-40 to +150	°C
Operating Temperature Range	T_{opr}	-40 to +85	°C
Storage Temperature Range	T_{stg}	-40 to +150	°C

(*1): Mounted on glass epoxy board. (76.2×114.3×1.6mm:based on EIA/JDEC standard, 2Layers)

(*2): Mounted on glass epoxy board. (76.2×114.3×1.6mm:based on EIA/JDEC standard, 4Layers)

(For 4Layers: Applying 74.2×74.2mm inner Cu area and a thermal via hall to a board based on JEDEC standard JESD51-5)

■ RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Supply Voltage	V^+	4.5	–	40	V
Power Good pin Voltage	V_{PG}	0	–	5.5	V
External Clock Input Range					
A version	f_{SYNC}	440	–	600	kHz
B version		280	–	500	

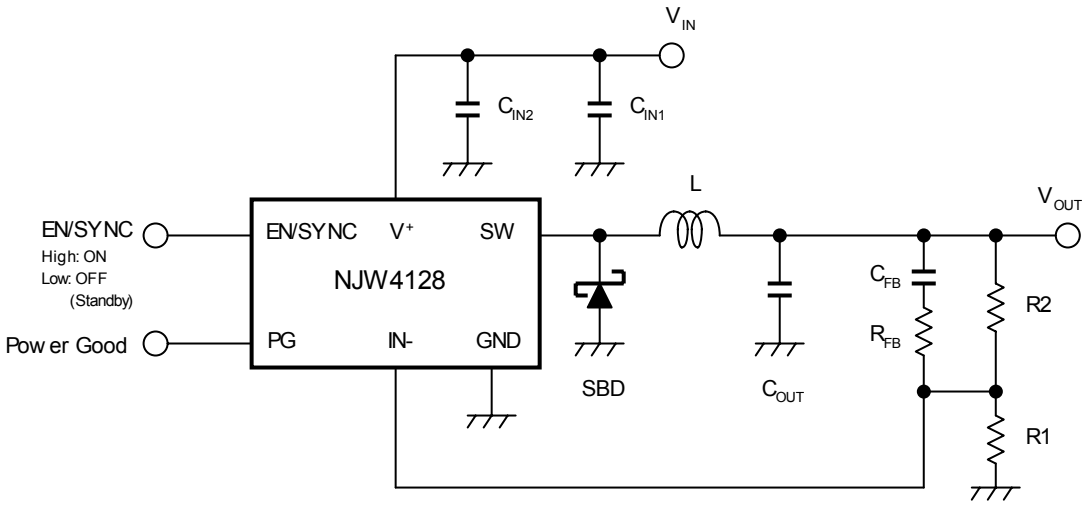
■ ELECTRICAL CHARACTERISTICS (Unless otherwise noted, V^+=$V_{EN./SYNC}$=12V, Ta=25°C)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Under Voltage Lockout Block						
ON Threshold Voltage	V_{T_ON}	V^+= L → H	4.2	4.4	4.5	V
OFF Threshold Voltage	V_{T_OFF}	V^+= H → L	4.1	4.3	4.4	V
Hysteresis Voltage	V_{HYS}		70	90	–	mV
Soft Start Block						
Soft Start Time	T_{SS}	V_B=0.75V	2	4	8	ms
Oscillator Block						
Oscillation Frequency	f_{OSC}	A version, V_{IN-}=0.7V	405	450	495	kHz
		B version, V_{IN-}=0.7V	270	300	330	kHz
Oscillation Frequency deviation (Supply voltage)	f_{DV}	V^+=4.5V to 40V	–	1	–	%
Oscillation Frequency deviation (Temperature)	f_{DT}	Ta=-40°C to +85°C	–	5	–	%
Error Amplifier Block						
Reference Voltage	V_B		-1.0%	0.8	+1.0%	V
Input Bias Current	I_B		-0.1	–	+0.1	μA
PWM Comparate Block						
Maximum Duty Cycle	$M_{AX}D_{UTY}$	V_{IN-}=0.7V	88	92	–	%
Minimum ON Time1 (Use Built-in Oscillator)	$t_{ON-min1}$	A version	–	220	300	ns
		B version	–	250	340	ns
Minimum ON Time2 (Use Ext CLK)	$t_{ON-min2}$	A version, f_{SYNC}=500kHz	–	150	220	ns
		B version, f_{SYNC}=400kHz	–	170	250	ns
OCP Block						
COOL DOWN Time	t_{COOL}		–	25	–	ms
Output Block						
Output ON Resistance	R_{ON}	I_{SW}=2.5A	–	0.15	0.3	Ω
Switching Current Limit	I_{LIM}		3.6	4.6	5.5	A
SW Leak Current	I_{LEAK}	$V_{EN/SYNC}$=0V, V^+=45V, V_{SW}=0V	–	–	4	μA

■ ELECTRICAL CHARACTERISTICS (Unless otherwise noted, $V^+=V_{EN/SYNC}$=12V, Ta=25°C)

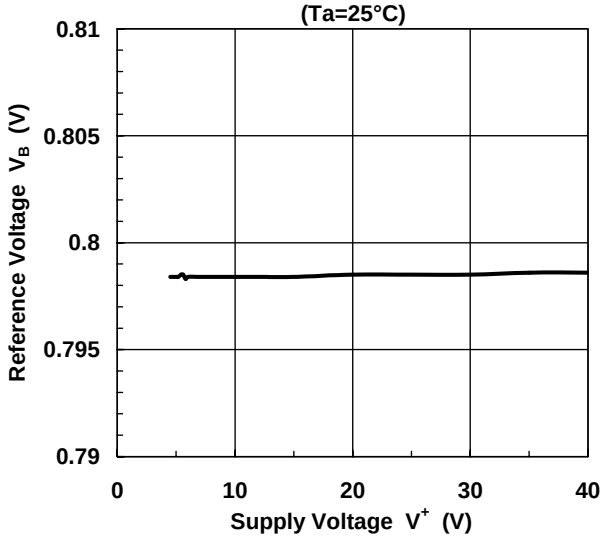
PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Standby Control / Sync Block						
EN/SYNC pin High Threshold Voltage	$V_{THH\_EN/SYNC}$	$V_{EN/SYNC}$= L → H	1.6	–	V^+	V
EN/SYNC pin Low Threshold Voltage	$V_{THL\_EN/SYNC}$	$V_{EN/SYNC}$= H → L	0	–	0.5	V
Input Bias Current (EN/SYNC pin)	I_{EN}	$V_{EN/SYNC}$=12V	–	170	250	μA
Power Good Block						
High Level Detection Voltage	V_{THH_PG}	Measured at IN- pin	105	110	115	%
High Level Detection Voltage	V_{THL_PG}	Measured at IN- pin	85	90	95	%
Hysterisis Region	V_{HYS_PG}		–	2	–	%
Power Good ON Resistance	R_{ON_PG}	I_{PG}=10mA	–	37	50	Ω
Leak Current at OFF State	I_{LEAK_PG}	V_{PG}=6V	–	–	0.1	μA
General Characteristics						
Quiescent Current	I_{DD}	A version, R_L=no load, V_{IN-}=0.7V	–	4	4.7	mA
		B version, R_L=no load, V_{IN-}=0.7V	–	3.5	4.2	mA
Standby Current	I_{DD_STB}	$V_{EN/SYNC}$=0V	–	–	3	μA

■ TYPICAL APPLICATIONS

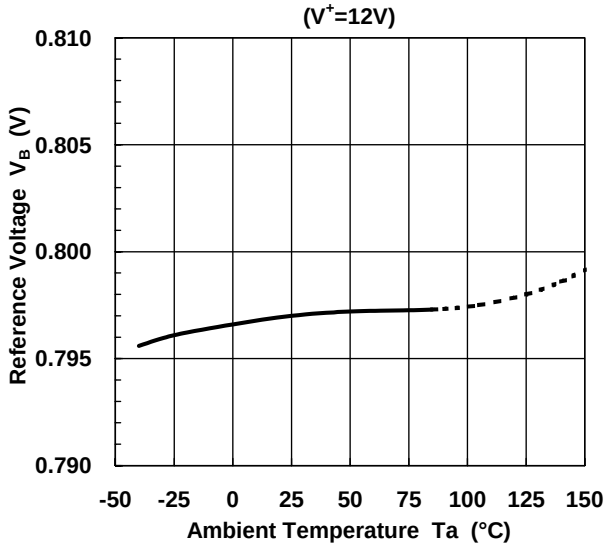


■ TYPICAL CHARACTERISTICS (A, B version)

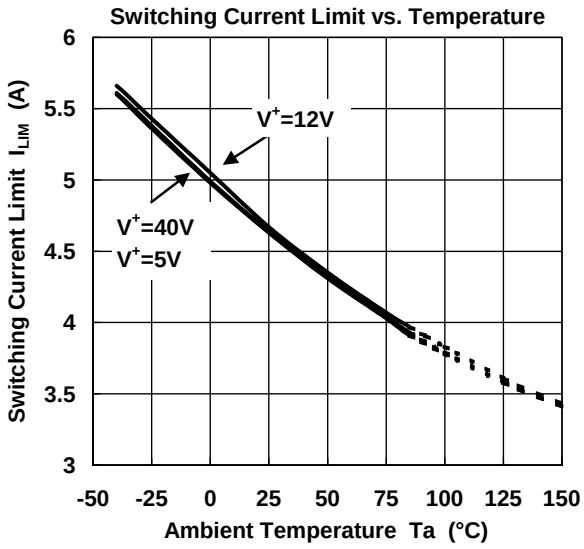
Reference Voltage vs. Supply Voltage
(Ta=25°C)



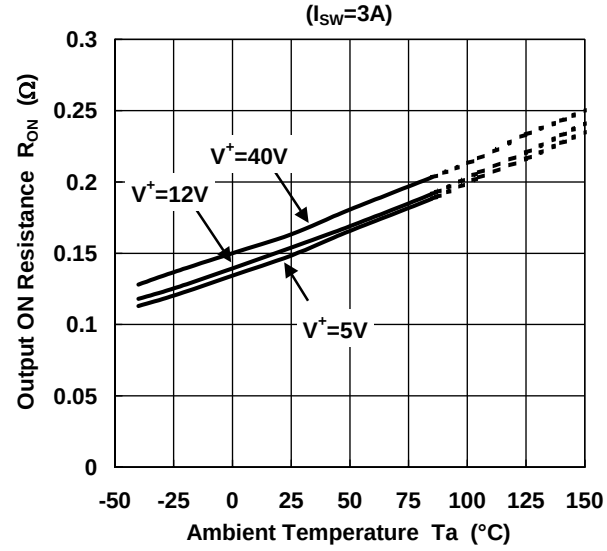
Reference Voltage vs. Temperature
(V^+=12V)



Switching Current Limit vs. Temperature

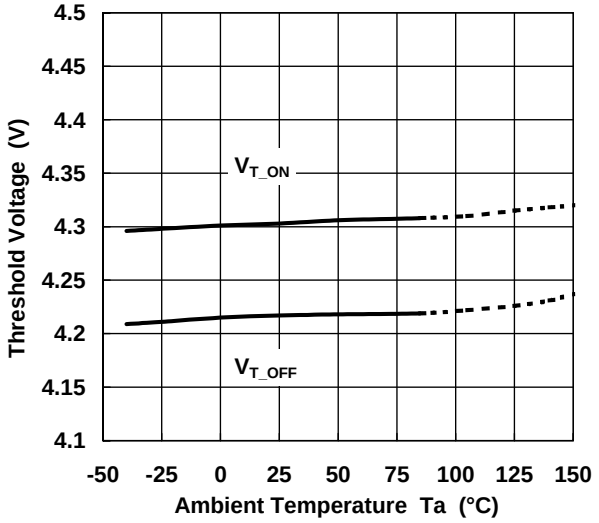


Output ON Resistance vs. Temperature
(I_{SW}=3A)

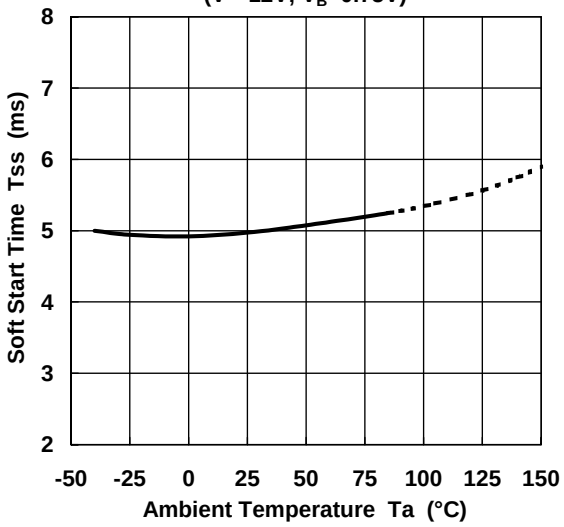


■ TYPICAL CHARACTERISTICS (A, B version)

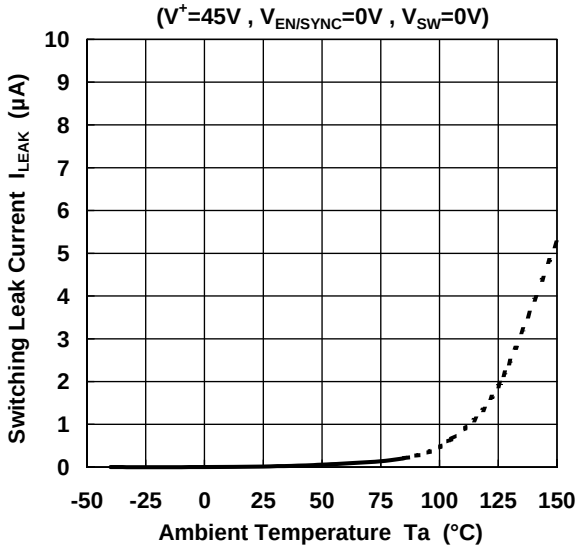
Under Voltage Lockout Voltage vs. Temperature



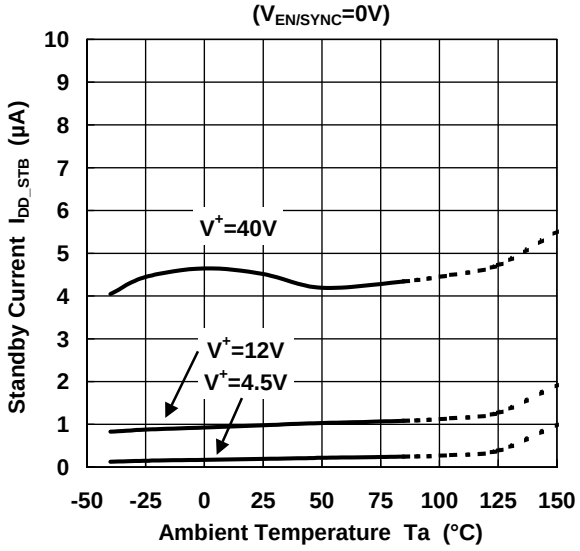
Soft Start Time vs. Temperature
(V^+=12V, V_B=0.75V)



Switching Leak Current vs. Temperature
(V^+=45V , $V_{EN/SYNC}$=0V , V_{SW}=0V)

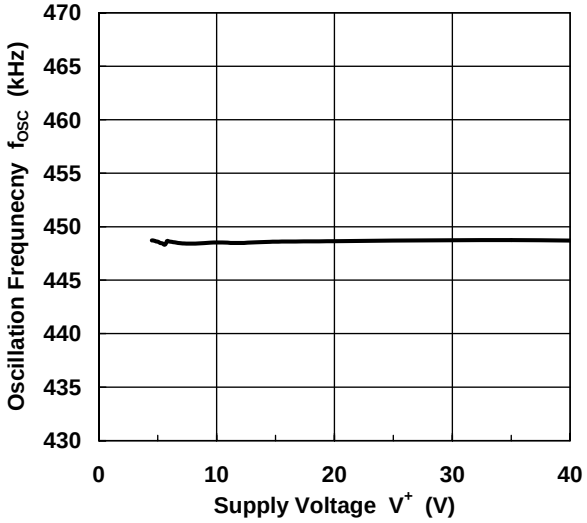


Standby Current vs. Temperature
($V_{EN/SYNC}$=0V)

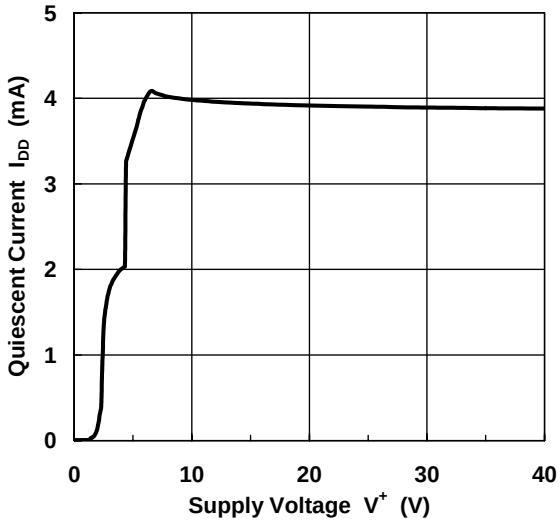


■ TYPICAL CHARACTERISTICS (A version)

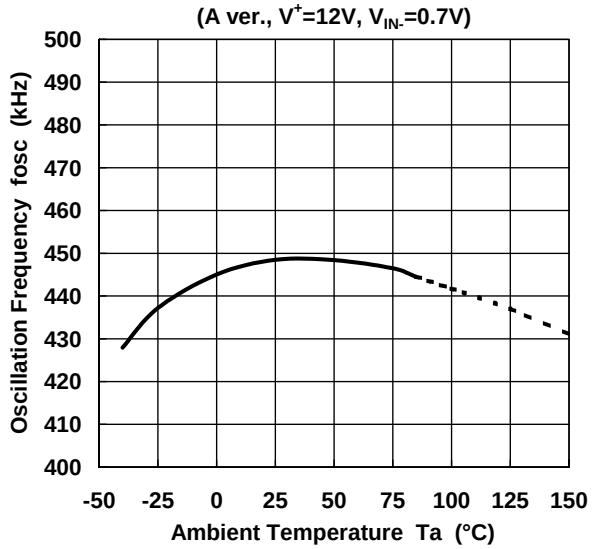
Oscillation Frequency vs. Supply Voltage
(A ver., V_{IN-}=0.7V, Ta=25°C)



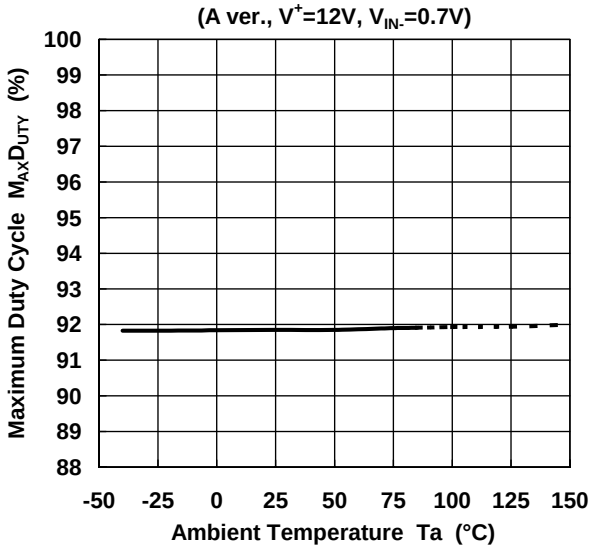
Quiescent Current vs. Supply Voltage
(A ver., R_L=no load, V_{IN-}=0.7V, Ta=25°C)



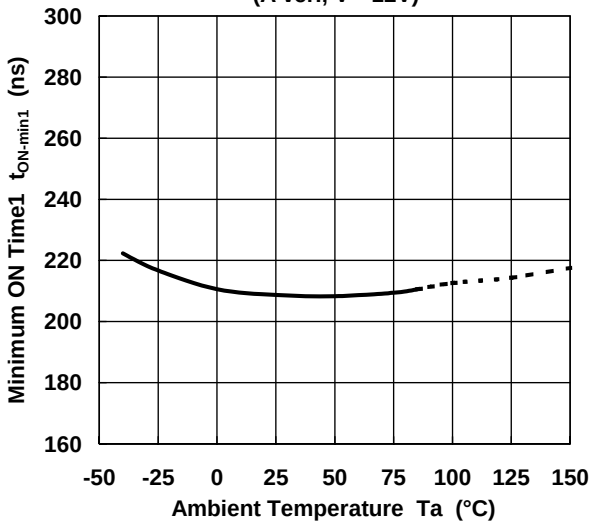
Oscillation Frequency vs Temperature
(A ver., V^+=12V, V_{IN-}=0.7V)



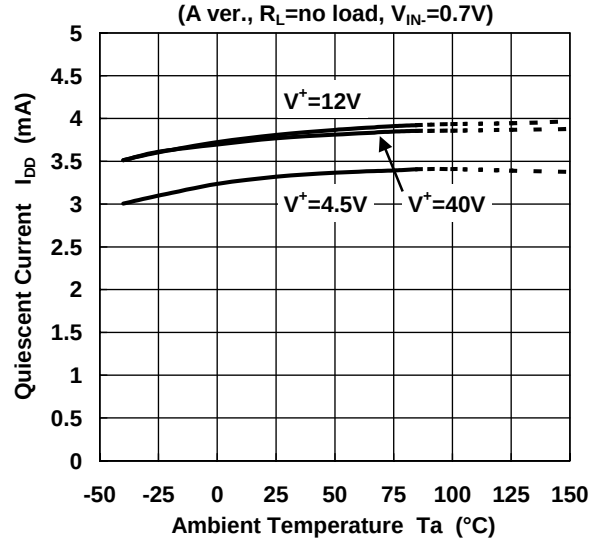
Maximum Duty Cycle vs. Temperature
(A ver., V^+=12V, V_{IN-}=0.7V)



Minimum ON Time1 vs. Temperature
(A ver., V^+=12V)

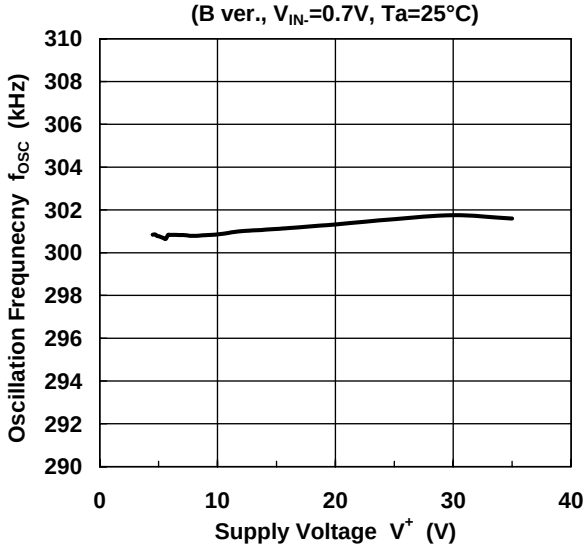


Quiescent Current vs. Temperature
(A ver., R_L=no load, V_{IN-}=0.7V)

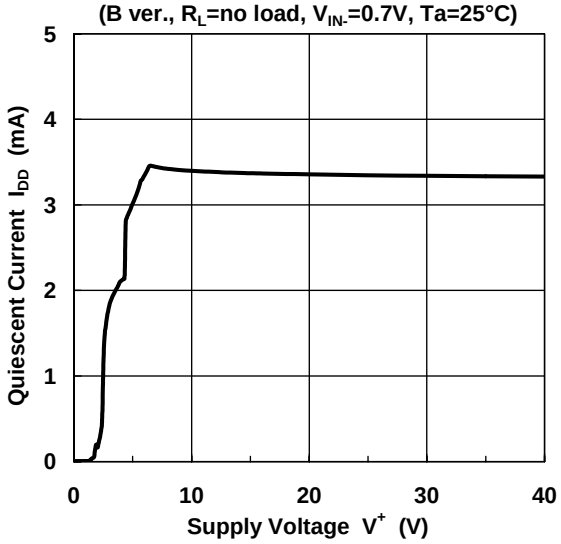


■ TYPICAL CHARACTERISTICS (B version)

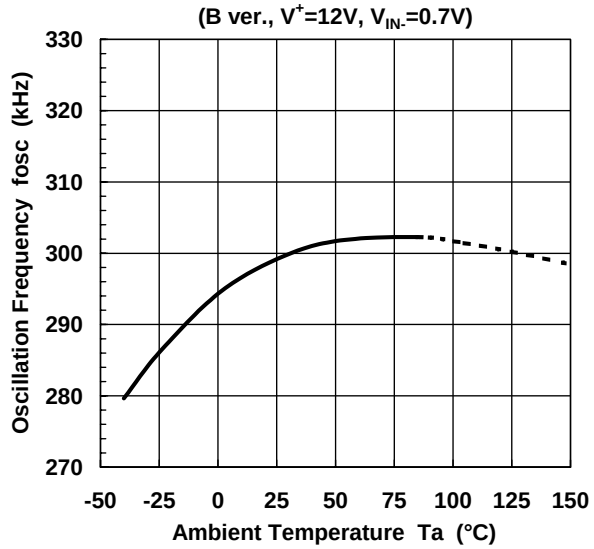
Oscillation Frequency vs. Supply Voltage
(B ver., V_{IN-}=0.7V, Ta=25°C)



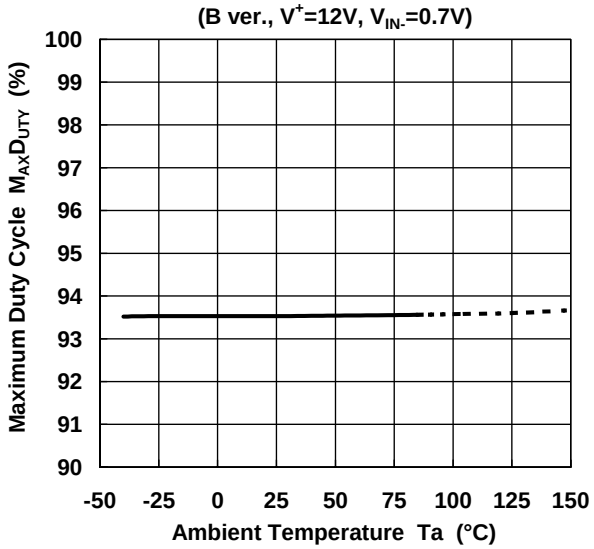
Quiescent Current vs. Supply Voltage
(B ver., R_L=no load, V_{IN-}=0.7V, Ta=25°C)



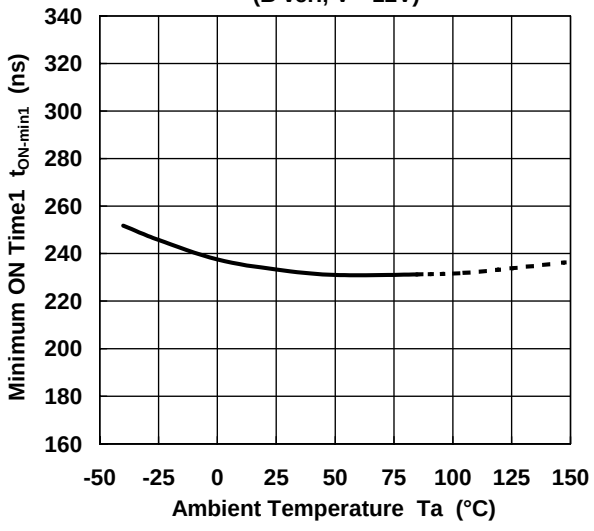
Oscillation Frequency vs Temperature
(B ver., V^+=12V, V_{IN-}=0.7V)



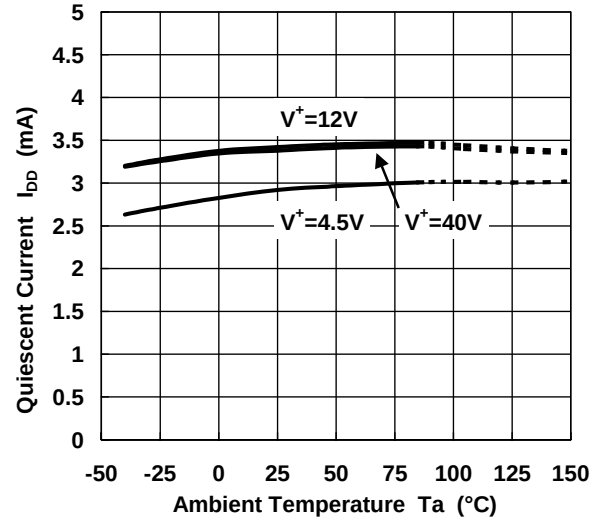
Maximum Duty Cycle vs. Temperature
(B ver., V^+=12V, V_{IN-}=0.7V)



Minimum ON Time1 vs. Temperature
(B ver., V^+=12V)



Quiescent Current vs. Temperature
(B ver., R_L=no load, V_{IN-}=0.7V)



■ PIN DESCRIPTIONS

PIN NAME	PIN NUMBER	FUNCTION
SW	1 2	Switch Output pin of Power MOSFET
GND	3	GND pin
PG	4	Power Good pin. An open drain output that goes high impedance when the IN- pin voltage is stable around ±10%.
IN-	5	Output Voltage Detecting pin Connects output voltage through the resistor divider tap to this pin in order to voltage of the IN- pin become 0.8V.
EN/SYNC	6	Standby Control pin The EN/SYNC pin internally pulls down with 100kΩ. Normal Operation at the time of High Level. Standby Mode at the time of Low Level or OPEN. Moreover, it operates by inputting clock signal at the oscillatory frequency that synchronized with the input signal.
V^+	7 8	Power Supply pin for Power Line
Exposed PAD	–	Connect to GND

■ Description of Block Features

1. Basic Functions / Features

● Error Amplifier Section (ER·AMP)

0.8V±1% precise reference voltage is connected to the non-inverted input of this section.

To set the output voltage, connects converter's output to inverted input of this section (IN- pin). If requires output voltage over 0.8V, inserts resistor divider.

Because the optimized compensation circuit is built-in, the application circuit can be composed of minimum external parts.

● PWM Comparator Section (PWM), Oscillation Circuit Section (OSC)

The NJW4128 uses a constant frequency, current mode step down architecture. The oscillation frequency is 450kHz (typ.) at A version and 300kHz (typ.) at B version. The PWM signal is output by feedback of output voltage and slope compensation switching current at the PWM comparator block.

The maximum duty ratio is 92% (typ.).

Table 1. Minimum ON time of NJW4128

	A version (f_{OSC} =450kHz)	B version (f_{OSC} =300kHz)
Use Built-in Oscillator	220ns typ.	250ns typ.
Use External Clock	150ns typ. (@ f_{SYNC}=500kHz)	170ns typ. (@ f_{SYNC}=400kHz)

The buck converter of ON time is decided the following formula.

$$ton = \frac{V_{OUT}}{V_{IN} \times f_{OSC}} [s]$$

V_{IN} shows input voltage and V_{OUT} shows output voltage.

When the ON time becomes below in $t_{ON\text{-}min}$, in order to maintain output voltage at a stable state, change of duty or pulse skip operation may be performed.

● Power MOSFET (SW Output Section)

The power is stored in the inductor by the switch operation of built-in power MOSFET. The output current is limited to 3.6A(min.) the overcurrent protection function. In case of step-down converter, the forward direction bias voltage is generated with inductance current that flows into the external regenerative diode when MOSFET is turned off.

The SW pin allows voltage between the PV^+ pin and the SW pin up to +45V. However, you should use an Schottky diode that has low saturation voltage.

● Power Supply, GND pin (V^+ and GND)

In line with switching element drive, current flows into the IC according to frequency. If the power supply impedance provided to the power supply circuit is high, it will not be possible to take advantage of IC performance due to input voltage fluctuation. Therefore insert a bypass capacitor close to the V^+ pin – the GND pin connection in order to lower high frequency impedance.

■ Description of Block Features (Continued)

2. Additional and Protection Functions / Features

● Under Voltage Lockout (UVLO)

The UVLO circuit operating is released above V^+=4.4V(typ.) and IC operation starts. When power supply voltage is low, IC does not operate because the UVLO circuit operates. There is 90mV(typ.) width hysteresis voltage at rise and decay of power supply voltage. Hysteresis prevents the malfunction at the time of UVLO operating and releasing.

● Soft Start Function (Soft Start)

The output voltage of the converter gradually rises to a set value by the soft start function. The soft start time is 4ms (typ.). It is defined with the time of the error amplifier reference voltage becoming from 0V to 0.75V. The soft start circuit operates after the release UVLO and/or recovery from thermal shutdown.

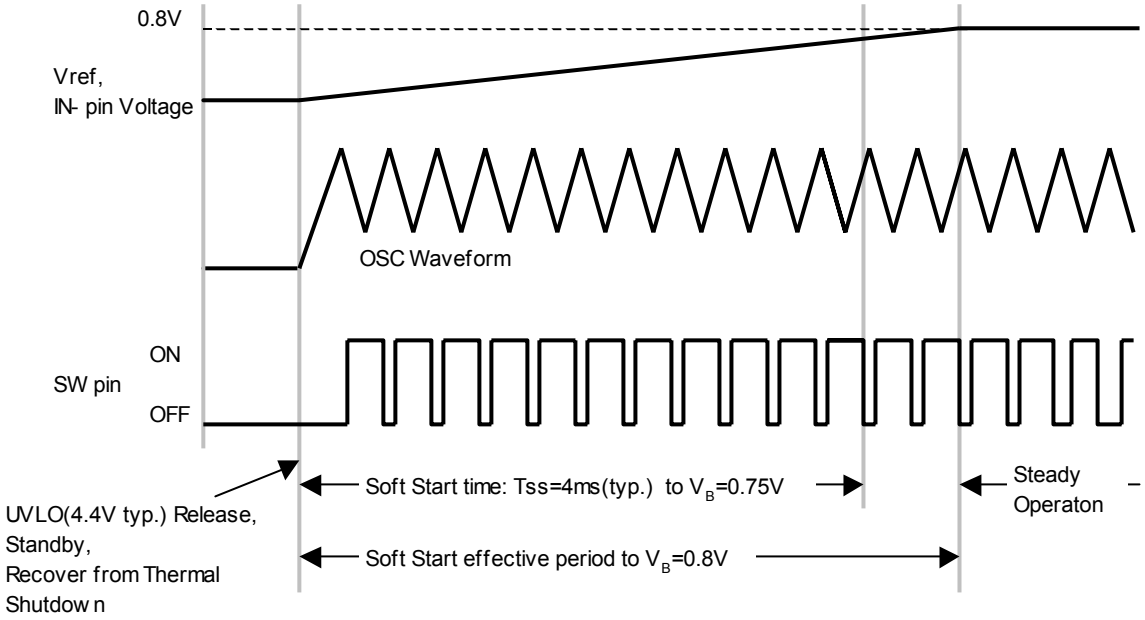


Fig. 1. Startup Timing Chart

■ Description of Block Features (Continued)

● Over Current Protection Circuit (OCP)

NJW4128 contains overcurrent protection circuit of hiccup architecture. The overcurrent protection circuit of hiccup architecture is able to decrease heat generation at the overload.

The NJW4128 output returns automatically along with release from the over current condition.

At when the switching current becomes I_{LIM} or more, the overcurrent protection circuit is stopped the MOSFET output. The switching output holds low level down to next pulse output at OCP operating.

At the same time starts pulse counting, and stops the switching operation when the overcurrent detection continues approx 1ms.

After NJW4128 switching operation was stopped, it restarts by soft start function after the cool down time of approx 25ms (typ.).

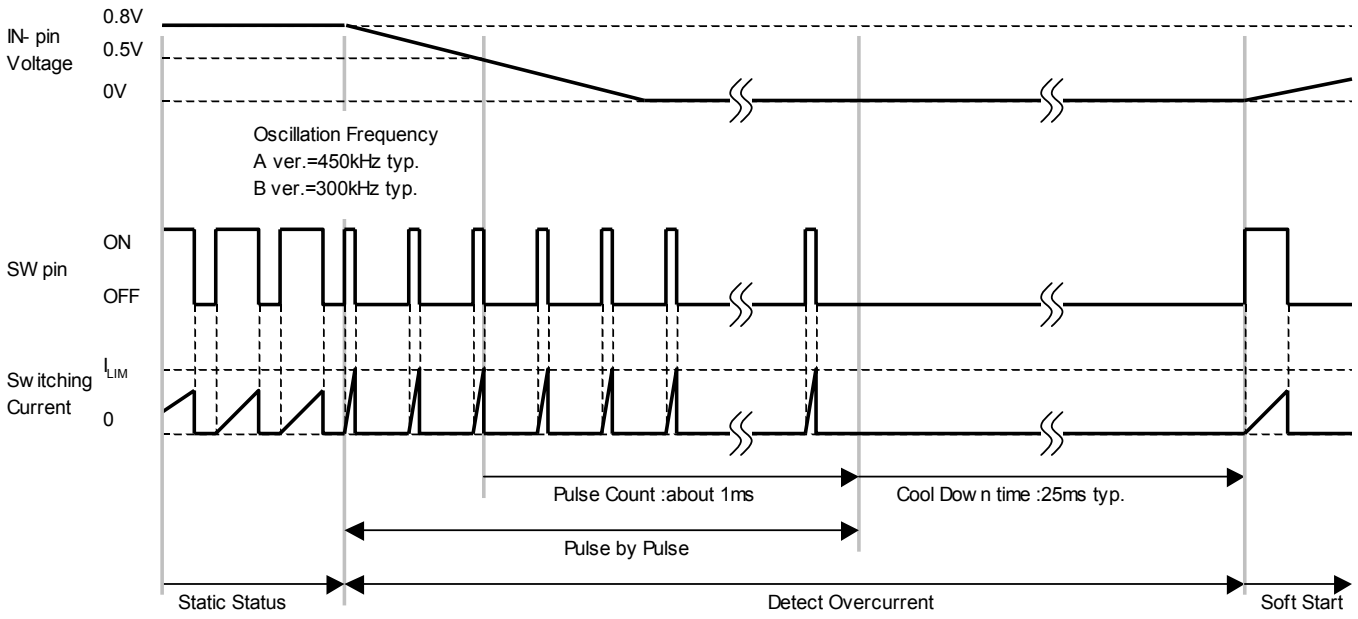


Fig. 2. Timing Chart at Over Current Detection

● Thermal Shutdown Function (TSD)

When Junction temperature of the NJW4128 exceeds the 160°C*, internal thermal shutdown circuit function stops SW function. When junction temperature decreases to 145°C* or less, SW operation returns with soft start operation.

The purpose of this function is to prevent malfunctioning of IC at the high junction temperature. Therefore it is not something that urges positive use. You should make sure to operate within the junction temperature range rated (150°C). (* Design value)

● Standby Function

The NJW4128 stops the operating and becomes standby status when the EN/SYNC pin becomes less than 0.5V.

The EN/SYNC pin internally pulls down with 100kΩ, therefore the NJW4128 becomes standby mode when the EN/SYNC pin is OPEN. You should connect this pin to V^+ when you do not use standby function.

■ Description of Block Features (Continued)

● External Clock Synchronization

By inputting a square wave to EN/SYNC pin, can be synchronized to an external frequency.
You should fulfill the following specification about a square wave. (Table 2.)

Table 2. The input square wave to an EN/SYNC pin.

	A version (f_{OSC} =450kHz)	B version (f_{OSC} =300kHz)
Input Frequency	440kHz to 600kHz	280kHz to 500kHz
Duty Cycle	25% to 75%	20% to 80%
Voltage magnitude	1.6V or more at High level 0.5V or less at Low level	

The trigger of the switching operating at the external synchronized mode is detected to the rising edge of the input signal. At the time of switching operation from standby or asynchronous to synchronous operation, it has set a delay time approx 20μs to 30μs in order to prevent malfunctions. (Fig. 3.)

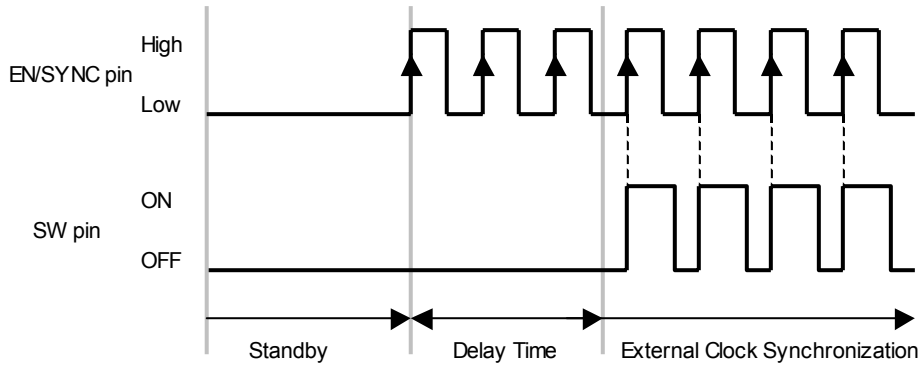


Fig. 3. Switching Operation by External Synchronized Clock

● Power Good Function

It monitors the output status and outputs a signal from PG pin that internally connected to open drain MOSFET.

The Power Good pin goes high impedance when the IN- pin voltage is stable around ±10%(typ.) of error amplifier reference voltage.

A low on the pin indicates that the IN- pin voltage is out of the setting voltage.

To prevent malfunction of the Power Good output, it has hysterisis 2%(typ.) and the delay time approx 20μs to 30μs against the IN- pin voltage changes.

■ Application Information

● Inductors

Because a large current flows to the inductor, you should select the inductor with the large current capacity not to saturate. Optimized inductor value is determined by the input voltage and output voltage.

The Inductor setting example is shown in Table 3.

Table 3. Inductor Setting Example (A ver.)

Input Voltage V_{IN}	Output Voltage V_{OUT}	Inductor L
12V	3.3V	≤ 6.8μH
	5.0V	≤ 10μH
	8.0V	≤ 10μH
24V	3.3V	≤ 10μH
	5.0V	≤ 12μH
	8.0V	≤ 12μH

When increasing inductor value, it is necessary to increasing capacity of an output capacitor and to secure the stability of application. The minimum of inductor value is restricted from the following formula, when ON duty exceeds 50%.

$$L \geq \frac{V_{IN} \times (2 \times D_{ON} - 1)}{2.3} \text{ [μH]}$$

Reducing L decreases the size of the inductor. However a peak current increases and adversely affects the efficiency. (Fig. 4.)

Moreover, you should be aware that the output current is limited because it becomes easy to operating to the overcurrent limit.

The peak current is decided the following formula.

$$\Delta I_L = \frac{(V_{IN} - V_{OUT}) \times V_{OUT}}{L \times V_{IN} \times f_{OSC}} \text{ [A]}$$

$$Ipk = I_{OUT} + \frac{\Delta I_L}{2} \text{ [A]}$$

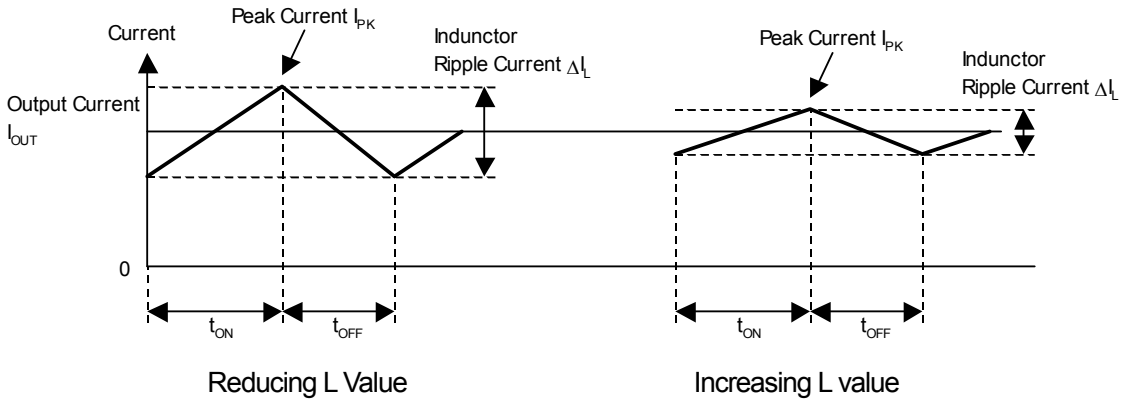


Fig. 4. Inductor Current State Transition (Continuous Conduction Mode)

■ Application Information (Continued)

● Input Capacitor

Transient current flows into the input section of a switching regulator responsive to frequency. If the power supply impedance provided to the power supply circuit is large, it will not be possible to take advantage of the NJW4128 performance due to input voltage fluctuation. Therefore insert an input capacitor as close to the MOSFET as possible. A ceramic capacitor is the optimal for input capacitor.

The effective input current can be expressed by the following formula.

$$I_{RMS} = I_{OUT} \times \frac{\sqrt{V_{OUT} \times (V_{IN} - V_{OUT})}}{V_{IN}} \text{ [A]}$$

In the above formula, the maximum current is obtained when $V_{IN} = 2 \times V_{OUT}$, and the result in this case is $I_{RMS} = I_{OUT(MAX)} \div 2$.

When selecting the input capacitor, carry out an evaluation based on the application, and use a capacitor that has adequate margin.

● Output Capacitor

An output capacitor stores power from the inductor, and stabilizes voltage provided to the output.

Because NJW4128 corresponds to the output capacitor of low ESR, the ceramic capacitor is the optimal for compensation. The output capacitor setting example is shown in Table 4.

Table 4. Output Capacitor Setting Example (A ver.)

Input Voltage V_{IN}	Output Voltage V_{OUT}	Output Capacitor C_{OUT}	Part Number
12V, 24V	3.3V	≥ 47μF×2 / 6.3V	GRM31CB30J476KE18: Murata
	5.0V	≥ 22μF×2 / 6.3V	GRM31CB30J226ME18: Murata
	8.0V	≥ 22μF×2 / 16V	GRM32EB31E226KE15: Murata

The output capacitor uses capacity bigger than Table 4.

In addition, you should consider varied characteristics of capacitor (a frequency characteristic, a temperature characteristic, a DC bias characteristic and so on) and unevenness peculiar to a capacitor supplier enough.

Therefore when selecting a capacitors, you should confirm the characteristics with supplier datasheets.

When selecting an output capacitor, you must consider Equivalent Series Resistance (ESR) characteristics, ripple current, and breakdown voltage.

The output ripple noise can be expressed by the following formula.

$$V_{ripple(p-p)} = ESR \times \Delta I_L \text{ [V]}$$

The effective ripple current that flows in a capacitor (I_{rms}) is obtained by the following equation.

$$I_{rms} = \frac{\Delta I_L}{2\sqrt{3}} \text{ [Arms]}$$

■ Application Information (Continued)

● Catch Diode

When the switch element is in OFF cycle, power stored in the inductor flows via the catch diode to the output capacitor. Therefore during each cycle current flows to the diode in response to load current. Because diode's forward saturation voltage and current accumulation cause power loss, a Schottky Barrier Diode (SBD), which has a low forward saturation voltage, is ideal.

An SBD also has a short reverse recovery time. If the reverse recovery time is long, through current flows when the switching transistor transitions from OFF cycle to ON cycle. This current may lower efficiency and affect such factors as noise generation.

● Setting Output Voltage, Compensation Capacitor

The output voltage V_{OUT} is determined by the relative resistances of R1, R2. The current that flows in R1, R2 must be a value that can ignore the bias current that flows in ER AMP.

$$V_{OUT} = \left(\frac{R2}{R1} + 1\right) \times V_B \text{ [V]}$$

The zero points are formed with R2 and C_{FB}, and it makes for the phase compensation of NJW4128. The zero point is shown the following formula.

$$f_{Z1} = \frac{1}{2 \times \pi \times R2 \times C_{FB}} \text{ [Hz]}$$

You should set the zero point as a guide from 50kHz to 70kHz.

Output voltage setting Resistor and compensation capacitor setting example is shown in Table 5.

Table 5. Output Voltage Setting Resistor and Compensation Capacitor Setting Example

Input Voltage V_{IN}	Output Voltage V_{OUT}	R1	R2	C_{FB}
12V, 24V	3.3V	4.7kΩ	15kΩ	180pF
	5.0V	3kΩ	16kΩ	180pF
	8.0V	3.9kΩ	36kΩ	82pF

■ Application Information (Continued)

● Board Layout

In the switching regulator application, because the current flow corresponds to the oscillation frequency, the substrate (PCB) layout becomes an important.

You should attempt the transition voltage decrease by making a current loop area minimize as much as possible. Therefore, you should make a current flowing line thick and short as much as possible. Fig.5. shows a current loop at step-down converter. Especially, should lay out high priority the loop of C_{IN}-SW-SBD that occurs rapid current change in the switching. It is effective in reducing noise spikes caused by parasitic inductance.

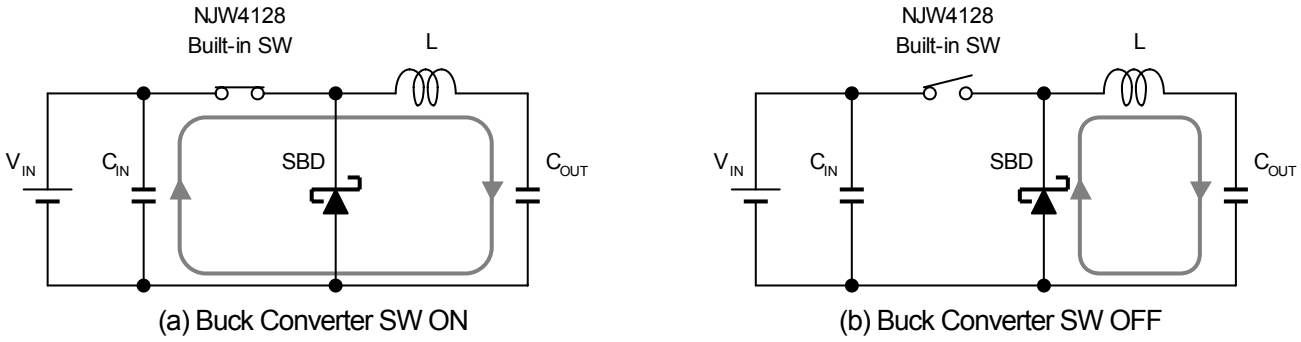


Fig. 5. Current Loop at Buck Converter

Concerning the GND line, it is preferred to separate the power system and the signal system, and use single ground point.

The voltage sensing feedback line should be as far away as possible from the inductance. Because this line has high impedance, it is laid out to avoid the influence noise caused by flux leaked from the inductance.

Fig. 6. shows example of wiring at buck converter. Fig. 7 shows the PCB layout example.

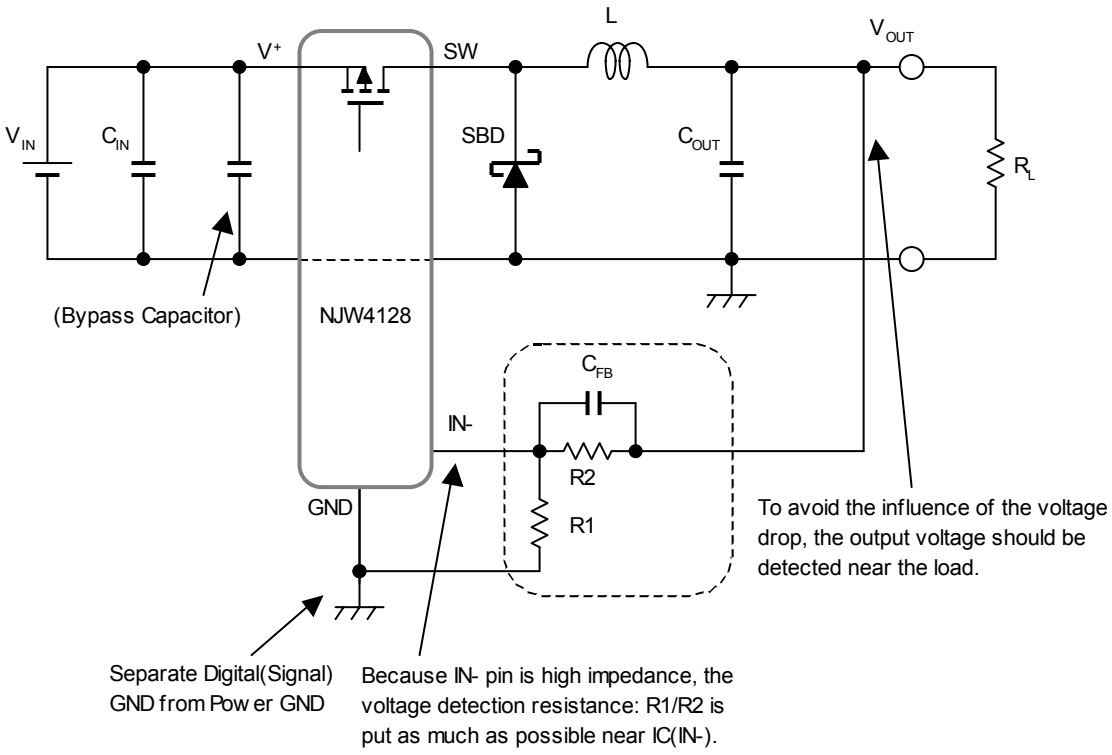
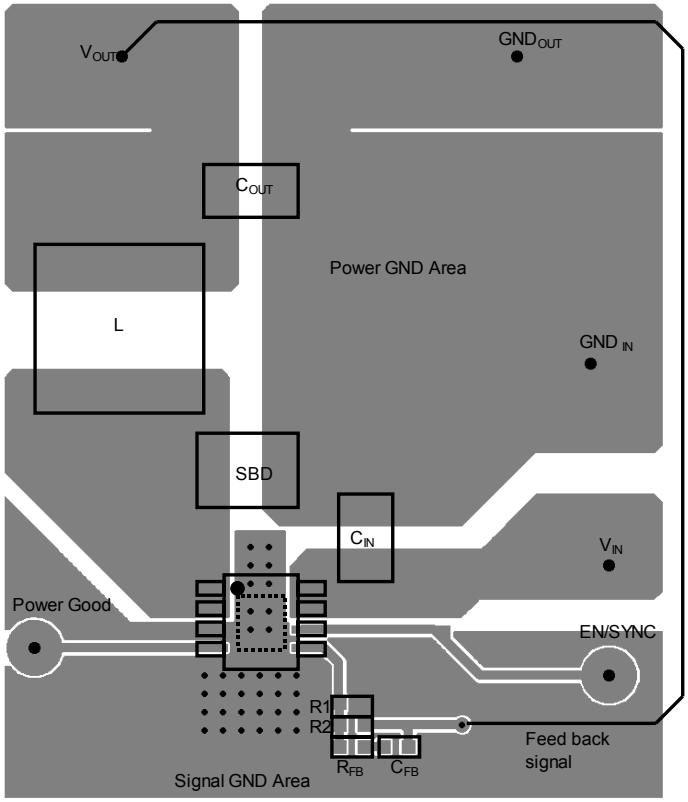


Fig. 6. Board Layout at Buck Converter

■ Application Information (Continued)



Connect Signal GND line and Power GND line on backside pattern

Fig. 7. Layout Example (upper view)

■ Calculation of Package Power

A lot of the power consumption of buck converter occurs from the internal switching element (Power MOSFET). Power consumption of NJW4128 is roughly estimated as follows.

Input Power: $P_{IN} = V_{IN} \times I_{IN}$ [W]
Output Power: $P_{OUT} = V_{OUT} \times I_{OUT}$ [W]
Diode Loss: $P_{DIODE} = V_F \times I_{L(avg)} \times$ OFF duty [W]
NJW4128 Power Consumption: $P_{LOSS} = P_{IN} - P_{OUT} - P_{DIODE}$ [W]

Where:

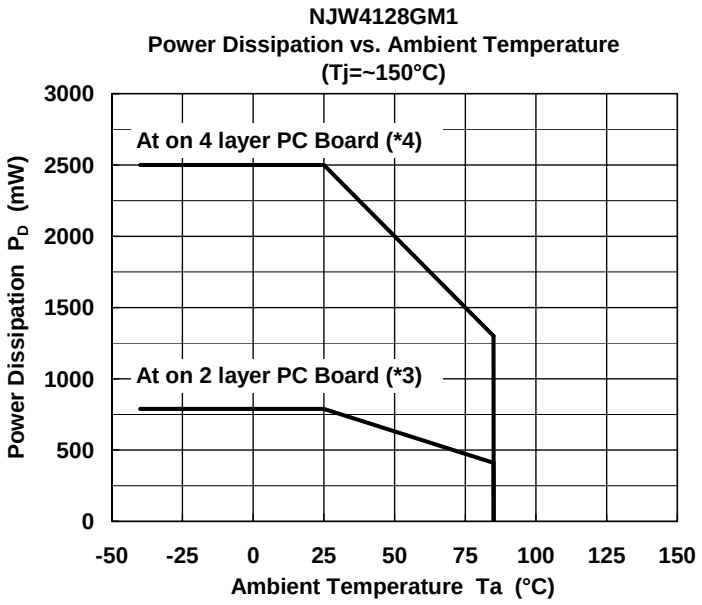
V_{IN}	: Input Voltage for Converter	I_{IN}	: Input Current for Converter
V_{OUT}	: Output Voltage of Converter	I_{OUT}	: Output Current of Converter
V_F	: Diode's Forward Saturation Voltage	$I_{L(avg)}$	: Inductor Average Current
OFF duty	: Switch OFF Duty		

Efficiency (η) is calculated as follows.

$\eta = (P_{OUT} \div P_{IN}) \times 100$ [%]

You should consider temperature derating to the calculated power consumption: P_D.

You should design power consumption in rated range referring to the power dissipation vs. ambient temperature characteristics (Fig. 8).



(*3): Mounted on glass epoxy board. (76.2×114.3×1.6mm:based on EIA/JDEC standard, 2Layers)
(*4): Mounted on glass epoxy board. (76.2×114.3×1.6mm:based on EIA/JDEC standard, 4Layers)
(For 4Layers: Applying 74.2×74.2mm inner Cu area and a thermal via hall to a board based on JEDEC standard JESD51-5)

Fig. 8. Power Dissipation vs. Ambient Temperature Characteristics