

# NP40N10YDF, NP40N10VDF, NP40N10PDF

100 V – 40 A – N-channel Power MOS FET Application: Automotive

R07DS0361EJ0201 Rev.2.01 May 13, 2013

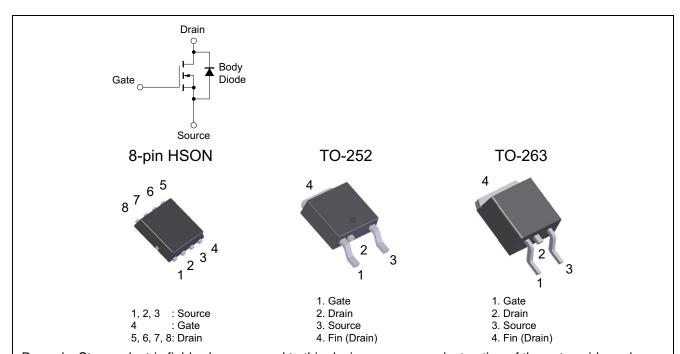
## **Description**

These products are N-channel MOS Field Effect Transistors designed for high current switching applications.

#### **Features**

- Low on-state resistance
  - $R_{DS(on)} = 25 \text{ m}\Omega \text{ MAX.}$  ( $V_{GS} = 10 \text{ V}$ ,  $I_D = 20 \text{ A}$ ) (NP40N10YDF)
  - --- R<sub>DS(on)</sub> = 26 mΩ MAX. (V<sub>GS</sub> = 10 V, I<sub>D</sub> = 20 A) (NP40N10VDF)
  - ---  $R_{DS(on)} = 27 \text{ m}\Omega \text{ MAX.}$  ( $V_{GS} = 10 \text{ V}$ ,  $I_D = 20 \text{ A}$ ) (NP40N10PDF)
- Low  $C_{iss}$ :  $C_{iss} = 2100 \text{ pF TYP}$ .  $(V_{DS} = 25 \text{ V}, V_{GS} = 0 \text{ V})$
- Logic level drive type
- Designed for automotive application and AEC-Q101 qualified

## **Outline**



Remark: Strong electric field, when exposed to this device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred.

## **Ordering Information**

Part No.	Lead Plating	Pac	Package	
NP40N10YDF-E1-AY *1	Pure Sn (Tin)	Tape 2500 p/reel	Taping (E1 type)	8-pin HSON
NP40N10YDF-E2-AY *1			Taping (E2 type)	
NP40N10VDF-E1-AY *1	Pure Sn (Tin)	Tape 2500 p/reel	Taping (E1 type)	TO-252 (MP-3ZP)
NP40N10VDF-E2-AY *1			Taping (E2 type)	
NP40N10PDF-E1-AY *1	Pure Sn (Tin)	Tape 800 p/reel	Taping (E1 type)	TO-263 (MP-25ZP)
NP40N10PDF-E2-AY *1			Taping (E2 type)	

Note: \*1. Pb-free (This product does not contain Pb in the external electrode)

## **Absolute Maximum Ratings** $(T_A = 25^{\circ}C)$

Item	Symbol	Ratings	Unit
Drain to Source Voltage (V <sub>GS</sub> = 0 V)	V <sub>DSS</sub>	100	V
Gate to Source Voltage (V <sub>DS</sub> = 0 V)	V <sub>GSS</sub>	±20	V
Drain Current (DC) (T <sub>C</sub> = 25°C)	I <sub>D(DC)</sub>	±40	А
Drain Current (pulse) *1	I <sub>D(pulse)</sub>	±80	А
Total Power Dissipation (T <sub>C</sub> = 25°C)	P <sub>T1</sub>	120	W
NP40N10YDF	P <sub>T2</sub>	1.0	W
Total Power Dissipation ( $T_A = 25^{\circ}C$ ) *2			
NP40N10VDF		1.2	
Total Power Dissipation ( $T_A = 25^{\circ}C$ ) *2			
NP40N10PDF		1.8	
Total Power Dissipation (T <sub>A</sub> = 25°C)			
Channel Temperature	T <sub>ch</sub>	175	°C
Storage Temperature	T <sub>stg</sub>	-55 to +175	°C
Single Avalanche Current *3	I <sub>AS</sub>	25	А
Single Avalanche Energy *3	E <sub>AS</sub>	61	mJ

## **Thermal Resistance**

Channel to Case Thermal Resistance	$R_{th(ch-C)}$		1.25	°C/W
Channel to Ambient Thermal Resistance *2	$R_{th(ch-A)}$	NP40N10YDF	150	°C/W
		NP40N10VDF	125	°C/W
		NP40N10PDF	83.3	°C/W

Notes: \*1.  $T_C$  = 25°C, PW  $\leq$  10  $\mu$ s, Duty Cycle  $\leq$  1%

<sup>\*2.</sup> Mounted on glass epoxy substrate of 40 mm  $\times$  40 mm  $\times$  1.6 mmt with 4% copper area (35  $\mu\text{m})$ 

<sup>\*3.</sup>  $T_{ch(start)}$  = 25°C,  $V_{DD}$  = 50 V,  $R_G$  = 25  $\Omega$ , L = 100  $\mu$ H,  $V_{GS}$  = 20 V  $\rightarrow$  0 V

## **Electrical Characteristics** (T<sub>A</sub> = 25°C)

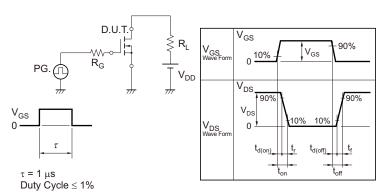
Item		Symbol	Min	Тур	Max	Unit	Test Conditions
Zero Gate Voltage Drain Current		I <sub>DSS</sub>			1	μΑ	$V_{DS} = 100 \text{ V}, V_{GS} = 0 \text{ V}$
Gate Leakage Current		I <sub>GSS</sub>			±100	nA	$V_{GS} = \pm 20 \text{ V}, V_{DS} = 0 \text{ V}$
Gate to Source Threshold Voltage		$V_{GS(th)}$	1.5	2.0	2.5	V	$V_{DS} = V_{GS}, I_D = 250 \mu\text{A}$
Forward Transfer	r Admittance *1	y <sub>fs</sub>	20	40		S	$V_{DS} = 5.0 \text{ V}, I_{D} = 20 \text{ A}$
Drain to Source	NP40N10YDF	R <sub>DS(on)1</sub>		21	25	mΩ	$V_{GS} = 10 \text{ V}, I_D = 20 \text{ A}$
On-state		R <sub>DS(on)2</sub>		23	30	mΩ	$V_{GS} = 5.0 \text{ V}, I_D = 20 \text{ A}$
Resistance *1		R <sub>DS(on)3</sub>		24	36	mΩ	$V_{GS} = 4.5 \text{ V}, I_D = 20 \text{ A}$
	NP40N10VDF	R <sub>DS(on)1</sub>		21	26	mΩ	$V_{GS} = 10 \text{ V}, I_D = 20 \text{ A}$
		R <sub>DS(on)2</sub>		23	31	mΩ	$V_{GS} = 5.0 \text{ V}, I_D = 20 \text{ A}$
		R <sub>DS(on)3</sub>		24	37	mΩ	$V_{GS} = 4.5 \text{ V}, I_D = 20 \text{ A}$
	NP40N10PDF	R <sub>DS(on)1</sub>		21	27	mΩ	$V_{GS} = 10 \text{ V}, I_D = 20 \text{ A}$
		R <sub>DS(on)2</sub>		23	32	mΩ	$V_{GS} = 5.0 \text{ V}, I_D = 20 \text{ A}$
		R <sub>DS(on)3</sub>		24	38	mΩ	$V_{GS} = 4.5 \text{ V}, I_D = 20 \text{ A}$
Input Capacitance		C <sub>iss</sub>		2100	3150	pF	$V_{DS} = 25 \text{ V},$
Output Capacitance		Coss		200	300	pF	$V_{GS} = 0 V$ ,
Reverse Transfer Capacitance		C <sub>rss</sub>		80	144	pF	f = 1 MHz
Turn-on Delay Ti	Turn-on Delay Time			15	33	ns	$V_{DD} = 50 \text{ V}, I_D = 20 \text{ A},$
Rise Time		t <sub>r</sub>		16	40	ns	$V_{GS} = 10 \text{ V},$
Turn-off Delay Ti	Turn-off Delay Time			60	120	ns	$R_G = 0 \Omega$
Fall Time		t <sub>f</sub>		5	13	ns	
Total Gate Charge		$Q_G$		47	71	nC	$V_{DD} = 80 \text{ V},$
Gate to Source Charge		$Q_{GS}$		8		nC	$V_{GS} = 10 \text{ V},$
Gate to Drain Charge		$Q_{GD}$		12		nC	$I_D = 40 \text{ A}$
Body Diode Forward Voltage *1		$V_{F(S-D)}$		0.9	1.5	V	$I_F = 40 \text{ A}, V_{GS} = 0 \text{ V}$
Reverse Recove		t <sub>rr</sub>		67		ns	$I_F = 40 \text{ A}, V_{GS} = 0 \text{ V},$
Reverse Recove	ry Charge	Q <sub>rr</sub>		162		nC	di/dt = 100 A/μs

Note: \*1. Pulsed test

## **TEST CIRCUIT 1 AVALANCHE CAPABILITY**

# $V_{GS} = 20 \rightarrow 0 \text{ V}$ $V_{DD}$ $V_{DD}$ $V_{DD}$ $V_{DD}$ $V_{DD}$ $V_{DD}$ $V_{DD}$ $V_{DD}$ $V_{DS}$ $V_{DS}$ $V_{DS}$ $V_{DS}$

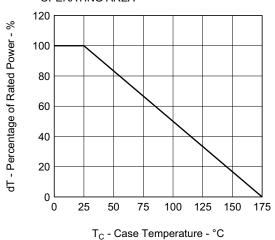
## TEST CIRCUIT 2 SWITCHING TIME



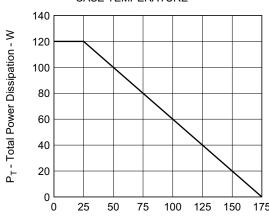
## **TEST CIRCUIT 3 GATE CHARGE**

## **Typical Characteristics** $(T_A = 25^{\circ}C)$

# DERATING FACTOR OF FORWARD BIAS SAFE OPERATING AREA

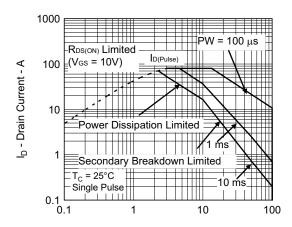


# TOTAL POWER DISSIPATION vs. CASE TEMPERATURE



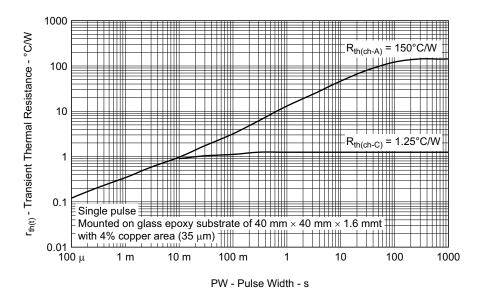
 $T_{C}$  - Case Temperature -  $^{\circ}C$ 

## FORWARD BIAS SAFE OPERATING AREA

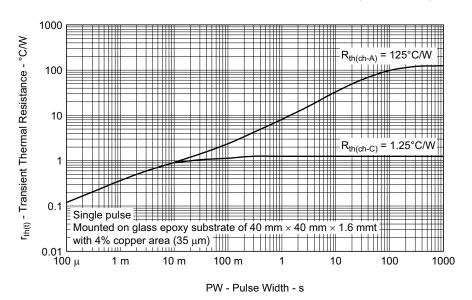


 $\mathrm{V}_{\mathrm{DS}}$  - Drain to Source Voltage - V

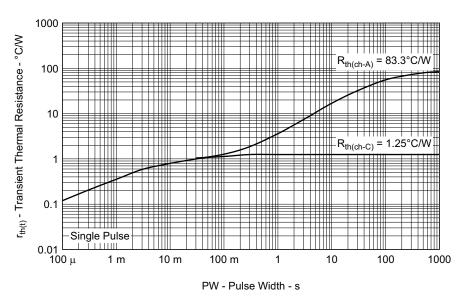
## TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH (NP40N10YDF)



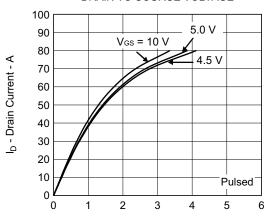
### TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH (NP40N10VDF)



## TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH (NP40N10PDF)

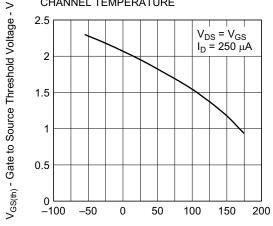


#### DRAIN CURRENT vs. DRAIN TO SOURCE VOLTAGE



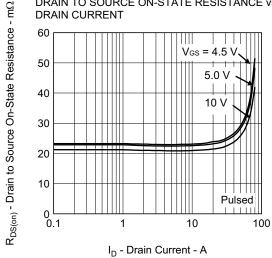
## V<sub>DS</sub> - Drain to Source Voltage - V

#### GATE TO SOURCE THRESHOLD VOLTAGE vs. CHANNEL TEMPERATURE

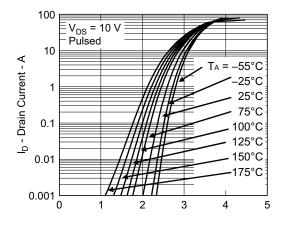


T<sub>ch</sub> - Channel Temperature - °C

#### DRAIN TO SOURCE ON-STATE RESISTANCE vs. **DRAIN CURRENT**

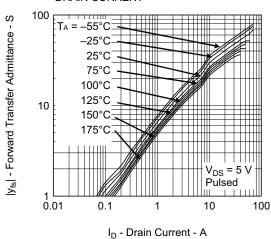


#### FORWARD TRANSFER CHARACTERISTICS

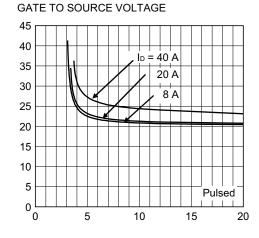


V<sub>GS</sub> - Gate to Source Voltage - V

#### FORWARD TRANSFER ADMITTANCE vs. DRAIN CURRENT



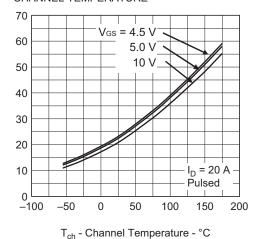
DRAIN TO SOURCE ON-STATE RESISTANCE vs.



V<sub>GS</sub> - Gate to Source Voltage - V

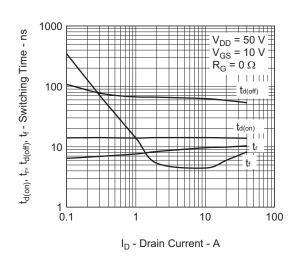
 $R_{DS(on)}$  - Drain to Source On-State Resistance -  $m\Omega$ 

# DRAIN TO SOURCE ON-STATE RESISTANCE vs. CHANNEL TEMPERATURE

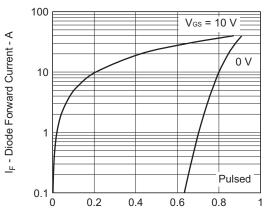


 $R_{DS(on)}$  - Drain to Source On-State Resistance -  $m\Omega$ 

## SWITCHING CHARACTERISTICS

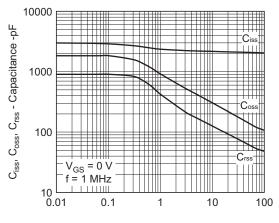


### SOURCE TO DRAIN DIODE FORWARD VOLTAGE



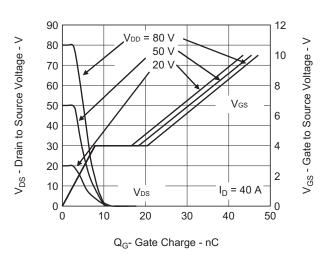
## $V_{F(S-D)}$ - Source to Drain Voltage - V

### CAPACITANCE vs. DRAIN TO SOURCE VOLTAGE

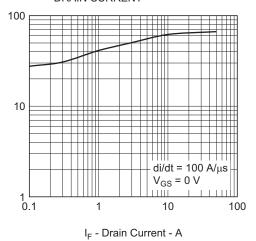


V<sub>DS</sub> - Drain to Source Voltage - V

#### DYNAMIC INPUT/OUTPUT CHARACTERISTICS



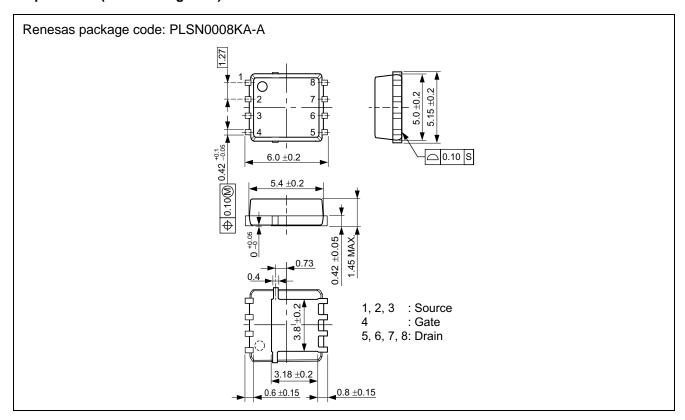
REVERSE RECOVERY TIME vs. DRAIN CURRENT



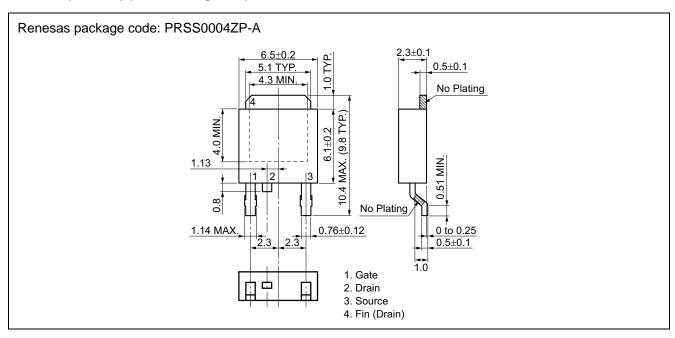
t<sub>rr</sub> - Reverse Recovery Time - ns

## Package Drawings (Unit: mm)

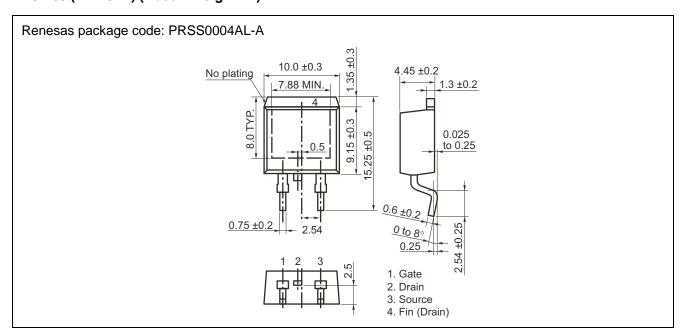
## 8-pin HSON (Mass: 0.13 g TYP.)



## TO-252 (MP-3ZP) (Mass: 0.27 g TYP.)



## TO-263 (MP-25ZP) (Mass: 1.48 g TYP.)



**Revision History** 

## NP40N10YDF, NP40N10VDF, NP40N10PDF Data Sheet

		Description		
Rev.	Date	Page	Summary	
1.00	Feb 21, 2013	_	First Edition Issued	
2.00	Mar 11, 2013	1	"Outline" added	
		7	Modification of "CAPACITANCE vs. DRAIN TO SOURCE VOLTAGE"	
2.01	May 13, 2013	1	Modification of "Outline"	
		8	Modification of "Package Drawings 8-pinHSON"	

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