RENESAS

Data Sheet

NP40N10YDF, NP40N10VDF, NP40N10PDF

100 V – 40 A – N-channel Power MOS FET
Application: Automotive

R07DS0361EJ0201
Rev.2.01
May 13, 2013

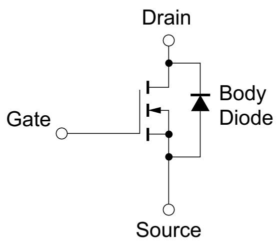
Description

These products are N-channel MOS Field Effect Transistors designed for high current switching applications.

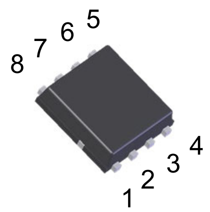
Features

- Low on-state resistance
  - $R_{DS(on)}$ = 25 mΩ MAX. (V_{GS} = 10 V, I_D = 20 A) (NP40N10YDF)
  - $R_{DS(on)}$ = 26 mΩ MAX. (V_{GS} = 10 V, I_D = 20 A) (NP40N10VDF)
  - $R_{DS(on)}$ = 27 mΩ MAX. (V_{GS} = 10 V, I_D = 20 A) (NP40N10PDF)
- Low C_{iss}: C_{iss} = 2100 pF TYP. (V_{DS} = 25 V, V_{GS} = 0 V)
- Logic level drive type
- Designed for automotive application and AEC-Q101 qualified

Outline

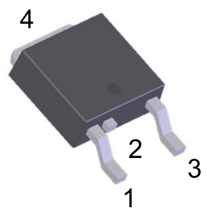


8-pin HSON



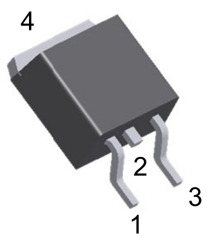
1, 2, 3 : Source
4 : Gate
5, 6, 7, 8: Drain

TO-252



1. Gate
2. Drain
3. Source
4. Fin (Drain)

TO-263



1. Gate
2. Drain
3. Source
4. Fin (Drain)

Remark: Strong electric field, when exposed to this device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred.

Ordering Information

Part No.	Lead Plating	Packing		Package
NP40N10YDF-E1-AY *1	Pure Sn (Tin)	Tape 2500 p/reel	Taping (E1 type)	8-pin HSON
NP40N10YDF-E2-AY *1			Taping (E2 type)	
NP40N10VDF-E1-AY *1	Pure Sn (Tin)	Tape 2500 p/reel	Taping (E1 type)	TO-252 (MP-3ZP)
NP40N10VDF-E2-AY *1			Taping (E2 type)	
NP40N10PDF-E1-AY *1	Pure Sn (Tin)	Tape 800 p/reel	Taping (E1 type)	TO-263 (MP-25ZP)
NP40N10PDF-E2-AY *1			Taping (E2 type)	

Note: *1. Pb-free (This product does not contain Pb in the external electrode)

Absolute Maximum Ratings (T_A = 25°C)

Item	Symbol	Ratings	Unit
Drain to Source Voltage (V_{GS} = 0 V)	V_{DSS}	100	V
Gate to Source Voltage (V_{DS} = 0 V)	V_{GSS}	±20	V
Drain Current (DC) (T_C = 25°C)	$I_{D(DC)}$	±40	A
Drain Current (pulse) *1	$I_{D(pulse)}$	±80	A
Total Power Dissipation (T_C = 25°C)	P_{T1}	120	W
NP40N10YDF Total Power Dissipation (T_A = 25°C) *2	P_{T2}	1.0	W
NP40N10VDF Total Power Dissipation (T_A = 25°C) *2		1.2	
NP40N10PDF Total Power Dissipation (T_A = 25°C)		1.8	
Channel Temperature	T_{ch}	175	°C
Storage Temperature	T_{stg}	–55 to +175	°C
Single Avalanche Current *3	I_{AS}	25	A
Single Avalanche Energy *3	E_{AS}	61	mJ

Thermal Resistance

Channel to Case Thermal Resistance	$R_{th(ch-C)}$		1.25	°C/W
Channel to Ambient Thermal Resistance *2	$R_{th(ch-A)}$	NP40N10YDF	150	°C/W
		NP40N10VDF	125	°C/W
		NP40N10PDF	83.3	°C/W

Notes: *1. T_C = 25°C, PW ≤ 10 μs, Duty Cycle ≤ 1%

*2. Mounted on glass epoxy substrate of 40 mm × 40 mm × 1.6 mmt with 4% copper area (35 μm)

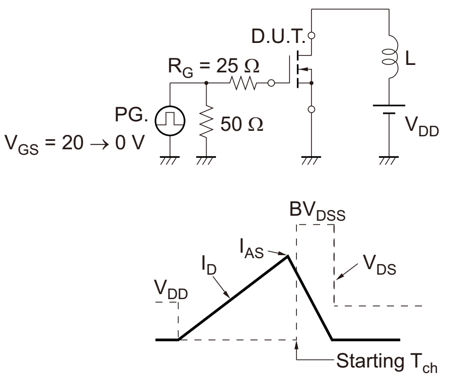
*3. $T_{ch(start)}$ = 25°C, V_{DD} = 50 V, R_G = 25 Ω, L = 100 μH, V_{GS} = 20 V → 0 V

Electrical Characteristics (T_A = 25°C)

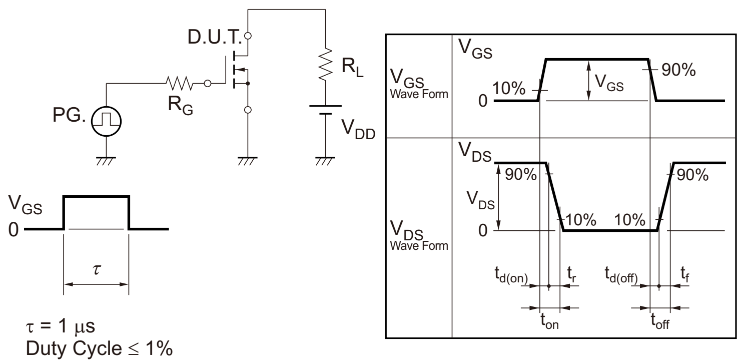
Item		Symbol	Min	Typ	Max	Unit	Test Conditions
Zero Gate Voltage Drain Current		I_{DSS}			1	μA	V_{DS} = 100 V, V_{GS} = 0 V
Gate Leakage Current		I_{GSS}			±100	nA	V_{GS} = ±20 V, V_{DS} = 0 V
Gate to Source Threshold Voltage		$V_{GS(th)}$	1.5	2.0	2.5	V	V_{DS} = V_{GS}, I_D = 250 μA
Forward Transfer Admittance *1		$\| y_{fs} \|$	20	40		S	V_{DS} = 5.0 V, I_D = 20 A
Drain to Source On-state Resistance *1	**NP40N10YDF**	$R_{DS(on)1}$		21	25	mΩ	V_{GS} = 10 V, I_D = 20 A
		$R_{DS(on)2}$		23	30	mΩ	V_{GS} = 5.0 V, I_D = 20 A
		$R_{DS(on)3}$		24	36	mΩ	V_{GS} = 4.5 V, I_D = 20 A
	NP40N10VDF	$R_{DS(on)1}$		21	26	mΩ	V_{GS} = 10 V, I_D = 20 A
		$R_{DS(on)2}$		23	31	mΩ	V_{GS} = 5.0 V, I_D = 20 A
		$R_{DS(on)3}$		24	37	mΩ	V_{GS} = 4.5 V, I_D = 20 A
	NP40N10PDF	$R_{DS(on)1}$		21	27	mΩ	V_{GS} = 10 V, I_D = 20 A
		$R_{DS(on)2}$		23	32	mΩ	V_{GS} = 5.0 V, I_D = 20 A
		$R_{DS(on)3}$		24	38	mΩ	V_{GS} = 4.5 V, I_D = 20 A
Input Capacitance		C_{iss}		2100	3150	pF	V_{DS} = 25 V,
Output Capacitance		C_{oss}		200	300	pF	V_{GS} = 0 V,
Reverse Transfer Capacitance		C_{rss}		80	144	pF	f = 1 MHz
Turn-on Delay Time		$t_{d(on)}$		15	33	ns	V_{DD} = 50 V, I_D = 20 A,
Rise Time		t_r		16	40	ns	V_{GS} = 10 V,
Turn-off Delay Time		$t_{d(off)}$		60	120	ns	R_G = 0 Ω
Fall Time		t_f		5	13	ns	
Total Gate Charge		Q_G		47	71	nC	V_{DD} = 80 V,
Gate to Source Charge		Q_{GS}		8		nC	V_{GS} = 10 V,
Gate to Drain Charge		Q_{GD}		12		nC	I_D = 40 A
Body Diode Forward Voltage *1		$V_{F(S-D)}$		0.9	1.5	V	I_F = 40 A, V_{GS} = 0 V
Reverse Recovery Time		t_{rr}		67		ns	I_F = 40 A, V_{GS} = 0 V,
Reverse Recovery Charge		Q_{rr}		162		nC	di/dt = 100 A/μs

Note: *1. Pulsed test

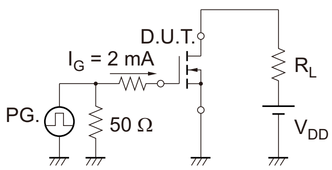
TEST CIRCUIT 1 AVALANCHE CAPABILITY



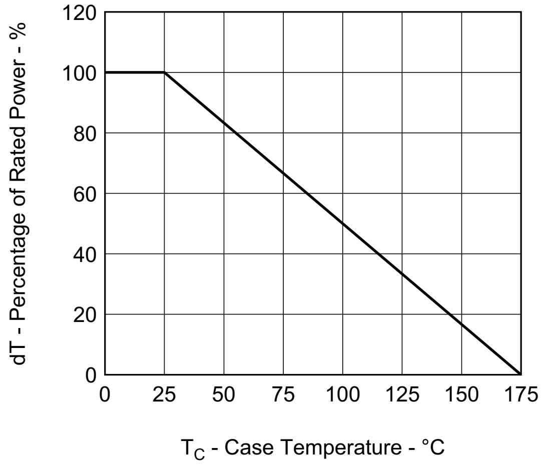
TEST CIRCUIT 2 SWITCHING TIME

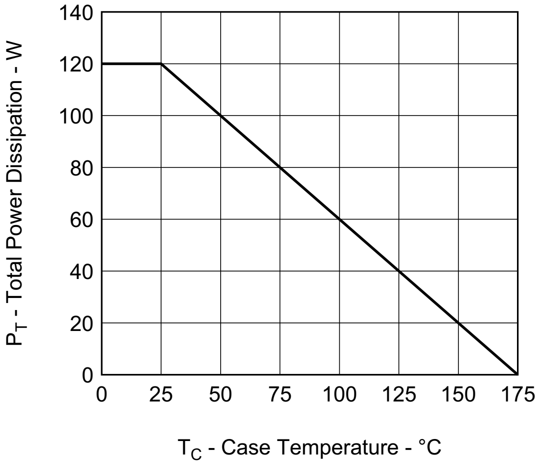


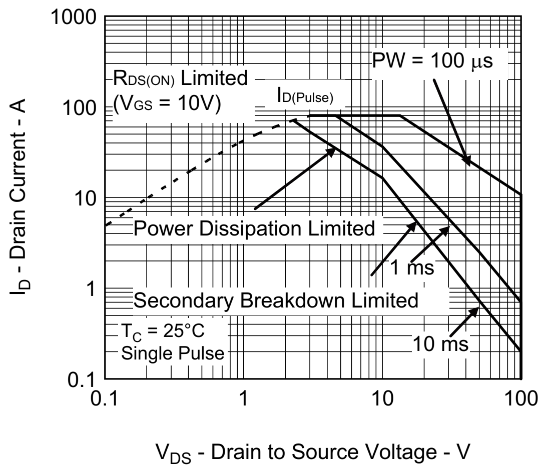
TEST CIRCUIT 3 GATE CHARGE



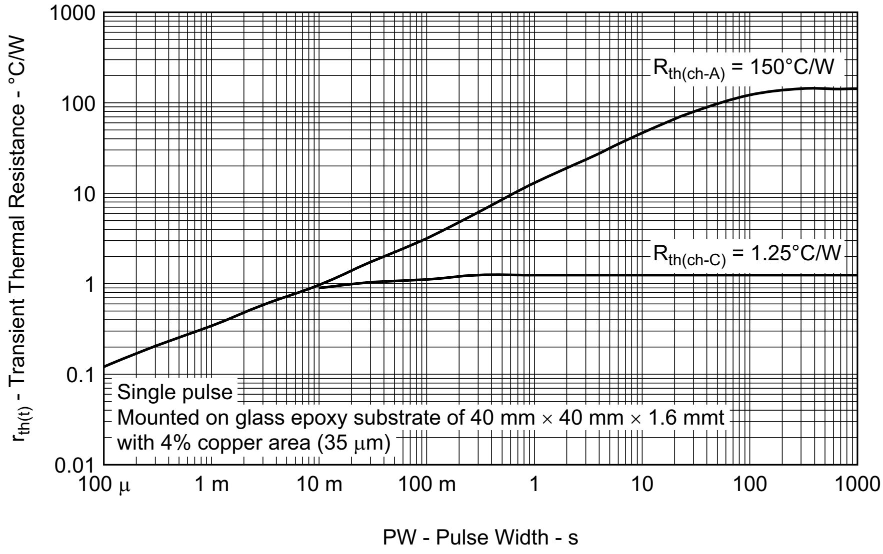
Typical Characteristics (T_A = 25°C)



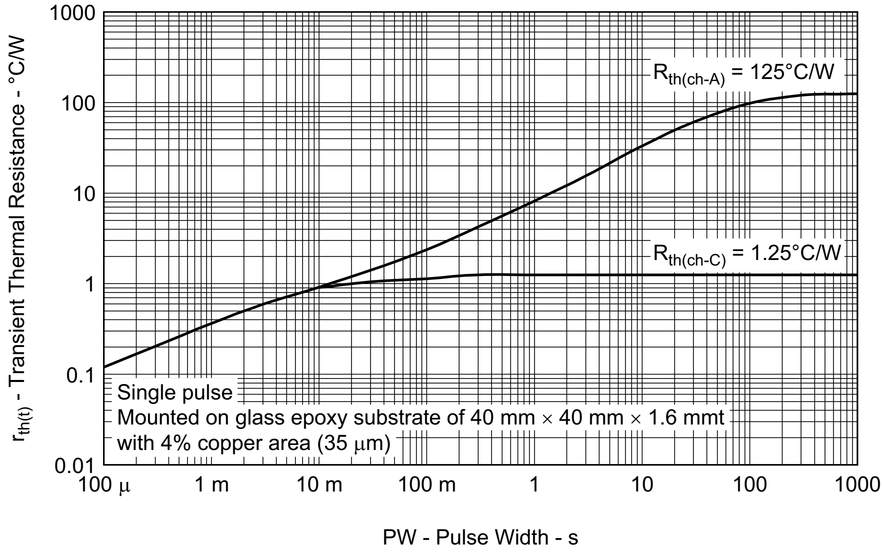




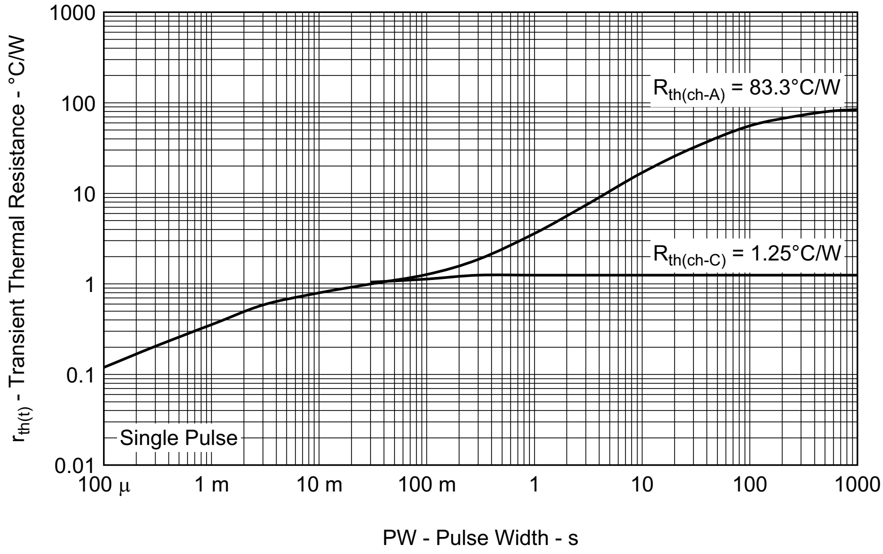
TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH (NP40N10YDF)



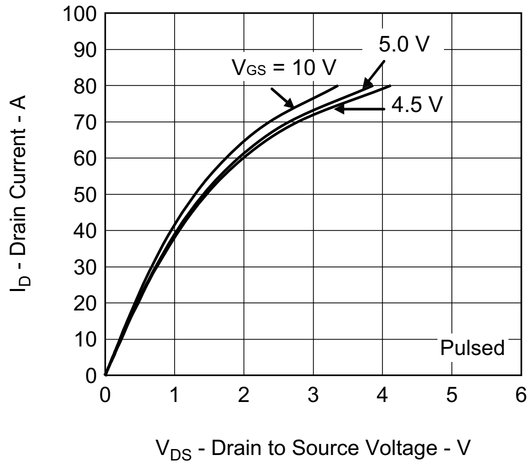
TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH (NP40N10VDF)



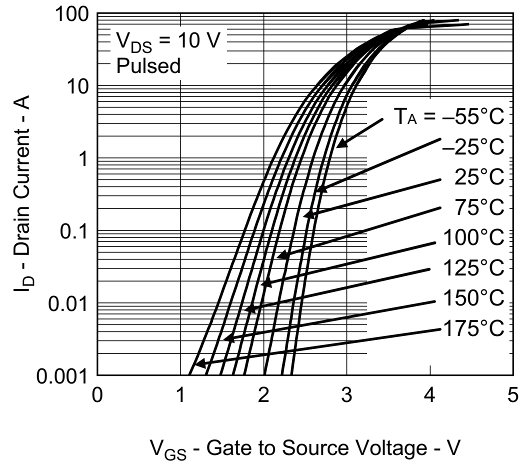
TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH (NP40N10PDF)



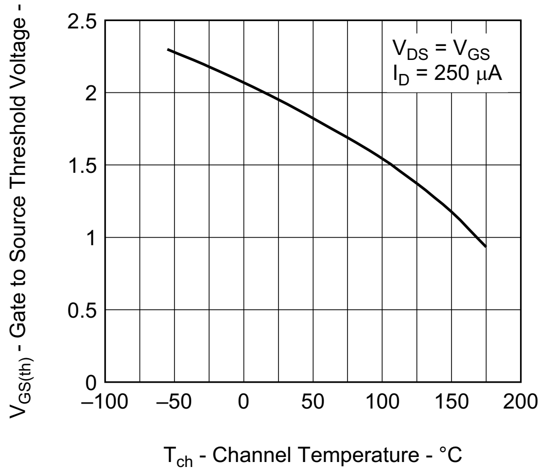
DRAIN CURRENT vs.
DRAIN TO SOURCE VOLTAGE



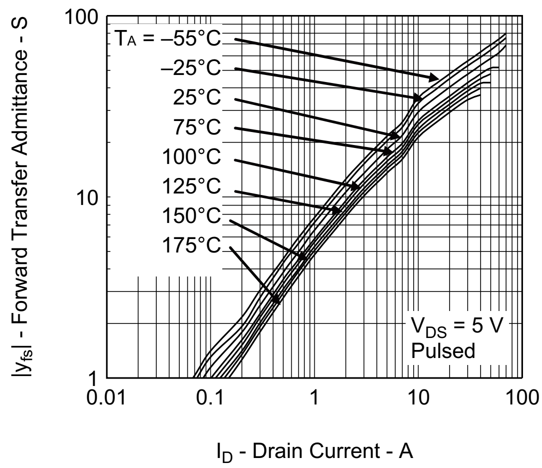
FORWARD TRANSFER CHARACTERISTICS



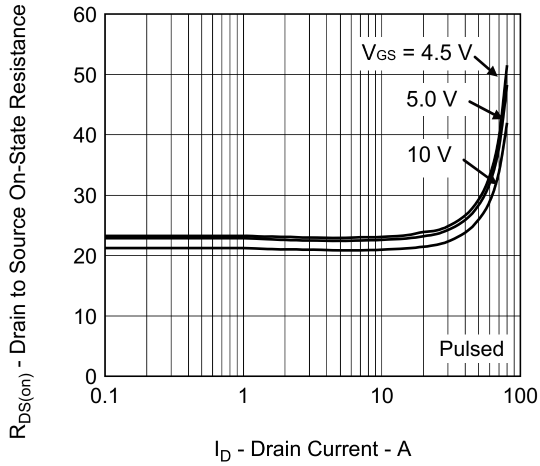
GATE TO SOURCE THRESHOLD VOLTAGE vs.
CHANNEL TEMPERATURE



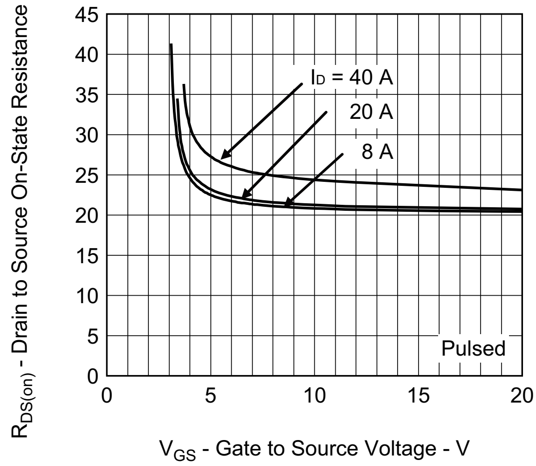
FORWARD TRANSFER ADMITTANCE vs.
DRAIN CURRENT



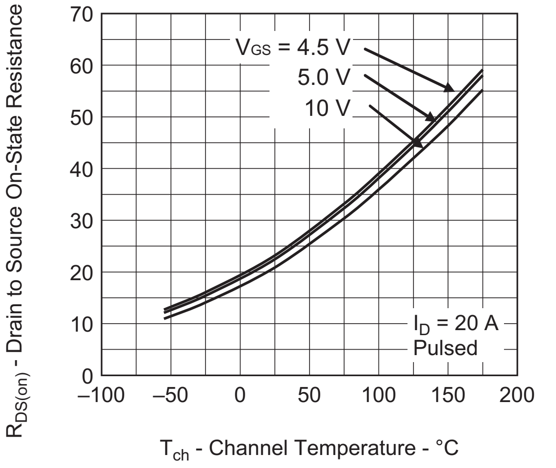
DRAIN TO SOURCE ON-STATE RESISTANCE vs.
DRAIN CURRENT



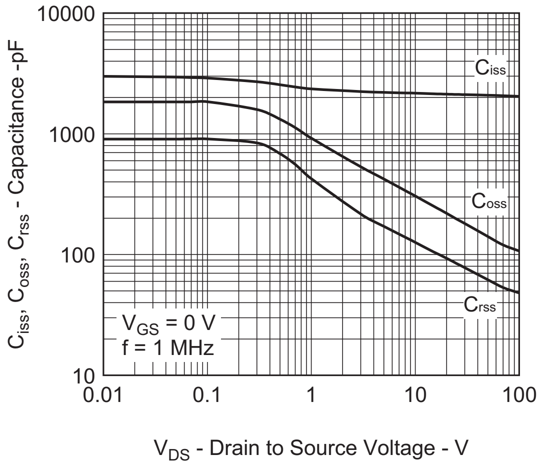
DRAIN TO SOURCE ON-STATE RESISTANCE vs.
GATE TO SOURCE VOLTAGE



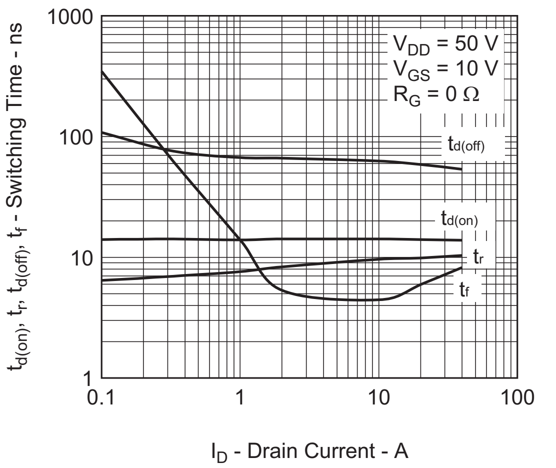
DRAIN TO SOURCE ON-STATE RESISTANCE vs. CHANNEL TEMPERATURE



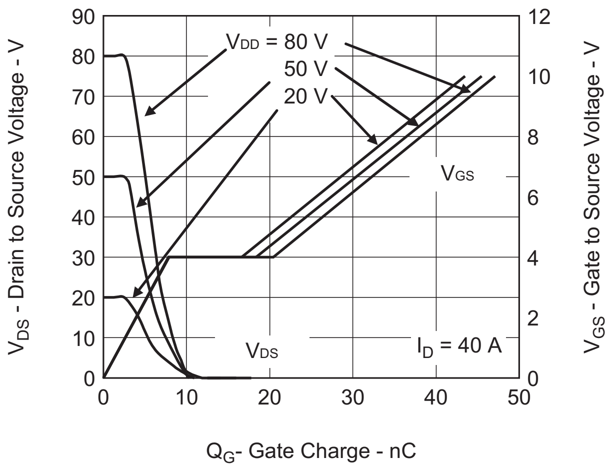
CAPACITANCE vs. DRAIN TO SOURCE VOLTAGE



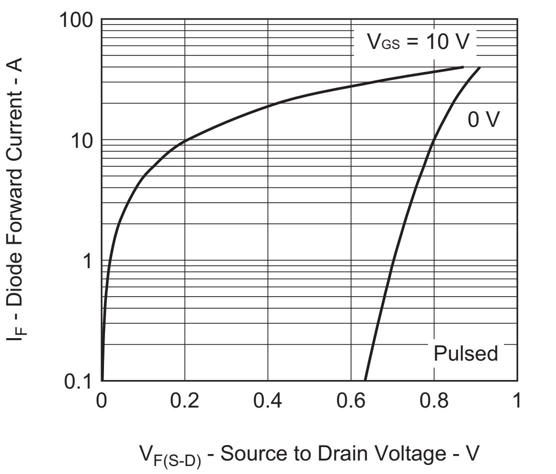
SWITCHING CHARACTERISTICS



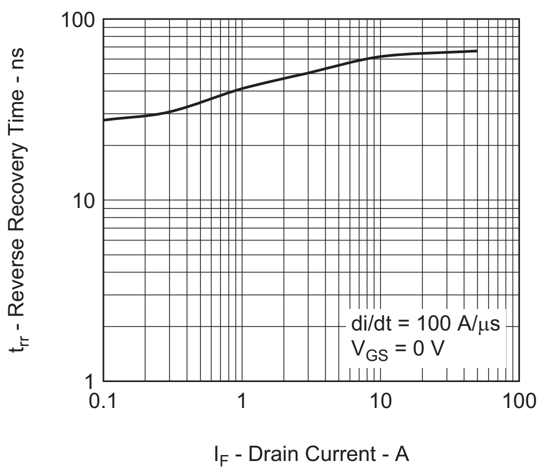
DYNAMIC INPUT/OUTPUT CHARACTERISTICS



SOURCE TO DRAIN DIODE FORWARD VOLTAGE



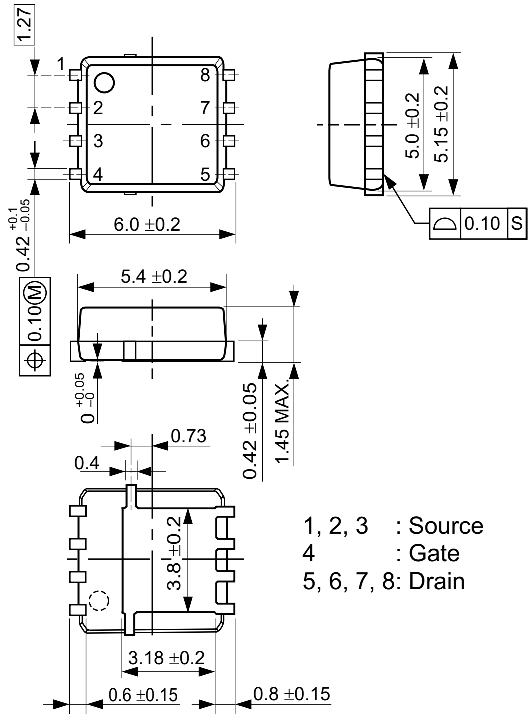
REVERSE RECOVERY TIME vs. DRAIN CURRENT



Package Drawings (Unit: mm)

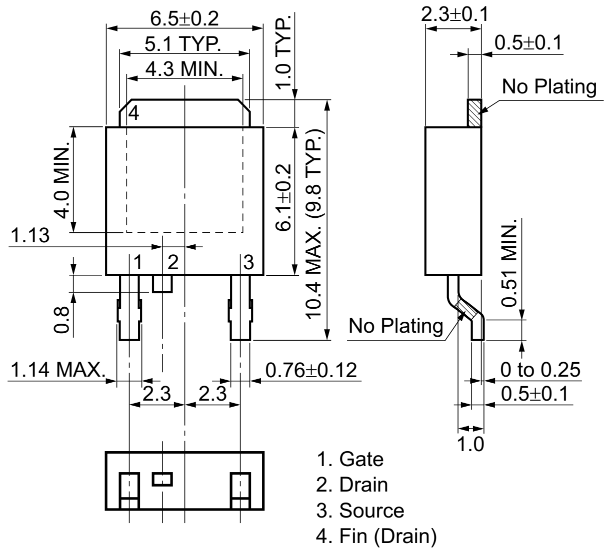
8-pin HSON (Mass: 0.13 g TYP.)

Renesas package code: PLSN0008KA-A



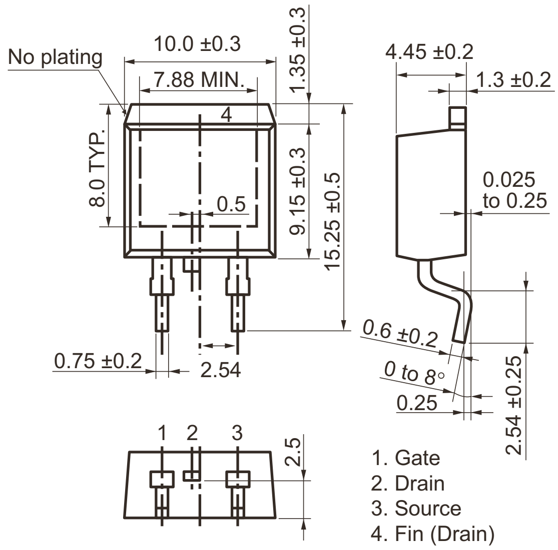
TO-252 (MP-3ZP) (Mass: 0.27 g TYP.)

Renesas package code: PRSS0004ZP-A



TO-263 (MP-25ZP) (Mass: 1.48 g TYP.)

Renesas package code: PRSS0004AL-A



Revision History	NP40N10YDF, NP40N10VDF, NP40N10PDF Data Sheet

Rev.	Date	Description	
		Page	Summary
1.00	Feb 21, 2013	—	First Edition Issued
2.00	Mar 11, 2013	1 7	"Outline" added Modification of "CAPACITANCE vs. DRAIN TO SOURCE VOLTAGE"
2.01	May 13, 2013	1 8	Modification of "Outline" Modification of "Package Drawings 8-pinHSON"

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Colophon 2.2