50 W AC-DC Converters H-Family

Single output: **series 110H/230H1000**
Dual output: **series 110H/230H2000**
Triple output: **series 110H/230H3000**

- Two input voltage ranges suitable for most AC mains
- Efficient input filter and built-in surge and transient suppression circuitry
- 3 kV_{rms} input to output electric strength test
- Outputs individually isolated
- Outputs fully protected against overload

Safety according to IEC 950

LGA

Table of Contents ..... Page

Description

The H-family of AC-DC converters represents a broad and flexible range of power supplies for use in advanced electronic systems. Features include high efficiency, reliability and low output voltage noise.

The converter inputs are protected against surges and transients occuring at the source lines. An input over- and undervoltage cut-out circuitry disables the outputs if the input voltage is outside the specified range. The modules include an inrush current limitation preventing circuit breakers and fuses from being damaged at switch-on.

All outputs are open- and short-circuit proof and are protected against overvoltages by means of built-in suppressor diodes. The outputs can be inhibited by a logic signal applied to the connector pin 2(i). If the inhibit function is not used pin 2 should be connected with pin 23 to enable the outputs.

LED indicators display the status of the converter and allow visual monitoring of the system at any time.

Full input to output, input to case, output to case and output to output isolation is provided. The modules are designed and built according to the international safety standard IEC 950 and have been approved by the safety agencies LGA (Germany) and UL (USA). The UL Mark for Canada has been officially recognized be regulatory authorities in provinces across Canada.

The case design allows operation at nominal load up to 50°C in a free air ambient temperature. If forced cooling is provided, the ambient temperature may exceed 50°C but the case temperature should remain below 80°C under all conditions.

A temperature sensor generates an inhibit signal which disables the outputs if the case temperature T_C exceeds the limit. The outputs are automatically re-enabled when the temperature drops below the limit.

Various options are available to adapt the converters to individual applications.

The modules may either be plugged into 19 inch rack systems according to DIN 41494, or be chassis mounted.

Case: aluminium, black finish, self cooling.
Dimensions: 38.7 × 111.2 × 168.5 mm. Weight: 770 g

Type Survey

Options see "Descriptions of Options"

Table 1: Type survey

Output 1		Output 2		Output 3		Input Voltage Range and Efficiency [1]				Option
$U_{o\,nom}$ V DC	$I_{o\,nom}$ A	$U_{o\,nom}$ V DC	$I_{o\,nom}$ A	$U_{o\,nom}$ V DC	$I_{o\,nom}$ A	$U_{i\,min}...U_{i\,max}$ **85...132 V AC 47...63 Hz**	η_{min} %	$U_{i\,min}...U_{i\,max}$ **187...255 V AC 47...63 Hz**	η_{min} %	
5.1	8.0					110H1001-2R	74	230H1001-2R	74	V2, V3
12.0	4.0					110H1301-2R	81	230H1301-2R	81	D1...D8
15.0	3.4					110H1501-2R	83	230H1501-2R	82	
24.0	2.0					110H1601-2R	83	230H1601-2R	82	
48.0	1.0					110H1901-2R	85	230H1901-2R	85	
12.0	2.0	12.0	2.0			110H2320-2	81	230H2320-2	81	
15.0	1.7	15.0	1.7			110H2540-2	82	230H2540-2	82	
5.1	5.0	12.0	0.7	12.0	0.7	110H3020-2	79	230H3020-2	78	
5.1	5.0	15.0	0.6	15.0	0.6	110H3040-2	79	230H3040-2	79	

[1] Efficiency measured at $U_{i\,nom}$ and $I_{o\,nom}$

Safety and Installation Instructions

Safety

If the output circuit of an AC-DC converter is operator-accessible according to the IEC 950 related safety standards, it shall be an SELV circuit (Safety Extra Low Voltage circuit, i.e. a circuit, separated from mains by at least basic insulation, that is so designed and protected such that under normal and single fault conditions, the voltage between any two conductors and between any conductor and earth does not exceed 60 V DC).

In the following section an interpretation is provided of the IEC 950 safety standard with respect to the safety status of the output circuit. However, it is the sole responsibility of the installer or user to assure the compliance with the relevant and applicable safety standards:

If the AC-DC converter is installed according to the relevant safety regulations its outputs are considered to be SELV circuits up to a nominal output voltage of 36 V.

For safety reasons, the modules must be wired via the female connector H11 (according to DIN 41612 see section "Accessories") in order to meet national and international safety requirements!

The connector protective earthing pin is leading. During the production process, all transformers and each of the fully assembled modules are individually tested for electric strength and earth continuity (see "Supplementary Data"). All electric strength tests are performed as factory tests.

Installation Instruction

Installation of the power supply must strictly follow the national safety regulations. To observe the safety requirements according to EN 60950/IEC 950, the module shall be connected via the female connector type H11 see section "Accessories". Other installation methods may not meet the safety requirements. The modules do not incorporate any fuse. At least one external fuse, installed in the wiring to the input is essential! See "Fuse types".

Whenever the inhibit function is not required, pin 2 (i) should be connected to pin 23 to enable the output(s).

Important Advice

Electric strength tests should not be repeated in the field. Improper test methods, for example overshooting or oscillating test voltages, voltage slopes exceeding 1 kV/µs, internal Y-capacitors not carefully discharged, etc. can cause severe damage to switching devices and ICs. Melcher AG will not honour any guarantee/warranty claims resulting from high voltage field tests.

Table 2: H11 connector pin allocation

Electrical Determination	H1000		H2000		H3000	
	Pin	Ident	Pin	Ident	Pin	Ident
Inhibit control input Safe Data or ACFAIL	2 5	i D or V	2 5	i D or V	2 5	i D or V
Output voltage (positive) Output voltage (negative)	8 11	Vo1+ Vo1–	8 11		8 11	Vo3+ Vo3–
Control input + Control input –	14 17	R G				
Output voltage (positive) Output voltage (negative)			14 17	Vo2+ Vo2–	14 17	Vo2+ Vo2–
Output voltage (positive) Output voltage (negative)	20 23	Vo1+ Vo1–	20 23	Vo1+ Vo1–	20 23	Vo1+ Vo1–
Protective earthing [1]	26	⏚	26	⏚	26	⏚
AC input voltage AC input voltage	29 32	N~ P~	29 32	N~ P~	29 32	N~ P~

[1] Leading pin (pregrounding)

Degree of Protection

Condition: Female connector fitted to the unit

IP 40: All units, except those with options D or V incorporating potentiometer adjustment.

IP 20: Type fitted with options D or V incorporating potentiometer.

Functional Description

The input voltage is fed via an input filter, an inrush current limiter and a bridge rectifier to the input capacitor. This capacitor sources a single transistor forward converter. Each output is powered by a separate secondary winding of the main transformer. The resultant voltages are rectified and their ripples smoothed by a power choke. The control logic senses the main output voltage U_{o1} and generates, with respect to the maximum admissible output currents, the control signal for the primary switching transistor. This signal is fed back via a coupling transformer.

The auxiliary outputs U_{o2} and U_{o3} are unregulated. Each auxiliary output's current is sensed and transferred to the main control circuit using a current transformer. If one of the outputs is driven into current limit, the other outputs will reduce their output voltages as well because all output currents are controlled by the same control circuit.

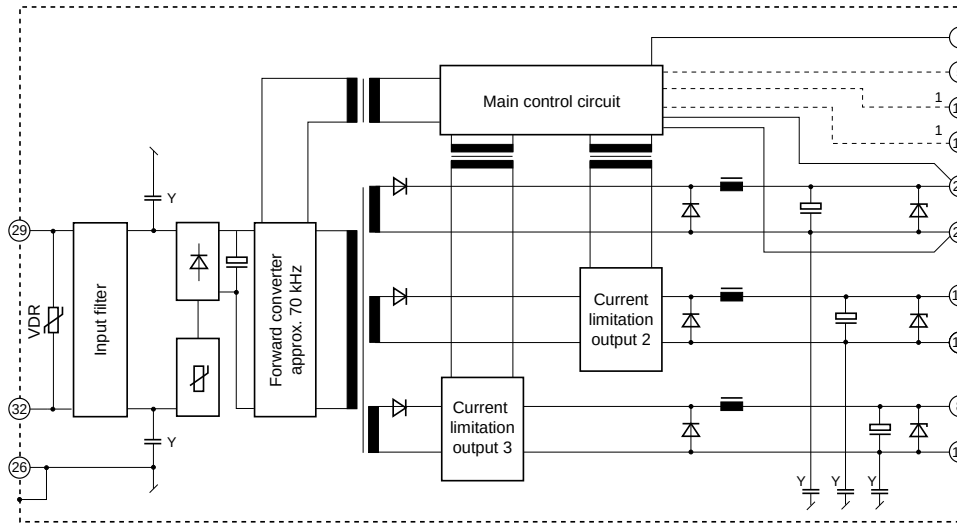


Fig. 1
AC-DC converter block diagram

[1] Single output modules H1000 (R input)

Electrical Input Data

General conditions:
– T_A = 25°C, unless T_C is specified. – Connector pins 2 and 23 interconnected, R input not connected.

Table 3: Input data

Input			110H			230H			
Characteristics		Conditions	min	typ	max	min	typ	max	Unit
U_i	Input voltage range	I_o = 0…$I_{o\,nom}$ $T_{C\,min}$…$T_{C\,max}$	85		132	187		255	V AC
$U_{i\,nom}$	Nominal input voltage			110			230		
I_i	Input current	$U_{i\,nom}$, $I_{o\,nom}$ [1]		0.78			0.44		A_{rms}
$S_{i\,0}$	No-load apparent input power: Single output Double output Triple output	$U_{i\,nom}$ $I_{o1,2,3}$ = 0		 1 7 7	 1.5 9 9		 1 7 7	 1.5 9 9	VA
$S_{i\,inh}$	Idle apparent input power	inhibit mode			2.5			2.5	
$I_{inr\,p}$ [3]	Peak inrush current	U_i = $U_{i\,max}$ R_S = 0 Ω [4] T_C = 25°C			80			42	A
$t_{inr\,r}$	Rise time			200			300		µs
$t_{inr\,h}$	Trailing edge half-life			1100			1600		
R_i	Input resistance	T_C = 25 °C	450			800			mΩ
R_{NTC} [2]	NTC resistance		2000			8000			
C_i	Input capacitance		250		570	50		270	µF
$U_{i\,abs}$	Input voltage limits without any damage		0		142	0		284	V AC

[1] With multiple output modules, the same condition for each output applies.
[2] Initial switch-on cycle. Subsequent switch on/off cycles increase the inrush current peak value.
[3] $I_{inr\,p} = U_i/(R_s + R_i + R_{NTC})$
[4] R_S = source resistance.

Input Under-/Overvoltage Cut-out

If the input voltage remains below 0.6 $U_{i\,min}$ or exceeds 1.1 $U_{i\,max}$ (approx. values), an internally generated inhibit signal disables the output(s). When checking this function the absolute maximum input voltage rating $U_{i\,abs}$ must be carefully considered (see table above).

Input fuse

The modules do not incorporate any fuse. External fuses installed in the wiring to the input are essential.

Table 4: Recommended fuse types (slow-blow)

Series	Schurter type	Part number
110H	SPT 2.5 A 250 V	0001.2508
230H	SPT 2.5 A 250 V	0001.2508

Electrical Output Data

General conditions
– T_A = 25°C, unless T_C is specified.
– Connector pins 2 and 23 interconnected, R input not connected.

Table 5a: Output data

Output		$U_{o\,nom}$	**5.1 V**			**12 V**			**15 V**			
Characteristics		Conditions	min	typ	max	min	typ	max	min	typ	max	Unit
U_{o1}	Output voltage	$U_{i\,nom}$, $I_{o\,nom}$ [1]	5.00		5.20	11.76		12.24	14.70		15.30	V
$U_{o2/3}$				-		11.10		12.90	13.90		16.10	
$U_{o2/3\,0}$		$U_{i\,min}$...$U_{i\,max}$ $I_{o2/3}$ = 0		-				13.80			17.25	
$U_{o1\,L}$	Overvoltage prot.	Failure in control circuit		7.5			21			25		
$U_{o2/3\,L}$				-			25			31		
$I_{o\,nom}$	Output current	$U_{i\,min}$...$U_{i\,max}$ $T_{C\,min}$...$T_{C\,max}$	see table 1									
$I_{o\,L}$	Output current limitation response		see fig. 2									
$u_{o1/2/3}$	Output voltage noise	$U_{i\,nom}$, $I_{o\,nom}$ [1] BW = 20 MHz			50			120			150	mV_{rms}
					200			360			450	mV_{pp}
$\Delta U_{o1\,U}$	Static line regulation	$U_{i\,min}$...$U_{i\,nom}$		±20	±50		±25	±120		±30	±150	mV
$\Delta U_{o2/3\,U}$		$U_{i\,nom}$...$U_{i\,max}$ $I_{o\,nom}$ [1]		-			±80	±240		±100	±300	
$\Delta U_{o1\,I}$	Static load regulation	$U_{i\,nom}$ I_o = $I_{o\,nom}$...0 [2]		15	50		35	120		45	150	
$\Delta U_{o2/3\,I}$				-			see fig. 3			see fig. 4		
$\Delta U_{o1\,Ic}$	Static cross load regulation [3]	$U_{i\,nom}$ I_o = $I_{o\,nom}$...0 [4]		±5	±15		±10	±30		±15	±45	
$\Delta U_{o2/3\,Ic}$				-			see fig. 3			see fig. 4		

Table 5b: Output data

Output		$U_{o\,nom}$	**24 V**			**48 V**			Unit
Characteristics		Conditions	min	typ	max	min	typ	max	
U_{o1}	Output voltage	$U_{i\,nom}$, $I_{o1\,nom}$	23.52		24.48	47.04		48.96	V
$U_{o\,L}$	Overvoltage prot.	$I_{o1\,nom}$		41			85		
$I_{o1\,nom}$	Output current	$U_{i\,min}$...$U_{i\,max}$ $T_{C\,min}$...$T_{C\,max}$	see table 1						
$U_{o1\,L}$	Output current limitation response		see fig. 2						
u_{o1}	Output voltage noise	$U_{i\,nom}$, $I_{o1\,nom}$ BW = 20 MHz			240			480	mV_{rms}
					720			1440	mV_{pp}
$\Delta U_{o1\,U}$	Static line regulation	$U_{i\,min}$...$U_{i\,nom}$ $U_{i\,nom}$...$U_{i\,max}$ $I_{o1\,nom}$		±30	±240		±30	±480	mV
$\Delta U_{o1\,I}$	Static load regulation	$U_{i\,nom}$ I_{o1} = $I_{o1\,nom}$...0		70	240		150	480	

[1] With multiple output modules, the same condition for each output applies.
[2] Condition for specified output. With multiple output modules, other output(s) loaded with constant current I_o = $I_{o\,nom}$.
[3] Condition for non-specified output, individually tested, other output(s) loaded with constant current I_o = $I_{o\,nom}$.
[4] Multiple output modules.

Output Protection

Each output is protected against overvoltages which could occur due to a failure of the internal control circuit. Voltage suppressor diodes (which under worst case condition may become a short circuit) provide the required protection. The suppressor diodes are not designed to withstand externally applied overvoltages. Overload at any of the outputs will cause a shut-down of all outputs.

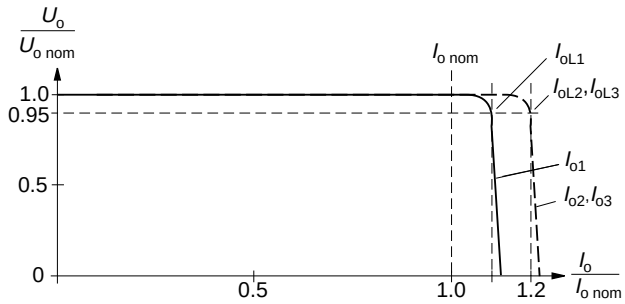


Fig. 2
Typical output voltage U_o versus output currents I_o

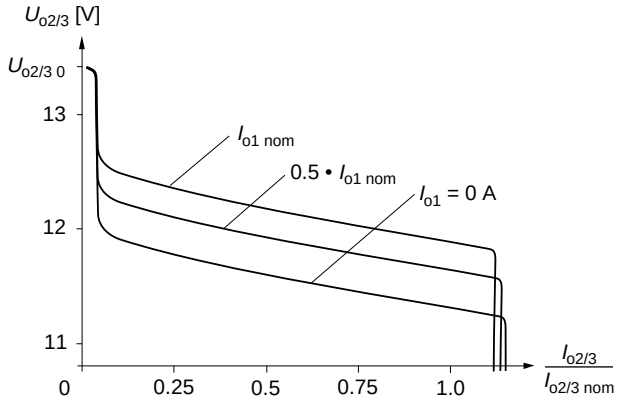


Fig. 3
H2320/3020: $\Delta U_{o2/3}$ (typ.) versus $I_{o2/3}$ with different I_{o1}

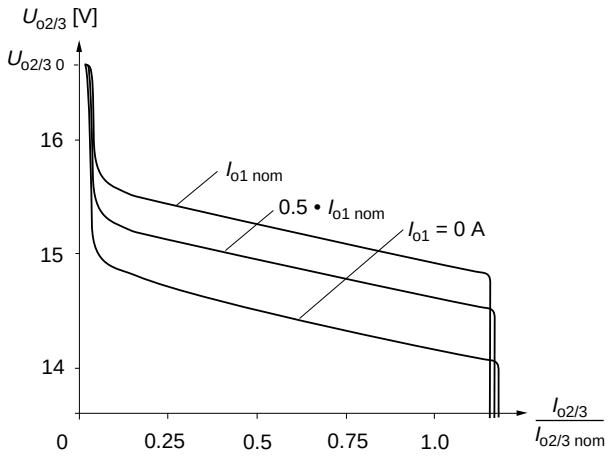


Fig. 4
H2540/3040: $\Delta U_{o2/3}$ (typ.) versus $I_{o2/3}$ with different I_{o1}

Parallel and Series Connection

Main outputs of equal nominal voltage can be connected in parallel. It is important to assure that the main output of a multiple output module is forced to supply a minimum current of 0.1 A to enable correct operation of its own auxiliary outputs. Outputs one and two of a dual output unit may be connected parallel without a minimum current requirement at the main output. Outputs two and three of a triple output unit can be connected in parallel.

In parallel operation, one or more of the outputs may operate continuously in current limit which will cause an increase in case temperature. Consequently, a reduction of the max. ambient temperature by 10 K is recommended.

Main or auxiliary outputs can be connected in series with any other output of the same or another module. In series connection, the maximum output current is limited by the lowest current limit. Output ripple and regulation values are added. Connection wiring should be kept as short as possible.

If output terminals are connected together in order to establish multi-voltage configurations, e.g. +5.1 V, ±12 V etc. the common ground connecting point should be as close as possible to the connector of the converter to avoid excessive output ripple voltages.

Inhibit (i Input)

The outputs of the module may be enabled or disabled by means of a logic signal (TTL, CMOS, etc.) applied to the inhibit input. If the inhibit function is not required, connect the inhibit pin 2 to pin 23 to enable the outputs (active low logic, fail safe).

The reference for the inhibit signal is the negative pin of output 1.

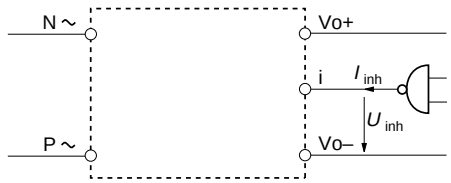


Fig. 5
Definition of inhibit voltage and current

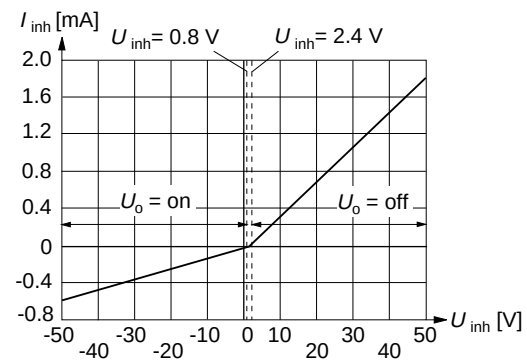


Fig. 6
Typical inhibit current I_{inh} versus inhibit voltage U_{inh}

Table 6: Inhibit data

Characteristics			Conditions	min	typ	max	Unit
U_{inh}	Inhibit input voltage causing output voltage being…	switched on	$U_{i\,min}$...$U_{i\,max}$	–50		0.8	V DC
		switched off		2.4		50	
I_{inh}	Inhibit current		U_{inh} = 0	–60	–100	–220	µA

Output Response

The reaction of the outputs is similar whether the input voltage is applied or the inhibit is switched low.

An output voltage overshoot will not occur when the module is turned on or off.

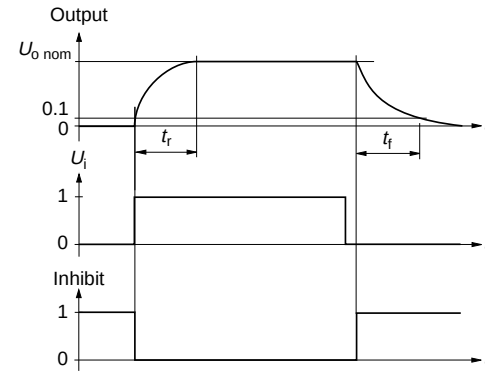


Fig. 7
Output response as a function of input voltage (on/off switching) or inhibit control

Table 7: Output response time

Type of Converter	t_r at P_o = 0 and t_f at P_o = $P_{o\,nom}$ typ	max	t_r and t_f at P_o = $^3/_4$ $P_{o\,nom}$ typ	max	t_r at P_o = $P_{o\,nom}$ typ	max	Unit
H1001-2R	3	17	3	17	5	25	ms
H1301-2R	5	25	8	30	10	40	
H1501-2R	3	17	5	25	15	50	
H1601-2R	8	30	15	45	20	70	
H1901-2R	35	100	50	150	85	230	
H2320-2	10	40	15	50	25	80	
H2540-2	8	30	10	40	20	60	
H3020-2	30	85	45	130	75	210	
H3040-2	20	70	30	90	50	150	

Conditions:
R input not used. For multiple output modules the figures indicated in the table above relate to the output which reacts slowest. All outputs are resistively loaded. Variation of the input voltage within $U_{i\,min}$...$U_{i\,max}$ does not influence the values.

Programmable Voltage (R Input)

As a standard feature single output modules offer an adjustable output voltage identified by letter R in the type designation. The control input R (pin 14) accepts either a control voltage U_{ext} or a resistor R_{ext} to adjust the desired output voltage. When not connected, the control input automatically sets the output voltage to $U_{o\,nom}$. The control input is protected against external overvoltage up to 8 V max.

a) Adjustment by means of an external control voltage U_{ext} between pin 14 (R) and pin 17 (G):
The control voltage range is 0...2.75 V and allows an adjustment in the range of approximately
U_o = 0...110 % $U_{o\,nom}$.

$$U_{ext} \approx \frac{U_o}{U_{o\,nom}} \bullet 2.5\ V$$

b) Adjustment by means of an external resistor:
Depending upon the value of the required output voltage, the resistor shall be connected
either: Between pin 14 and pin 17 ($U_o < U_{o\,nom}$) to achieve an output voltage adjustment range of approx. U_o = 0...100% $U_{o\,nom}$

$$R_{ext} \approx 4\ k\Omega \bullet \frac{U_o}{U_{o\,nom} - U_o}$$

or: Between pin 14 and pin 20 ($U_o > U_{o\,nom}$) to achieve an output voltage adjustment range of approximately U_o = 100...110 % of $U_{o\,nom}$

$$R'_{ext} \approx 4\ k\Omega \bullet \frac{(U_o - 2.5\ V)}{2.5\ V \bullet (U_o/U_{o\,nom} - 1)}$$

For output voltages $U_o > U_{o\,nom}$, the minimum input voltage according to "Electrical Input Data" increases proportionally to $U_o/U_{o\,nom}$.

Warning

The value of R'_{ext} should never be less than 47 kΩ to avoid damage to the unit! R inputs may be parallel connected, but $1/R_{tot} = 1/R_1 + 1/R_2 + ...$ should be considered.

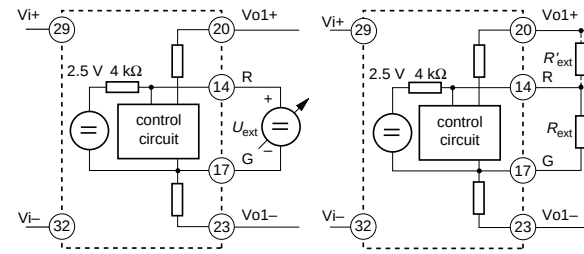


Fig. 8
Output voltage control by means of the R input

Table 8a: R_{ext} for $U_o < U_{o\,nom}$ (conditions: $U_{i\,nom}$, $I_{o\,nom}$, rounded up to resistor values E 96); $R'_{ext} = \infty$

$U_{o\,nom}$ = 5.1 V		$U_{o\,nom}$ = 12 V		$U_{o\,nom}$ = 15 V		$U_{o\,nom}$ = 24 V		$U_{o\,nom}$ = 48 V	
U_o [V]	R_{ext} [kΩ]	U_o [V]	R_{ext} [kΩ]	U_o [V]	R_{ext} [kΩ]	U_o [V]	R_{ext} [kΩ]	U_o [V]	R_{ext} [kΩ]
0.5	0.432	2.0	0.806	2.0	0.619	4.0	0.806	8.0	0.806
1.0	0.976	3.0	1.33	4.0	1.47	6.0	1.33	12.0	1.33
1.5	1.65	4.0	2.0	6.0	2.67	8.0	2.0	16.0	2.0
2.0	2.61	5.0	2.87	8.0	4.53	10.0	2.87	20.0	2.87
2.5	3.83	6.0	4.02	9.0	6.04	12.0	4.02	24.0	4.02
3.0	5.76	7.0	5.62	10.0	8.06	14.0	5.62	28.0	5.62
3.5	8.66	8.0	8.06	11.0	11.0	16.0	8.06	32.0	8.06
4.0	14.7	9.0	12.1	12.0	16.2	18.0	12.1	36.0	12.1
4.5	30.1	10.0	20.0	13.0	26.1	20.0	20.0	40.0	20.0
5.0	200.0	11.0	44.2	14.0	56.2	22.0	44.2	44.0	44.2

Table 8b: R'_{ext} for $U_o > U_{o\,nom}$ (conditions: $U_{i\,nom}$, $I_{o\,nom}$, rounded up to resistor values E 96); $R_{ext} = \infty$

$U_{o\,nom}$ = 5.1 V		$U_{o\,nom}$ = 12 V		$U_{o\,nom}$ = 15 V		$U_{o\,nom}$ = 24 V		$U_{o\,nom}$ = 48 V	
U_o [V]	R'_{ext} [kΩ]	U_o [V]	R'_{ext} [kΩ]	U_o [V]	R'_{ext} [kΩ]	U_o [V]	R'_{ext} [kΩ]	U_o [V]	R'_{ext} [kΩ]
5.15	464	12.1	1780	15.2	1470	24.25	3160	48.5	6810
5.20	215	12.2	909	15.4	750	24.50	1620	49.0	3480
5.25	147	12.3	619	15.6	511	24.75	1100	49.5	2370
5.30	110	12.4	464	15.8	383	25.00	825	50.0	1780
5.35	90.9	12.5	383	16.0	332	25.25	715	50.5	1470
5.40	78.7	12.6	316	16.2	274	25.50	590	51.0	1270
5.45	68.1	12.7	274	16.4	237	25.75	511	51.5	1100
5.50	61.9	12.8	249	16.5	226	26.00	453	52.0	953
		13.0	200			26.25	402	52.5	845
		13.2	169			26.40	383	52.8	806

EMC and Immunity to Input Transients

A metal oxide VDR together with an input filter form an effective protection against input transient voltages which typically occur in most installations. The H-Family has been successfully tested to the following specifications:

Electromagnetic Immunity

Table 9: Immunity type tests

Phenomenon	Standard	Level	Coupling mode [3]	Value applied	Waveform	Source impedance	Test procedure	In operation	Performance
Electrostatic discharge	IEC 801-2 (1991-04)	2	contact discharge to case,	4000 V_p	1/50 ns	330 Ω	10 positive and 10 negative	yes	[2]
Electric field	IEC 801-3 (1984)	2	antenna in 1m distance	3 V/m	sine wave modulated w. 1 kHz		26…1000 MHz	yes	[2]
Fast transient/ burst	IEC 801-4 (1988)	1	i/c, +i/–i	500 V_p	bursts of 5/50 ns 5 kHz rep. rate transients with 15 ms burst duration and a 300 ms period	50 Ω	1 min positive 1 min negative bursts per coupling mode	yes	[2]
Transient	IEC 801-5 (Draft 1993-01)	1	i/c	500 V_p	1.2/50 µs	12 Ω	5 pos. and 5 neg. impulses per coupling mode	yes	[1]
			+i/–i	500 V_p		2 Ω			

[1] Normal operation, no deviation from specifications
[2] Normal operation, temporary deviation from specs possible
[3] i = input, o = output, c = case

Electromagnetic Emissions

Table 10: Emissions at $U_{i\,nom}$ and $I_{o\,nom}$

Series	Standard	
	EN 55011, 1991 [1] EN 55022, 1987 [2]	
	≤30 MHz	≥30 MHz
110H	<B	<B
230H	<B	<B

[1] Identical with CISPR 11 (1990-09) and VDE 0875 part 11 (1992-07)
[2] Identical with CISPR 22 (1985) and FCC Part 15, VDE 0878 part 3 (1989-11)

Supplementary Data

Isolation

Input to output electric strength tests, in accordance with the safety standards IEC 950, EN 60950, VDE 0805 and EN 41003 are performed as factory tests and should not be repeated in the field.

Important Advice

Testing by applying AC voltages will result in high and dangerous leakage currents through the Y-capacitors (see fig. 1). Melcher will not honour any guarantee/warranty claims resulting from high voltage field tests. Reference is also made to chapter: "Safety and Installation Instructions".

Table 11: Electric strength test voltage, insulation resistance, clearance and creepage distances

Characteristic Values according to IEC 950		Input to output	Input to case	Output to case	Output to output	Unit
Electric strength test voltage	DC: 1 s	4243 [1]	2122	707	300	V
	AC: 50 Hz, 1 min	3000 [1]	1500	500	200	
Insulation resistance	at 500 V DC	≥300	≥300	≥100	–	MΩ
Clearance and creepage distances		4.0	2.0	1.0	0.9	mm

[1] Only subassemblies performance in accordance with IEC 950

Display Status of LEDs

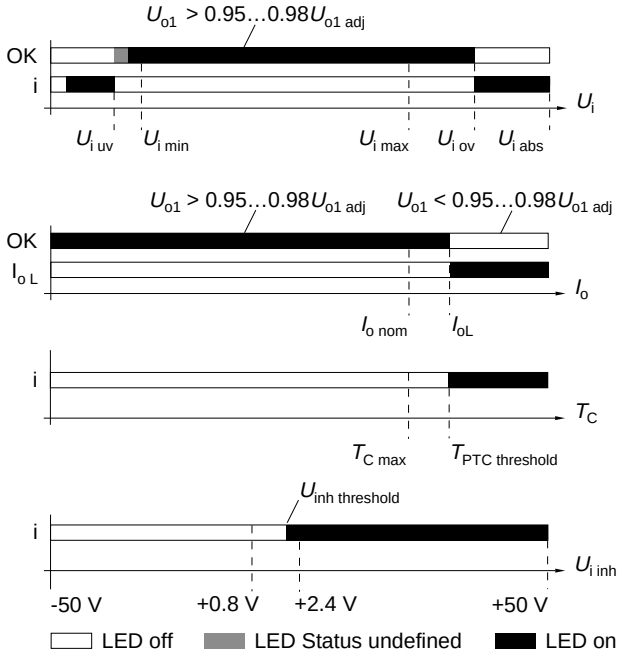


Fig. 9
LEDs "OK" and "i" status versus input voltage
Conditions: $I_o \le I_{o\,nom}$, $T_C \le T_{C\,max}$, $U_{inh} \le 0.8$ V
$U_{i\,uv}$ = undervoltage lock-out, $U_{i\,ov}$ = overvoltage lock-out

LED "OK" status versus output current
Conditions: $U_{i\,min}$...$U_{i\,max}$, $T_C \le T_{C\,max}$, $U_{inh} \le 0.8$ V

LED "i" versus case temperature
Conditions: $U_{i\,min}$...$U_{i\,max}$, $I_o \le I_{o\,nom}$, $U_{inh} \le 0.8$ V

LED "i" versus U_{inh}
Conditions: $U_{i\,min}$...$U_{i\,max}$, $I_o \le I_{o\,nom}$, $T_C \le T_{C\,max}$

10.3

Description of Options

Table 12: Survey of options

Option	Function of Option	Characteristic
D [1]	Input and/or output undervoltage monitoring circuitry	Safe data signal output (D1...D8)
V [1 2]	Input and output undervoltage monitoring circuitry	ACFAIL signal according to VME specifications (V2, V3)

[1] Option D excludes option V and vice versa
[2] Only available with main output voltage U_{o1} = 5.1 V

Option D Undervoltage monitor

The input and/or output undervoltage monitoring circuit operates independently of the built-in input undervoltage lockout circuit. A logic "low" (JFET output) or "high" signal (NPN output) is generated at pin 5 as soon as one of the monitored voltages drops below the preselected threshold level U_t. The return for this signal is Vo1– (pin 23). The D output recovers when the monitored voltage(s) exceed(s) U_t+U_h. The threshold level U_t is either adjustable by a potentiometer, accessible through a hole in the front cover, or is factory adjusted to a fixed value specified by the customer.

Option D exists in various versions D1...D8 as shown in the following table.

Table 13: Undervoltage monitor functions

Output type JFET	Output type NPN	Monitoring U_i	Monitoring U_{o1}	Minimum adjustment range of threshold level U_t U_{ti}	Minimum adjustment range of threshold level U_t U_{to}	Typical hysteresis U_h [% of U_t] for $U_{t\,min}$...$U_{t\,max}$ U_{hi}	Typical hysteresis U_h [% of U_t] for $U_{t\,min}$...$U_{t\,max}$ U_{ho}
D1	D5	no	yes	–	3.5 V...48 V [1]	–	2.3...1
D2	D6	yes	no	$U_{i\,min}$...$U_{i\,max}$ [1]	–	3.0...0.5	–
D3	D7	yes	yes	$U_{i\,min}$...$U_{i\,max}$ [1]	0.95...0.98 U_{o1} [2]	3.0...0.5	"0"
D4	D8	no	yes	–	0.95...0.98 U_{o1} [2]	–	"0"

[1] Threshold level adjustable by potentiometer (not recommended for mobile applications)
[2] Fixed value between 95% and 98% of U_{o1} (tracking)

JFET output (D1…D4):

Connector pin D is internally connected via the drain-source path of a JFET (self-conducting type) to the negative potential of output 1. $U_D \le 0.4$ V (logic low) corresponds to a monitored voltage level (U_i and/or U_{o1}) < U_t. The current I_D through the JFET should not exceed 2.5 mA. The JFET is protected by a 0.5 W Zener diode of 8.2 V against external overvoltages.

U_i, U_{o1} status	D output, U_D
U_i or $U_{o1} < U_t$	low, L, $U_D \le 0.4$ V at I_D = 2.5 mA
U_i and $U_{o1} > U_t + U_h$	high, H, $I_D \le 25$ µA at U_D = 5.25 V

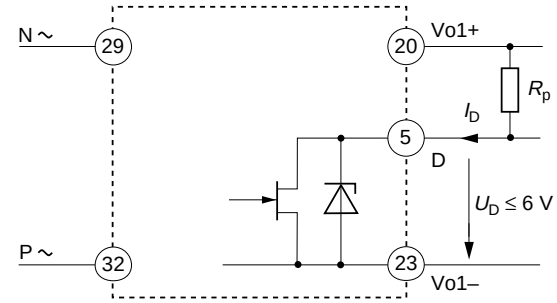


Fig. 10
Options D1...D4, JFET output

NPN output (D5...D8):

Connector pin D is internally connected via the collector-emitter path of a NPN transistor to the negative potential of output 1. $U_D < 0.4$ V (logic low) corresponds to a monitored voltage level (U_i and/or U_{o1}) > $U_t + U_h$. The current I_D through the open collector should not exceed 20 mA. The NPN output is not protected against external overvoltages. U_D should not exceed 40 V.

U_i, U_{o1} status	D output, U_D
U_i or $U_{o1} < U_t$	high, H, $I_D \le 25$ µA at U_D = 40 V
U_i and $U_{o1} > U_t + U_h$	low, L, $U_D \le 0.4$ V at I_D = 20 mA

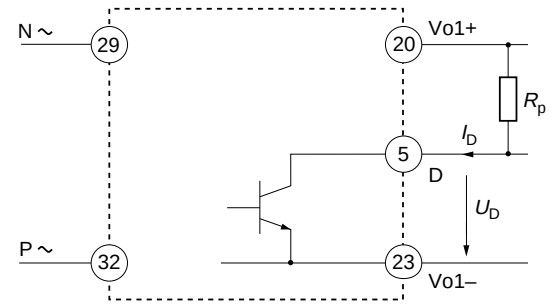


Fig. 11
Options D5...D8, NPN output

Threshold tolerances and hysteresis:

If U_i is monitored, the internal input voltage after the input filter and rectifier is measured. Consequently this voltage differs from the voltage at the connector pins by the voltage drop ΔU_{ti} across the input filter. The value of ΔU_{ti} depends upon the input voltage range, threshold level U_t, temperature and input current. The input current is a function of the input voltage and the output power.

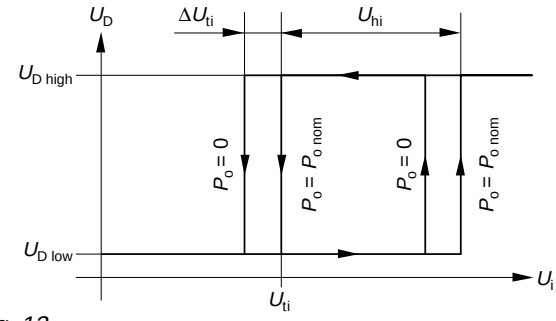
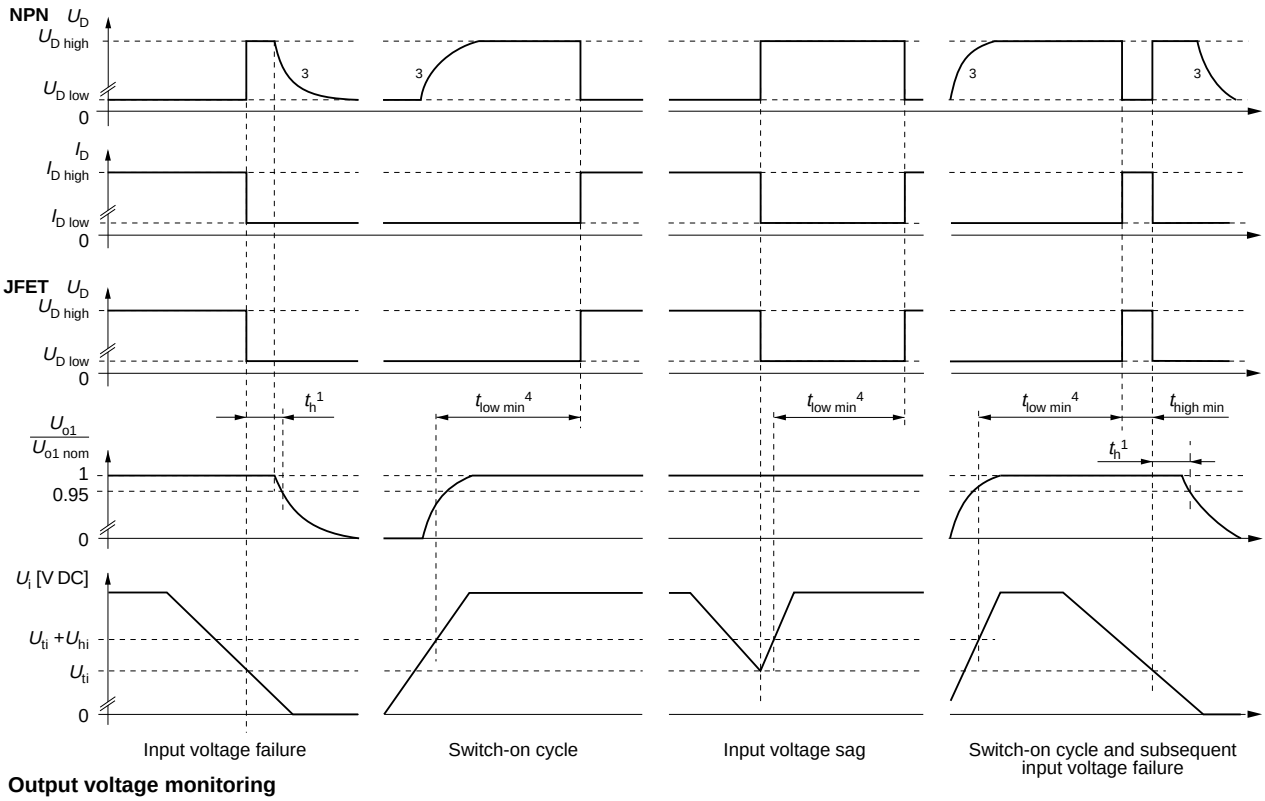
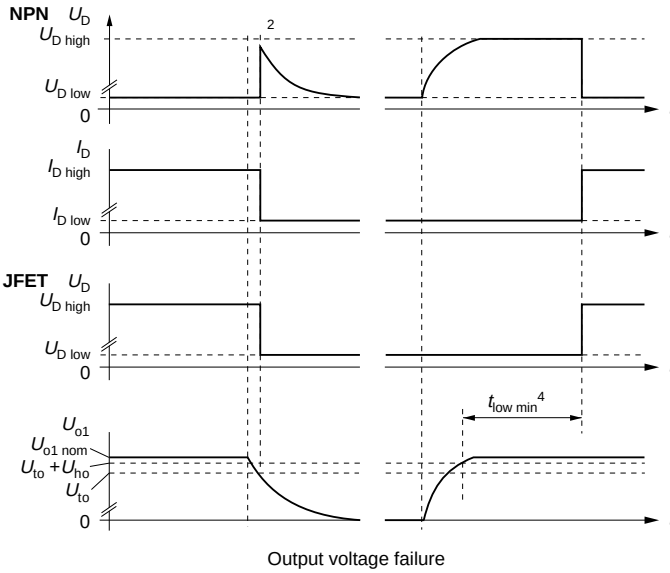


Fig. 12
Definition of U_{ti}, ΔU_{ti} and U_{hi} (JFET output)

Input voltage monitoring



Output voltage monitoring



[1] With output voltage monitoring the hold-up time $t_h = 0$
[2] The D signal remains high if the D output is connected to an external source.
[3] $t_{low\,min}$ = 40...200 ms, typically 80 ms

Fig. 13
Relationship between U_i, U_{o1}, U_D, I_D and $U_{o1}/U_{o\,nom}$ versus time.

Option V ACFAIL signal (VME)

This option defines an undervoltage monitoring circuit for the input or the input and main output voltage ($U_{o1\ nom}$ = 5.1 V only) equivalent to option D and generates the ACFAIL signal (V signal) which conforms to the VME standard. The low state level of the ACFAIL signal is specified at a sink current of I_V = 48 mA to $U_V \le 0.6$ V (open-collector output of a NPN transistor). The pull-up resistor feeding the open-collector output should be placed on the VME backplane.

After the ACFAIL signal has gone low, the VME standard requires a hold-up time t_h of at least 4 ms before the 5.1 V output drops to 4.875 V when the 5.1 V output is fully loaded. This hold-up time t_h is provided by the internal input capacitance. Consequently the working input voltage and the threshold level U_{ti} should be adequately above the minimum input voltage $U_{i\ min}$ of the converter so that enough energy is remaining in the input capacitance.

Table 14: Factory potentiometer setting of U_{ti}

Types	**110H**	**230H**	Unit
$C_{i\ min}$	0.25	0.05	mF
U_{ti}	94	200	V DC
t_h	5	5	ms

Formula for threshold level for desired value of t_h:

$$U_{ti} = \sqrt{\frac{2 \cdot P_o \cdot (t_h + 0.3\ ms) \cdot 100}{C_{i\ min} \cdot \eta}} + U_{i\ min}^2$$

where as:

$C_{i\ min}$ = minimum internal input capacitance [mF], according to table below
P_o = output power [W]
h = efficiency [%]
t_h = hold-up time [ms]
$U_{i\ min}$ = minimum input voltage [V]
U_{ti} = threshold level [V]

Remarks:

The threshold level U_{ti} of option V2 and V3 is adjusted during manufacture to a value according to table "Undervoltage monitor functions", section "Option D").

A decoupling diode should be connected in series with the input to avoid the input capacitance discharging through other loads connected to the same source voltage.

Option V operates independently of the built-in input undervoltage lock-out circuit. A logic "low" signal is generated at pin 5 as soon as one of the monitored voltages drops below the preselected threshold level U_t. The return for this signal is Vo1– (pin 23). The V output recovers when the monitored voltage(s) exceed(s) $U_t + U_h$. The threshold level U_t is adjustable by a potentiometer accessible through a hole in the front cover.
Versions V2 and V3 are available as shown below.

Table 15: Undervoltage monitor functions

V output (VME compatible)	**Monitoring** U_i	U_{o1}	**Minimum adjustment range of threshold level U_t** U_{ti}	U_{to}	**Typical hysteresis U_h [% of U_t] for $U_{t\ min}$...$U_{t\ max}$** U_{hi}	U_{ho}
V2	yes	no	$U_{i\ min}$...$U_{i\ max}$ [1]	–	3.0...0.5	-
V3	yes	yes	$U_{i\ min}$...$U_{i\ max}$ [1]	0.95...0.98 U_{o1} [2]	3.0...0.5	"0"

[1] Threshold level adjustable by potentiometer (not recommended for mobile applications)
[2] Fixed value between 95% and 98% of U_{o1} (tracking), output undervoltage monitoring is not a requirement of VME standard

V output (V2, V3):

Connector pin V is internally connected to the open collector of a NPN transistor. The emitter is connected to the negative potential of output 1. $U_V \le 0.6$ V (logic low) corresponds to a monitored voltage level (U_i and/or U_{o1}) < U_t. The current I_V through the open collector should not exceed 50 mA. The NPN output is not protected against external overvoltages. U_V should not exceed 80 V.

U_i, U_{o1} status	V output, U_V
U_i or $U_{o1} < U_t$	low, L, $U_V \le 0.6$ V at I_V = 50 mA
U_i and $U_{o1} > U_t + U_h$	high, H, $I_V \le 25$ µA at U_V = 5.1 V

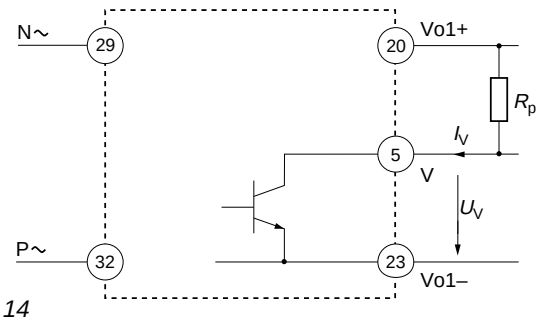


Fig. 14
Output configuration of options V2 and V3

Threshold tolerances and hysteresis:

If U_i is monitored, the internal input voltage is measured after the input filter and rectifier. Consequently this voltage differs from the voltage at the connector pins by the voltage drop ΔU_{ti} across input filter and rectifier. The value of ΔU_{ti} depends upon the input voltage range, threshold level U_t, temperature and input current. The input current is a function of input voltage and output power.

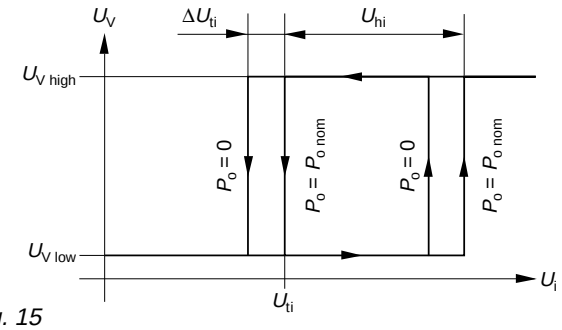
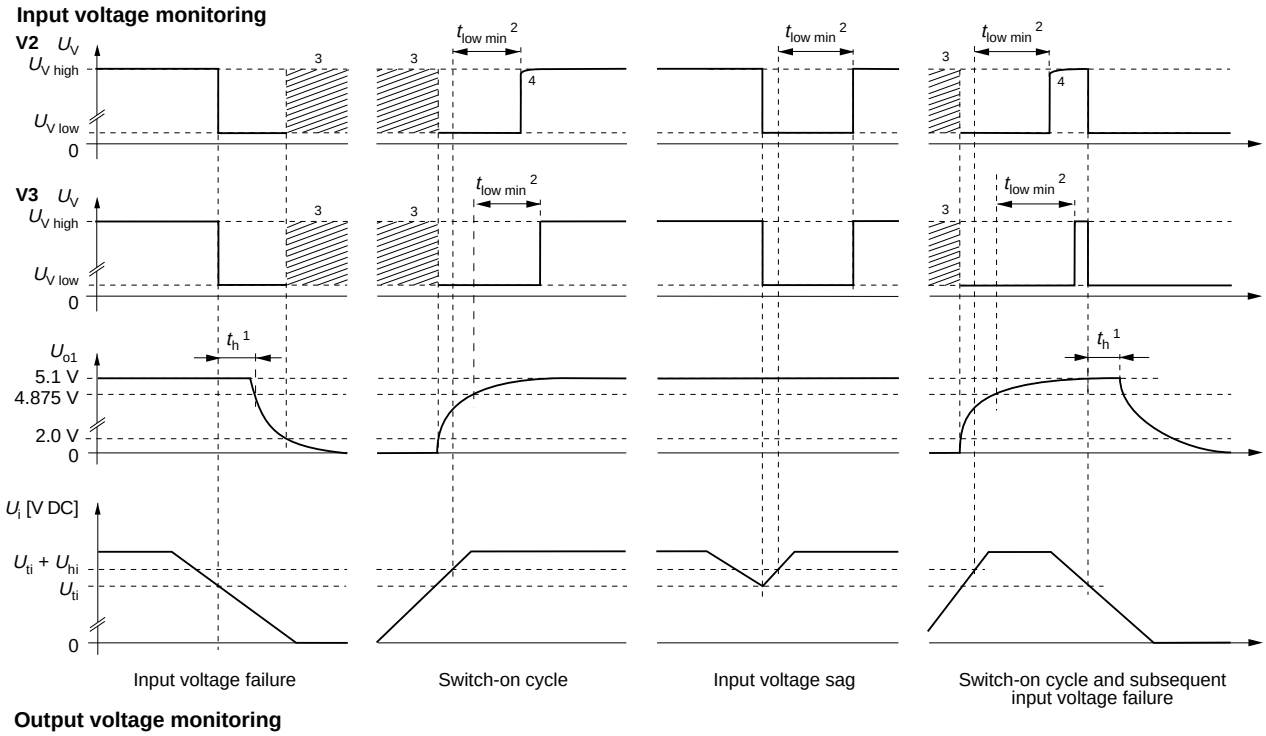
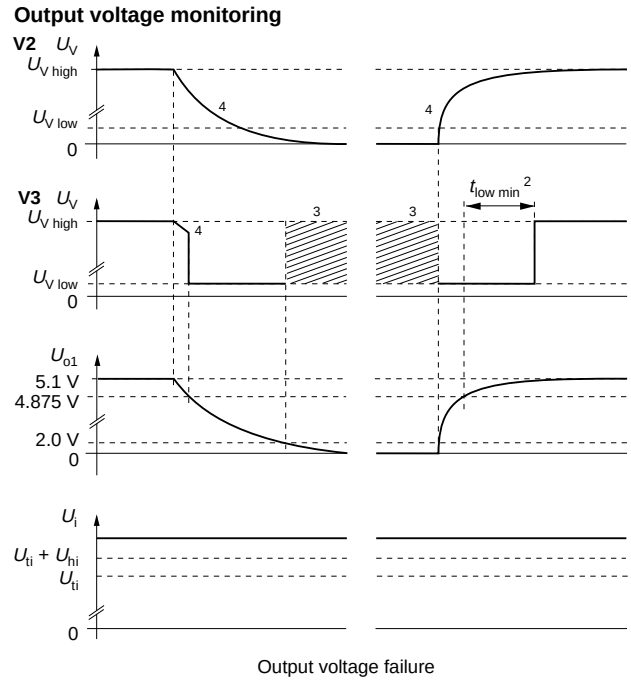


Fig. 15
Definition of U_{ti}, ΔU_{ti} and U_{hi}





[1] VME request: minimum 4 ms
[2] $t_{low\,min}$ = 40...200 ms, typically 80 ms
[3] U_V level not defined at U_{o1} < 2.0 V
[4] The V signal drops simultaneously with the output voltage, if the pull-up resistor R_P is connected to Vo1+. The V signal remains high if R_P is connected to an external source.

Fig. 16
Relationship between U_i, U_{o1}, U_V, I_V and $U_{o1}/U_{o\,nom}$ versus time.

Immunity to Environmental Conditions

Table 16: Mechanical stress

Test Method		Standard	Test Conditions	
Ca	Damp heat steady state	DIN 40046 part 5 IEC 68-2-3	Temperature: Relative humidity: Duration:	$40^{\pm 2}$ °C $93^{+2/-3}$ % 21 days Unit not operating
Ea	Shock (half-sinusoidal)	DIN 40046 part 7 IEC 68-2-27 MIL-STD-810D section 516.3	Acceleration amplitude: Bump duration: Number of bumps:	15 g_n = 147 m/s^2 11 ms 18 (3 each direction) Unit operating
Eb	Continuous shock (half-sinusoidal)	DIN 40046 part 26 IEC 68-2-29 MIL-STD-810D section 516.3	Acceleration amplitude: Bump duration: Number of bumps:	10 g_n = 98 m/s^2 16 ms 6000 (1000 each direction) Unit operating
Fc	Vibration (sinusoidal)	DIN 40046 part 8 IEC 68-2-6 MIL-STD-810D section 514.3	Frequency (1 Oct/min): Acceleration amplitude: Test duration:	10...150 Hz 2 g_n = 20 m/s^2 3.75 h (1.25 h each axis) Unit operating

Thermal considerations

Table 17: Temperature specifications, values given are for an air pressure of 800...1200 hPa (800...1200 mbar)

Characteristic		min	max	Unit
T_A	Standard operational ambient temperature range -2	-10	50	°C
T_C	Standard operational case temperature range -2, overtemp. lock-out (PTC) above $T_{C\,max}$	-10	80	
T_S	Storage temperature range -2	–25	100	

Basically the available output power is limited by thermal characteristics. Operation at higher temperatures with nominal output currents is also possible if forced cooling can be provided (heat sink, fan, etc.).

Example: Sufficient forced cooling allows $T_{A\,max}$ = 65 °C. A simple check of the case temperature T_C ($T_C \leq 80$ °C) at full load ensures correct operation of the system (temperature measurement point on the case see "Mechanical Data").

In general: For an ambient temperature of 65 °C with only convection cooling, the maximum permissible current for each output is approx. 50% of it's nominal value.

Table 18: MTBF

Values at specified Case Temperature	Module Types	Ground Benign 40°C	Unit
MTBF	H1000 H2000 H3000	384'000 306'000 270'000	h

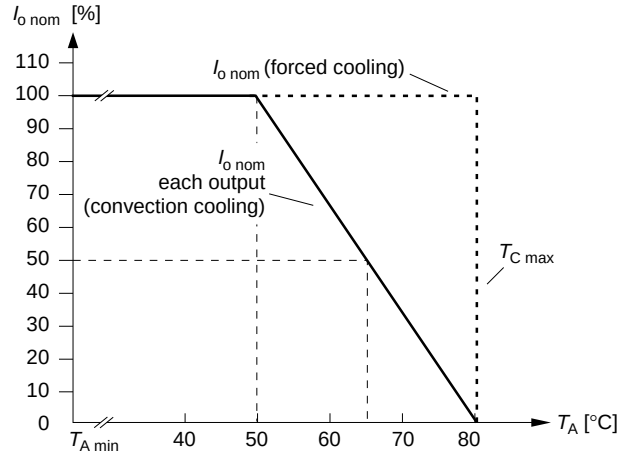


Fig. 17
Output derating versus ambient temperature under convection and forced cooling conditions

Mechanical Data

Dimensions in mm. Tolerances ±0.3 mm unless otherwise indicated.

European Projection

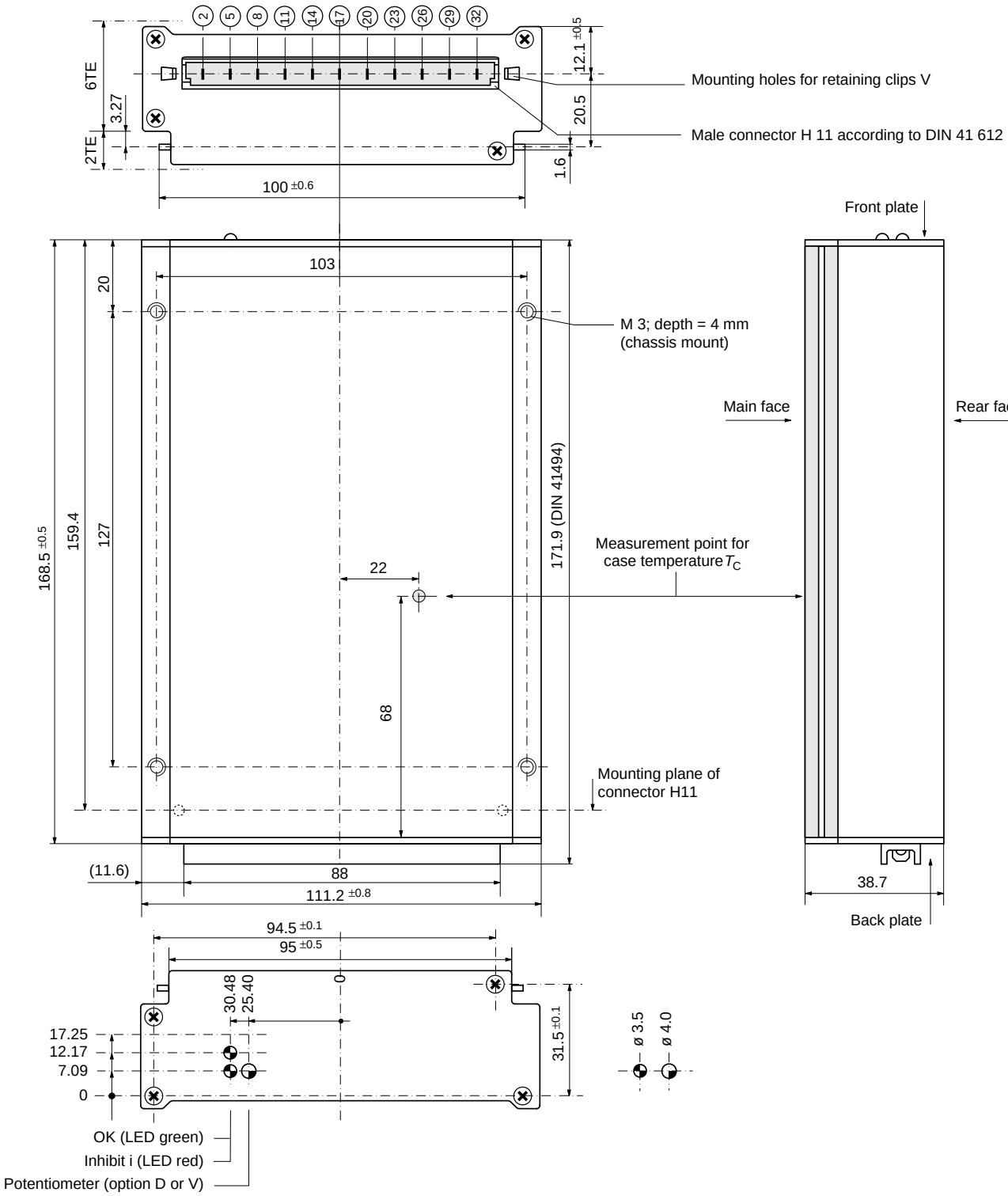
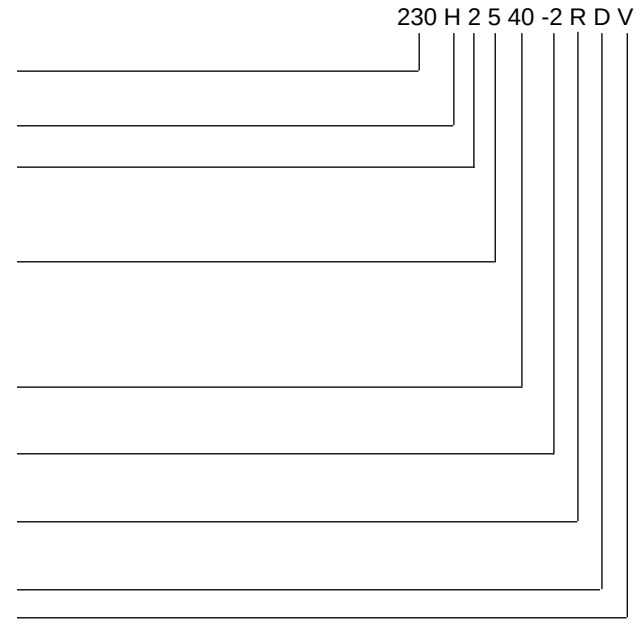


Fig. 18
Case H02, weight 770 g (approx.)

Type Key and Product Marking

Type Key



Input voltage range U_i:
85...132 V AC 110
187...255 V AC 230

Family ..... H

Number of outputs ..... 1...3

Output 1, $U_{o1\ nom}$:
5.1 V 0
12 V 3
15 V 5
24 V 6
48 V 9

Single output modules 01
Output 2 and 3, $U_{o2\ nom}$, $U_{o3\ nom}$:
12 V 20
15 V 40

Ambient temperature range T_A: -10…50 °C ..... -2
(operational)

Output voltage control input (single output modules only) R

Options:
Save data signal (D1...D8, to be specified) ..... D [1]
ACFAIL signal (V2, V3, to be specified) ..... V [1]

[1] Option D excludes option V and vice versa

Example: 230H1501-2RD3: AC-DC converter, input voltage range 187...255 V AC, providing output with 15 V/3.4 A; equipped with an output voltage control input and undervoltage monitoring.

Accessories: Front panels, female connectors, mounting facilities, etc. please refer to section "Accessories".

Product Marking (refer also to "Mechanical Data")

Main face: Basic type designation, applicable safety approval and recognition marks, warnings, pin allocation, Melcher patents and company logo.

Front plate: Identification of LEDs and potentiometer.

Back plate: Specific type designation, input voltage range, nominal output voltage(s) and current(s), pin allocation of options and auxiliary functions, external fuse specification and degree of protection.

Rear face: Label with batch no., serial no. and data code comprising production site, modification status of the main PCB, date of production. Confirmation of successfully passed final test.