

## 16-bit buffer/line driver; (3-State)

74LVC16541A  
74LVCH16541A

## FEATURES

- 5 volt tolerant inputs/outputs for interfacing with 5V logic
- Wide supply voltage range of 1.2 V to 3.6 V
- Complies with JEDEC standard no. 8-1A
- CMOS low power consumption
- MULTIBYTE™ flow-through standard pin-out architecture
- Low inductance multiple power and ground pins for minimum noise and ground bounce
- Direct interface with TTL levels
- All data inputs have bushold (74LVCH16541A only)

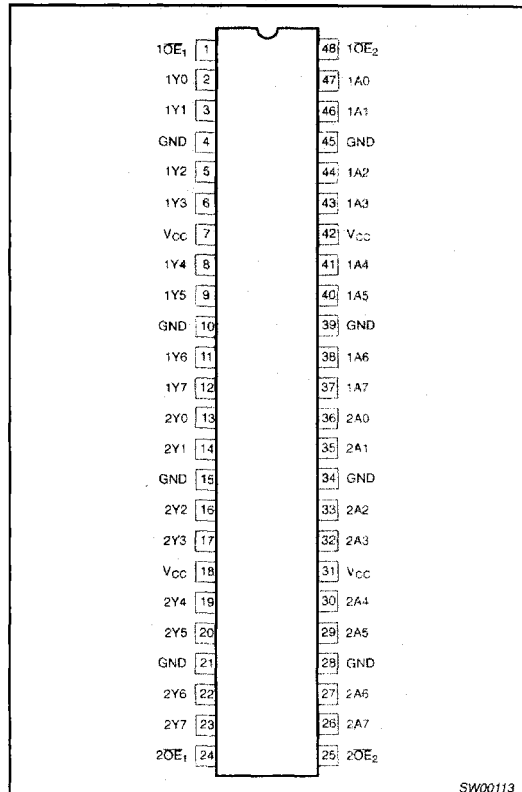
## DESCRIPTION

The 74LVC(H)16541A is a high-performance, low-power, low-voltage, Si-gate CMOS device, superior to most advanced CMOS compatible TTL families. Inputs can be driven from either 3.3V or 5V devices. In 3-State operation, outputs can handle 5V. These features allow the use of these devices in a mixed 3.3V/5V environment.

The 74LVC(H)16541A is a 16-bit inverting buffer/line driver with 3-State outputs. The 3-State outputs are controlled by the output enable inputs  $1OE_n$  and  $2OE_n$ . A HIGH on  $nOE_n$  causes the outputs to assume a high impedance OFF-state.

The 74LVC(H)16541A is identical to the 74LVC(H)16540A but has non-inverting outputs.

## PIN CONFIGURATION



## ORDERING INFORMATION

| PACKAGES                     | TEMPERATURE RANGE | OUTSIDE NORTH AMERICA | NORTH AMERICA | DWG NUMBER |
|------------------------------|-------------------|-----------------------|---------------|------------|
| 48-Pin Plastic SSOP Type III | -40°C to +85°C    | 74LVC16541A DL        | VC16541A DL   | SOT370-1   |
| 48-Pin Plastic TSSOP Type II | -40°C to +85°C    | 74LVC16541A DGG       | VC16541A DGG  | SOT362-1   |
| 48-Pin Plastic SSOP Type III | -40°C to +85°C    | 74LVCH16541A DL       | VCH16541A DL  | SOT370-1   |
| 48-Pin Plastic TSSOP Type II | -40°C to +85°C    | 74LVCH16541A DGG      | VCH16541A DGG | SOT362-1   |

## QUICK REFERENCE DATA

GND = 0V;  $T_{amb} = 25^\circ\text{C}$ ;  $t_r = t_f \leq 2.5\text{ns}$

| SYMBOL            | PARAMETER                                      | CONDITIONS                                    | TYPICAL | UNIT |
|-------------------|--|---|---------|------|
| $t_{PHL}/t_{PLH}$ | Propagation delay<br>1An to 1Yn;<br>2An to 2Yn | $C_L = 50\text{pF}$<br>$V_{CC} = 3.3\text{V}$ | 3.5     | ns   |
| $C_i$             | Input capacitance                              |   | 3.0     | pF   |
| $C_{PD}$          | Power dissipation capacitance per buffer       | $V_i = \text{GND to } V_{CC}^1$               | 30      | pF   |

## NOTES:

1.  $C_{PD}$  is used to determine the dynamic power dissipation ( $P_D$  in  $\mu\text{W}$ ):

$$P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o)$$

where:  
 $f_i$  = input frequency in MHz;  $C_L$  = output load capacity in pF;  
 $f_o$  = output frequency in MHz;  $V_{CC}$  = supply voltage in V;  
 $\sum (C_L \times V_{CC}^2 \times f_o)$  = sum of outputs.

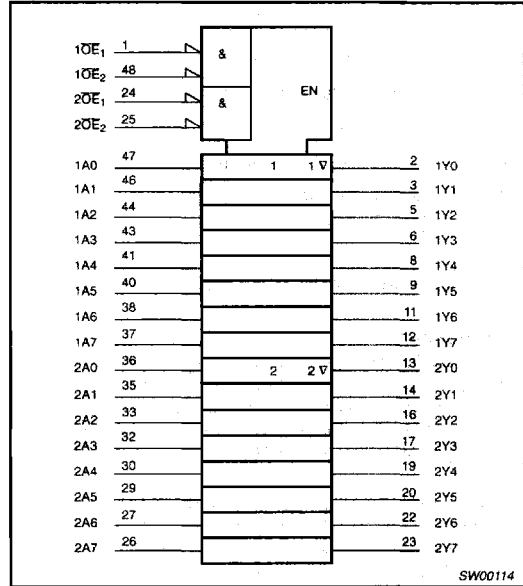
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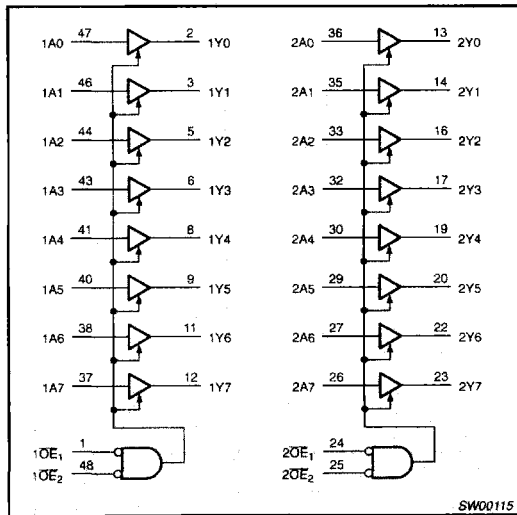
### PIN DESCRIPTION

| PIN NUMBER                     | SYMBOL           | NAME AND FUNCTION                |
|--------------------------------|------------------|----------------------------------|
| 1, 24                          | nOE <sub>1</sub> | Output enable input (active LOW) |
| 2, 3, 5, 6, 8, 9, 11, 12       | 1Y0 to 1Y7       | Data outputs                     |
| 4, 10, 15, 21, 28, 34, 39, 45  | GND              | Ground (0V)                      |
| 7, 18, 31, 42                  | V <sub>CC</sub>  | Positive supply voltage          |
| 13, 14, 16, 17, 19, 20, 22, 23 | 2Y0 to 2Y7       | Data outputs                     |
| 25, 48                         | nOE <sub>2</sub> | Output enable input (active LOW) |
| 36, 35, 33, 32, 30, 29, 27, 26 | 2A0 to 2A7       | Data inputs                      |
| 47, 46, 44, 43, 41, 40, 38, 37 | 1A0 to 1A7       | Data inputs                      |

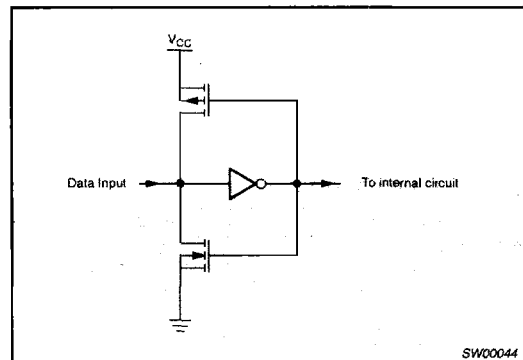
### LOGIC SYMBOL (IEEE/IEC)



### LOGIC SYMBOL



### BUSHOLD CIRCUIT



### FUNCTION TABLE

| INPUTS           |                  |     | OUTPUT |
|------------------|------------------|-----|--------|
| nOE <sub>1</sub> | nOE <sub>2</sub> | nAn | nYn    |
| L                | L                | L   | L      |
| L                | L                | H   | H      |
| X                | H                | X   | Z      |
| H                | X                | X   | Z      |

H = HIGH voltage level  
L = LOW voltage level  
X = don't care  
Z = high impedance OFF-state

## 16-bit buffer/line driver; (3-State)

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In accordance with the Absolute Maximum Rating System (IEC 134) Voltages are referenced to GND (ground = 0V)

| SYMBOL            | PARAMETER   | CONDITIONS   | MIN  | MAX            | UNIT               |
|-------------------|---|--|------|----------------|--------------------|
| $V_{CC}$          | DC supply voltage   |  | -0.5 | +6.5           | V                  |
| $I_{IK}$          | DC input diode current  | $V_I < 0$  | -    | -50            | mA                 |
| $V_I$             | DC input voltage  | Note 3   | -0.5 | +6.5           | V                  |
| $I_{OK}$          | DC output diode current   | $V_O > V_{CC}$ or $V_O < 0$  | -    | $\pm 50$       | mA                 |
| $V_O$             | DC output voltage; output HIGH or LOW state                               | Note 3   | -0.5 | $V_{CC} + 0.5$ | V                  |
| $V_O$             | DC output voltage; output 3-State   | Note 3   | -0.5 | 6.5            | V                  |
| $I_O$             | DC output source or sink current  | $V_O = 0$ to $V_{CC}$  | -    | $\pm 50$       | mA                 |
| $I_{GND}, I_{CC}$ | DC $V_{CC}$ or GND current  |  | -    | $\pm 100$      | mA                 |
| $T_{stg}$         | Storage temperature range   |  | -60  | +150           | $^{\circ}\text{C}$ |
| $P_{tot}$         | Power dissipation per package<br>- SO package<br>- SSOP and TSSOP package | Above +70 $^{\circ}\text{C}$ derate linearly 8mW/K<br>Above +60 $^{\circ}\text{C}$ derate linearly 5.5mW/K | -    | 500            | mW                 |

**NOTES:**

- Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150 $^{\circ}\text{C}$ .
- The input and output voltage ratings may be exceeded if the input and output clamp current ratings are observed.

**RECOMMENDED OPERATING CONDITIONS**

| SYMBOL     | PARAMETER   | CONDITIONS   | MIN. | MAX.     | UNIT               |
|------------|---|--|------|----------|--------------------|
| $V_{CC}$   | DC supply voltage (for max. speed performance)    |  | 2.7  | 3.6      | V                  |
| $V_{CC}$   | DC supply voltage (for low-voltage applications)  |  | 1.2  | 3.6      | V                  |
| $V_I$      | DC Input voltage range                            |  | 0    | 5.5      | V                  |
| $V_O$      | DC output voltage range; output HIGH or LOW state |  | 0    | $V_{CC}$ | V                  |
| $V_O$      | DC output voltage range; output 3-State           |  | 0    | 5.5      | V                  |
| $T_{amb}$  | Operating ambient temperature range in free air   | See DC and AC characteristics for individual device                | -40  | +85      | $^{\circ}\text{C}$ |
| $t_r, t_f$ | Input rise and fall times                         | $V_{CC} = 1.2$ to $2.7\text{V}$<br>$V_{CC} = 2.7$ to $3.6\text{V}$ | 0    | 20       | ns/V               |
|            |   |  | 0    | 10       |                    |

## 16-bit buffer/line driver; (3-State)

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Over recommended operating conditions

Voltages are referenced to GND (ground = 0V)

| SYMBOL                             | PARAMETER   | TEST CONDITIONS  | LIMITS                |                  |      | UNIT |
|------------------------------------|---|--|-----------------------|------------------|------|------|
|                                    |   |  | Temp = -40°C to +85°C |                  |      |      |
|                                    |   |  | MIN                   | TYP <sup>1</sup> | MAX  |      |
| V <sub>IH</sub>                    | HIGH level input voltage                                | V <sub>CC</sub> = 1.2V   | V <sub>CC</sub>       |                  |      | V    |
|                                    |   | V <sub>CC</sub> = 2.7 to 3.6V  | 2.0                   |                  |      |      |
| V <sub>IL</sub>                    | LOW level input voltage                                 | V <sub>CC</sub> = 1.2V   |                       |                  | GND  | V    |
|                                    |   | V <sub>CC</sub> = 2.7 to 3.6V  |                       |                  | 0.8  |      |
| V <sub>OH</sub>                    | HIGH level output voltage                               | V <sub>CC</sub> = 2.7; V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; I <sub>O</sub> = -12mA                | V <sub>CC</sub> -0.5  |                  |      | V    |
|                                    |   | V <sub>CC</sub> = 3.0V; V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; I <sub>O</sub> = -100μA              | V <sub>CC</sub> -0.2  | V <sub>CC</sub>  |      |      |
|                                    |   | V <sub>CC</sub> = 3.0V; V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; I <sub>O</sub> = -18mA               | V <sub>CC</sub> -0.6  |                  |      |      |
|                                    |   | V <sub>CC</sub> = 3.0V; V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; I <sub>O</sub> = -24mA               | V <sub>CC</sub> -0.8  |                  |      |      |
| V <sub>OH</sub>                    | HIGH level output voltage                               | V <sub>CC</sub> = 2.7; V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; I <sub>O</sub> = -6mA <sup>7</sup>    | V <sub>CC</sub> -0.5  |                  |      | V    |
|                                    |   | V <sub>CC</sub> = 3.0V; V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; I <sub>O</sub> = -100μA <sup>7</sup> | V <sub>CC</sub> -0.2  | V <sub>CC</sub>  |      |      |
|                                    |   | V <sub>CC</sub> = 3.0V; V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; I <sub>O</sub> = -12mA <sup>7</sup>  | V <sub>CC</sub> -1.0  |                  |      |      |
| V <sub>OL</sub>                    | LOW level output voltage                                | V <sub>CC</sub> = 2.7V; V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; I <sub>O</sub> = 12mA                |                       |                  | 0.40 | V    |
|                                    |   | V <sub>CC</sub> = 3.0V; V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; I <sub>O</sub> = 100μA               |                       |                  | 0.20 |      |
|                                    |   | V <sub>CC</sub> = 3.0V; V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; I <sub>O</sub> = 24mA                |                       |                  | 0.55 |      |
| V <sub>OL</sub>                    | LOW level output voltage                                | V <sub>CC</sub> = 2.7V; V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; I <sub>O</sub> = 6mA <sup>7</sup>    |                       |                  | 0.40 | V    |
|                                    |   | V <sub>CC</sub> = 3.0V; V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; I <sub>O</sub> = 100μA <sup>7</sup>  |                       |                  | 0.20 |      |
|                                    |   | V <sub>CC</sub> = 3.0V; V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; I <sub>O</sub> = 12mA <sup>7</sup>   |                       |                  | 0.55 |      |
| I <sub>I</sub>                     | Input leakage current                                   | V <sub>CC</sub> = 3.6V; V <sub>I</sub> = 5.5V or GND; not for I/O pins <sup>6</sup>                                |                       | ±0.1             | ±5   | μA   |
| I <sub>IHZ</sub> /I <sub>ILZ</sub> | Input current for common I/O pins                       | V <sub>CC</sub> = 3.6V; V <sub>I</sub> = 5.5V or GND; output disabled <sup>6</sup>                                 |                       | ±0.1             | ±10  | μA   |
| I <sub>OZ</sub>                    | 3-State output OFF-state current                        | V <sub>CC</sub> = 3.6V; V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; V <sub>O</sub> 5.5V or GND           |                       | 0.1              | ±10  | μA   |
| I <sub>OFF</sub>                   | Power off leakage current                               | V <sub>CC</sub> = 0.0V; V <sub>I</sub> or V <sub>O</sub> = 5.5V  |                       |                  | ±10  | μA   |
| I <sub>CC</sub>                    | Quiescent supply current                                | V <sub>CC</sub> = 3.6V; V <sub>I</sub> = V <sub>CC</sub> or GND; I <sub>O</sub> = 0                                |                       | 0.1              | 20   | μA   |
| ΔI <sub>CC</sub>                   | Additional quiescent supply current given per input pin | V <sub>CC</sub> = 2.7 to 3.6V; V <sub>I</sub> = V <sub>CC</sub> - 0.6V; I <sub>O</sub> = 0                         |                       | 5                | 500  | μA   |
| I <sub>BHL</sub>                   | Bus hold LOW sustaining current                         | V <sub>CC</sub> = 3.0V; V <sub>I</sub> = 0.8V <sup>2, 3, 4</sup>   | 75                    |                  |      | μA   |
| I <sub>BHH</sub>                   | Bus hold HIGH sustaining current                        | V <sub>CC</sub> = 3.0V; V <sub>I</sub> = 2.0V <sup>2, 3, 4</sup>   | -75                   |                  |      | μA   |
| I <sub>BHLO</sub>                  | Bus hold LOW overdrive current                          | V <sub>CC</sub> = 3.6V <sup>2, 3, 5</sup>  | 500                   |                  |      | μA   |
| I <sub>BHHO</sub>                  | Bus hold HIGH overdrive current                         | V <sub>CC</sub> = 3.6V <sup>2, 3, 5</sup>  | -500                  |                  |      | μA   |

**NOTES:**

- All typical values are at V<sub>CC</sub> = 3.3V and T<sub>amb</sub> = 25°C.
- Valid for data inputs of bus hold parts (LVCH16-A) only.
- For data inputs only, control inputs do not have a bus hold circuit.
- The specified sustaining current at the data input holds the input below the specified V<sub>I</sub> level.
- The specified overdrive current at the data input forces the data input to the opposite logic input state.
- For bus hold parts, the bus hold circuit is switched off when V<sub>I</sub> exceeds V<sub>CC</sub> allowing 5.5V on the input terminal.
- For data outputs of damping resistor parts (LVC(H)16-A only).

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74LVCH16541A

## AC CHARACTERISTICS

GND = 0V;  $t_R = t_F = 2.5\text{ns}$ ;  $C_L = 50\text{pF}$ ;  $R_L = 500\Omega$ ;  $T_{amb} = -40^\circ\text{C}$  to  $+85^\circ\text{C}$ .

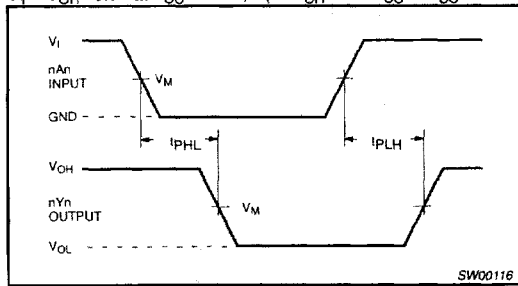
| SYMBOL                 | PARAMETER   | WAVEFORM | LIMITS                   |                  |                 |     | UNIT |
|------------------------|---|----------|--------------------------|------------------|-----------------|-----|------|
|                        |   |          | $V_{CC} = 3.3V \pm 0.3V$ |                  | $V_{CC} = 2.7V$ |     |      |
|                        |   |          | MIN                      | TYP <sup>1</sup> | MAX             | MAX |      |
| $t_{PHL}$<br>$t_{PLH}$ | Propagation delay<br>1An to 1Yn;<br>2An to 2Yn  | 1, 3     |                          | 5.2              | 6.2             | ns  |      |
| $t_{PZH}$<br>$t_{PZL}$ | 3-State output enable time<br>1OE <sub>n</sub> to 1Y <sub>n</sub> ;<br>2OE <sub>n</sub> to 2Y <sub>n</sub>  | 2, 3     |                          | 7.5              | 8.5             | ns  |      |
| $t_{PHZ}$<br>$t_{PLZ}$ | 3-State output disable time<br>1OE <sub>n</sub> to 1Y <sub>n</sub> ;<br>2OE <sub>n</sub> to 2Y <sub>n</sub> | 2, 3     |                          | 7.0              | 8.0             | ns  |      |

**NOTE:**

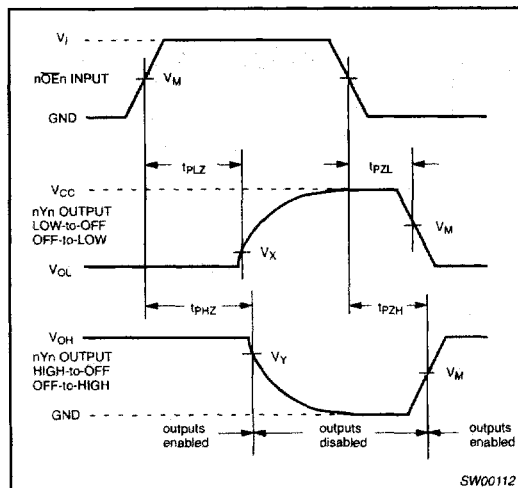
1. All typical values are at  $V_{CC} = 3.3V$  and  $T_{amb} = 25^\circ\text{C}$ .

## AC WAVEFORMS

$V_M = 1.5V$  at  $V_{CC} \geq 2.7V$ ;  $V_M = 0.5 V_{CC}$  at  $V_{CC} < 2.7V$ .  
 $V_{OL}$  and  $V_{OH}$  are the typical output voltage drop that occur with the output load.  
 $V_X = V_{OL} + 0.3V$  at  $V_{CC} \geq 2.7V$ ;  $V_X = V_{OL} + 0.1 V_{CC}$  at  $V_{CC} < 2.7V$   
 $V_Y = V_{OH} - 0.3V$  at  $V_{CC} \geq 2.7V$ ;  $V_Y = V_{OH} - 0.1 V_{CC}$  at  $V_{CC} < 2.7V$

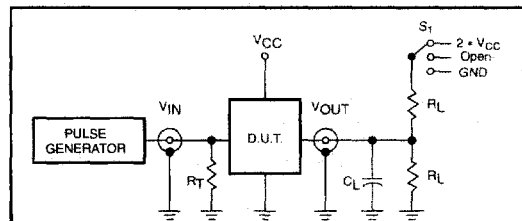


Waveform 1. Waveforms showing the input (An) to output (Yn) propagation delay times



Waveform 2. Waveforms showing the 3-State enable and disable times

## TEST CIRCUIT



Test Circuit for 3-State Outputs

**SWITCH POSITION**

| TEST              | SWITCH       |
|-------------------|--------------|
| $t_{PLH}/t_{PHL}$ | Open         |
| $t_{PLZ}/t_{PZL}$ | $2 * V_{CC}$ |
| $t_{PHZ}/t_{PZH}$ | GND          |

| $V_{CC}$     | $V_I$    |
|--------------|----------|
| $< 2.7V$     | $V_{CC}$ |
| $2.7 - 3.6V$ | $2.7V$   |

**DEFINITIONS**

$R_L$  = Load resistor; see AC CHARACTERISTICS for value.  
 $C_L$  = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.  
 $R_T$  = Termination resistance should be equal to  $Z_{OUT}$  of pulse generators.

Waveform 3. Load circuitry for switching times