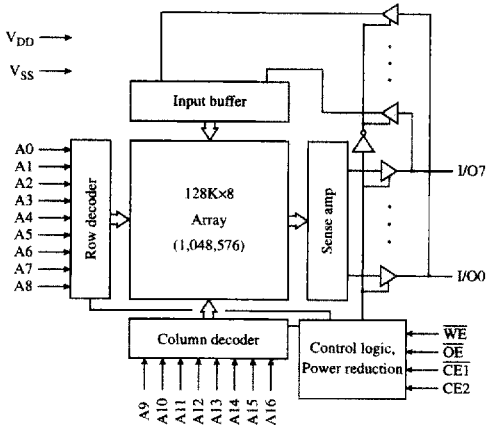
128K×8 Intelliwatt™ low power CMOS SRAM

Advance information

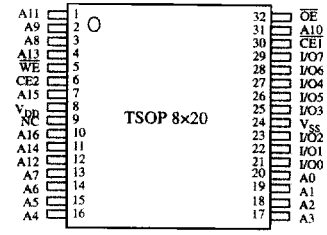
Features

- Intelliwatt active power reduction circuitry
- 2.3V to 3.0V operating range (JESD 8-5)
- Organization: 131,072 words × 8 bits
- High speed
  - 55/70/100 ns address access time
- Low power consumption
  - Active: 45 mW max (100 ns cycle)
  - Typical: <15 mW (100 ns cycle)
  - Standby: 3.0 µW max, CMOS I/O
  - Very low DC component in active power
- 1.5V data retention
- Easy memory expansion with $\overline{CE1}$, CE2, $\overline{OE}$ inputs
- JEDEC registered packaging
  - 32-pin TSOP package
  - 48-ball 8mm × 6mm CSP BGA
- ESD protection ≥ 2000 volts
- Latch-up current ≥ 200 mA
- Industrial and commercial temperature available
- Other voltage versions available
  - 1.65V to 1.95V (AS7C181024LL)
  - 2.7V to 3.6V (AS7C31024LL)

Logic block diagram



Pin arrangement (top view)



48-CSP Ball-Grid-Array Package (shading indicates no ball)

	1	2	3	4	5	6
A	A_0	A_1	CE2	A_3	A_6	A_8
B	I/O_4	A_2	$\overline{WE}$	A_4	A_7	I/O_0
C	I/O_5		NC	A_5		I/O_1
D	V_{SS}					V_{DD}
E	V_{DD}					V_{SS}
F	I/O_6		NC	NC		I/O_2
G	I/O_7	$\overline{OE}$	$\overline{CE1}$	A_{16}	A_{15}	I/O_3
H	A_9	A_{10}	A_{11}	A_{12}	A_{13}	A_{14}

Selection guide

	7C251024LL-55	7C251024LL-70	7C251024LL-100	Unit
Maximum address access time	55	70	100	ns
Maximum output enable access time	25	35	50	ns
Maximum operating current	25	20	15	mA
Maximum standby current	1	1	1	µA

DID 11-20017-A.

Functional description

The AS7C251024LL is a high performance CMOS 1,048,576-bit Static Random Access Memory (SRAM) organized as 131,072 words × 8 bits. It is designed for portable applications where fast data access, long battery life, and simple interfacing are desired.

Equal address access and cycle times (t_{AA}, t_{RC}, t_{WC}) of 55/70/100 ns with output enable access times (t_{OE}) of 15/25/35/50 ns are ideal for high performance applications. Active high and low chip enables ($\overline{CE1}$, CE2) permit easy memory expansion with multiple-bank memory systems.

When $\overline{CE1}$ is High or CE2 is Low the device enters standby mode. The AS7C31024LL is guaranteed not to exceed 3.0 µW power consumption in standby mode. This device also returns data when V_{CC} is reduced to 1.5V, for even lower power consumption.

A write cycle is accomplished by asserting write enable ($\overline{WE}$) and both chip enables ($\overline{CE1}$, CE2). Data on the input pins I/O0-I/O7 is written on the rising edge of $\overline{WE}$ (write cycle 1) or the active-to-inactive edge of $\overline{CE1}$ or CE2 (write cycle 2). To avoid bus contention, external devices should drive I/O pins only after outputs have been disabled with output enable ($\overline{OE}$) or write enable ($\overline{WE}$).

A read cycle is accomplished by asserting output enable ($\overline{OE}$) and both chip enables ($\overline{CE1}$, CE2), with write enable ($\overline{WE}$) HIGH. The chip drives I/O pins with the data word referenced by the input address. When either chip enable or output enable is inactive, or write enable is active, output drivers stay in high-impedance mode.

The device is packaged in common industry standard packages. Chip scale BGA packaging, easy to use in manufacturing, provides the smallest possible footprint. This 48-ball JEDEC registered package has a ball pitch of 0.75 mm and external dimensions of 8 mm × 6 mm.

Low power design

In the AS7C251024LL design, priority was placed on low power, while maintaining moderately high performance. To reduce standby and data retention current, a 6-transistor memory cell was utilized. Active power was reduced considerably over traditional designs by using Intelliwatt™ power reduction circuitry. With Intelliwatt, SRAM powers down unused circuits between access operations, resulting in longer cycle times and lower duty cycles, and providing incremental power savings. During periods of inactivity, Intelliwatt SRAM power consumption can be as low as fully de-activated standby power, even though the chip is enabled. This power savings, both in active and inactive modes, results in longer battery life, and better system marketability. All chip inputs and outputs are TTL-compatible, and operation is from a single 2.3-3.0V supply.

Intelliwatt® is a trademark of Alliance Semiconductor.

DID 11-20017-A.