

Features

128Kx8 bits Monolithic CMOS Static

Random Access Memory

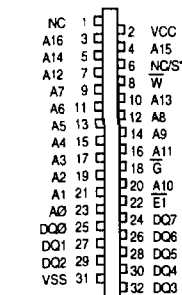
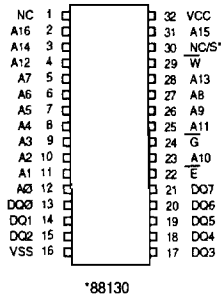
- Access Times: 70, 85 and 100ns
- Available with Single (EDI88128) or Dual (EDI88130) Chip Selects
- Battery Back-up Operation
2V Data Retention (LP Versions)
- \bar{E} & \bar{G} Functions for Bus Control
- Inputs and Outputs Directly TTL Compatible
- Fully Static, No Clocks

Three Ceramic Package Options, JEDEC Pinout

- 32 Pin Ceramic DIP, 0.6 mils wide, No. 9
- 32 Pin Ceramic ZIP, No. 100
- 32 Lead Ceramic CSOJ, No. 141

Single +5V ($\pm 10\%$) Supply Operation

Pin Configurations and Block Diagram



128Kx8 Monolithic CMOS Static RAM, High Speed

The EDI88128C is a high speed, high performance, monolithic Static RAM organized as 128Kx8 bits.

The device is also available as EDI88130C with an additional chip select line (S) which will automatically power down the device when proper logic levels are applied.

The second chip select (S) line can be used to provide system memory security during power down in non-battery backed up systems and simplify decoding schemes in memory banking where large multiple pages of memory are required.

Low power versions, EDI88128LP and EDI88130LP, offer a 2V data retention function for battery back-up applications.

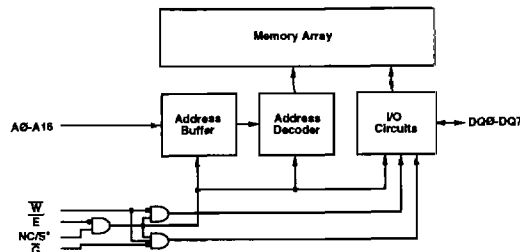
The EDI88128C and the EDI88130C have eight bi-directional input-output lines to provide simultaneous access to all bits in a word.

An automatic power down feature permits the on-chip circuitry to enter a very low standby power mode and be brought back into operation at a speed equal to the address access time.

Military product is available compliant to Appendix A of Mil-PRF-38535.

Pin Names

| | |
|-----------|-------------------------|
| A0-A16 | Address Inputs |
| \bar{E} | Chip Enable |
| S | Chip Select |
| W | Write Enable |
| \bar{G} | Output Enable |
| DQ0-DQ7 | Data Input/Output |
| VCC | Power (+5V $\pm 10\%$) |
| VSS | Ground |
| NC | No Connection |



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Absolute Maximum Ratings*

| | |
|------------------------------------|-----------------|
| Voltage on any pin relative to VSS | -0.5V to 7.0V |
| Operating Temperature TA (Ambient) | |
| Commercial | 0°C to +70°C |
| Industrial | -40°C to +85°C |
| Military | -55°C to +125°C |
| Storage Temperature | -65°C to +150°C |
| Power Dissipation | 1 Watt |
| Output Current | 20 mA |
| Junction Temperature, TJ | 175°C |

*Stress greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions greater than those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Recommended DC Operating Conditions

| Parameter | Sym | Min | Typ | Max | Units |
|--------------------|-----|------|-----|---------|-------|
| Supply Voltage | VCC | 4.5 | 5.0 | 5.5 | V |
| Supply Voltage | VSS | 0 | 0 | 0 | V |
| Input High Voltage | VIH | 2.2 | -- | VCC+0.5 | V |
| Input Low Voltage | VIL | -0.3 | -- | 0.8 | V |

AC Test Conditions

| | |
|--------------------------------|-------------|
| Input Pulse Levels | VSS to 3.0V |
| Input Rise and Fall Times | 5ns |
| Input and Output Timing Levels | 1.5V |
| Output Load | Figure 1 |

(note: For TEHQZ, TGHQZ and TWLQZ, Figure 2)

Figure 1

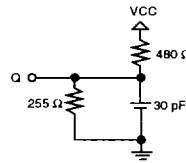
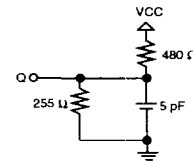


Figure 2



DC Electrical Characteristics

| Parameter | Sym | Conditions | Min | Typ* | Max | Units |
|------------------------|------|--|-----|------|-----|---------|
| Operating Power | ICC1 | $\bar{W}, \bar{E} = VIL, I/O = 0mA, \text{Min Cycle}$ | -- | | 95 | mA |
| Supply Current | | $S = VIH$ | | | | |
| Standby (TTL) Power | ICC2 | $\bar{E} \geq VIH \text{ \&/or } S \leq VIL,$ | -- | | 10 | mA |
| Supply Current | | $VIN \geq VIH \text{ or } \leq VIL$ | | | | |
| Full Standby Power | ICC3 | $\bar{E} \geq VCC-0.2V \text{ \&/or } S \leq VCC+0.2V$ | C | 1 | 5 | mA |
| Supply Current | | $VIN \geq VCC-0.2V \text{ or } VIN \leq 0.2V$ | LP | -- | 1 | mA |
| Input Leakage Current | ILI | $VIN = 0V \text{ to } VCC$ | -5 | -- | 5 | μA |
| Output Leakage Current | ILO | $V I/O = 0V \text{ to } VCC, \bar{E} \geq VIH \text{ \&/or } S \leq VIL$ | -10 | -- | 10 | μA |
| Output High Voltage | VOH | $IOH = -1.0mA$ | 2.4 | -- | -- | V |
| Output Low Voltage | VOL | $IOL = 2.1mA$ | -- | -- | 0.4 | V |

*Typical: TA=25°C, VCC=5.0V

Truth Table

| \bar{G} | \bar{E} | \bar{S} | W | Mode | Output | Power |
|-----------|-----------|-----------|---|-----------------|--------|------------|
| X | H | X | X | Standby | High Z | ICC2, ICC3 |
| X | X | L | X | Standby | High Z | ICC2, ICC3 |
| X | X | L | X | Output Deselect | High Z | ICC1 |
| H | L | H | H | Output Deselect | High Z | ICC1 |
| L | L | H | H | Read | DOUT | ICC1 |
| X | L | H | L | Write | High Z | ICC1 |

Capacitance

(f=1.0MHz, VIN=VCC or VSS)

| Parameter | Sym | Max | Unit |
|--------------------|------|-----|------|
| Address Lines | CI | 12 | pF |
| Input/Output Lines | CD/Q | 14 | pF |

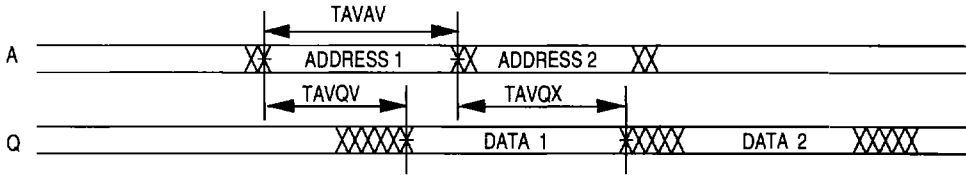
These parameters are sampled, not 100% tested

AC Characteristics Read Cycle

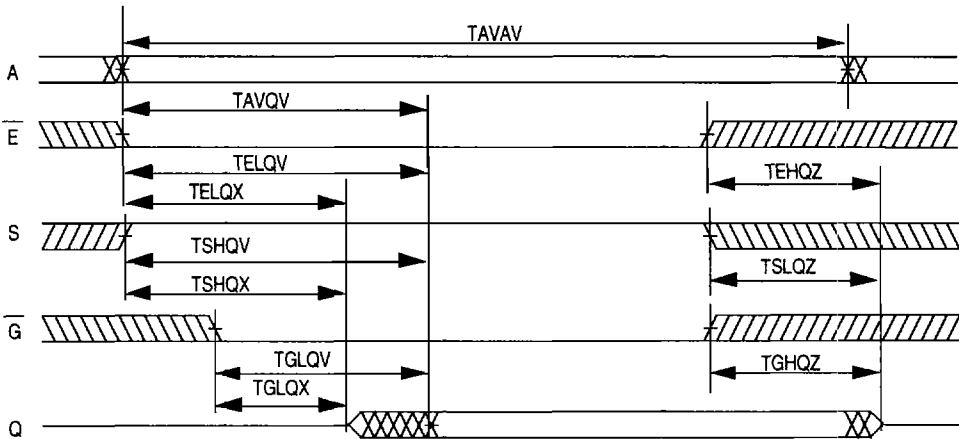
| Parameter | Symbol | | 70ns | | 85ns | | 100ns | | Units |
|--|--------|------|------|-----|------|-----|-------|-----|-------|
| | JEDEC | Alt. | Min | Max | Min | Max | Min | Max | |
| Read Cycle Time | TAVAV | TRC | 70 | | 85 | | 100 | | ns |
| Address Access Time | TAVQV | TAA | | 70 | | 85 | | 100 | ns |
| Chip Enable Access Time | TELQV | TACS | | 70 | | 85 | | 100 | ns |
| | TSHQV | TACS | | 70 | | 85 | | 100 | ns |
| Chip Enable to Output in Low Z (1) | TELQX | TCLZ | 3 | | 3 | | 3 | | ns |
| | TSHQX | TCLZ | 3 | | 3 | | 3 | | ns |
| Chip Disable to Output in High Z (1) | TEHQZ | TCHZ | 0 | 30 | 0 | 35 | 0 | 40 | ns |
| | TSLOZ | TCHZ | 0 | 30 | 0 | 35 | 0 | 40 | ns |
| Output Hold from Address Change | TAVQX | TOH | 3 | | 3 | | 3 | | ns |
| Output Enable to Output Valid | TGLQV | TOE | | 35 | | 45 | | 50 | ns |
| Output Enable to Output in Low Z (1) | TGLQX | TOLZ | 0 | | 0 | | 0 | | ns |
| Output Disable to Output in High Z (1) | TGHQZ | TOHZ | 0 | 30 | 0 | 35 | 0 | 35 | ns |

Note 1: Parameter guaranteed, but not tested.

Read Cycle 1 - W, S High; G, E Controlled



Read Cycle 2 - W High



2

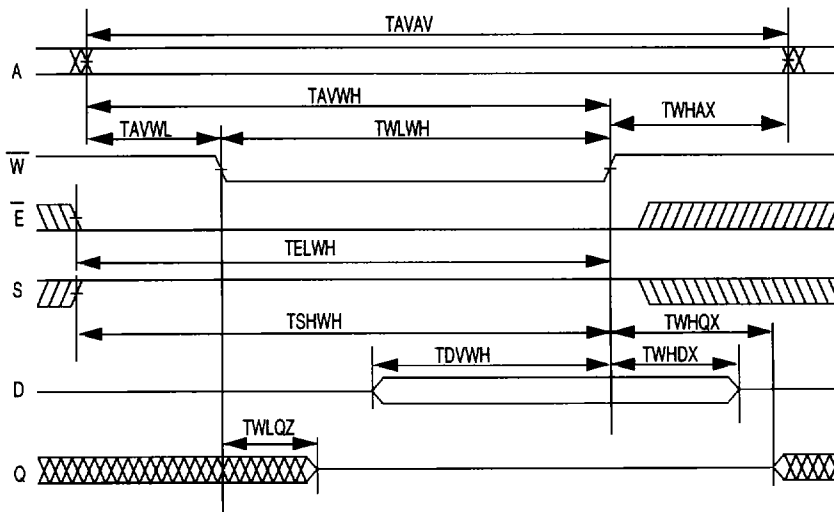


AC Characteristics Write Cycle

| Parameter | Symbol | | 70ns | | 85ns | | 100ns | | Units |
|-------------------------------------|--------|-------|------|-----|------|-----|-------|-----|-------|
| | JEDEC | Alt. | Min | Max | Min | Max | Min | Max | |
| Write Cycle Time | TAVAV | TWC | 70 | | 85 | | 100 | | ns |
| Chip Enable to End of Write | TELWH | TCW | 65 | | 70 | | 80 | | ns |
| | TELEH | TCW | 65 | | 70 | | 80 | | ns |
| | TSHWH | TCW | 65 | | 70 | | 80 | | ns |
| | TSHSL | TCW | 65 | | 70 | | 80 | | ns |
| Address Setup Time | TAVWL | TAS | 0 | | 0 | | 0 | | ns |
| | TAVEL | TAS | 0 | | 0 | | 0 | | ns |
| | TAVSH | TAS | 0 | | 0 | | 0 | | ns |
| Address Valid to End of Write | TAVWH | TAW | 65 | | 70 | | 80 | | ns |
| Write Pulse Width | TWLWH | TWP | 65 | | 70 | | 80 | | ns |
| | TWLEH | TWP | 65 | | 70 | | 80 | | ns |
| | TWLSL | TWP | 65 | | 70 | | 80 | | ns |
| Write Recovery Time | TWHAX | TWR | 0 | | 0 | | 0 | | ns |
| | TEHAX | TWR | 0 | | 0 | | 0 | | ns |
| | TSLAX | TWR | 0 | | 0 | | 0 | | ns |
| Data Hold Time | TWHDX | TDH | 0 | | 0 | | 0 | | ns |
| | TEHDX | TDH | 0 | | 0 | | 0 | | ns |
| | TSLDX | TDH | 0 | | 0 | | 0 | | ns |
| Write to Output in High Z (1) | TWLQZ | TW-HZ | 0 | 30 | 0 | 35 | 0 | 40 | ns |
| Data to Write Time | TDVWH | TDW | 30 | | 35 | | 40 | | ns |
| | TDVEH | TDW | 30 | | 35 | | 40 | | ns |
| | TDVSL | TDW | 30 | | 35 | | 40 | | ns |
| Output Active from End of Write (1) | TWHQX | TWLZ | 5 | | 5 | | 5 | | ns |

Note 1: Parameter guaranteed, but not tested.

Write Cycle 1 - Late Write, W Controlled



Data Retention Characteristics

EDI88128LP & EDI88130LP Only

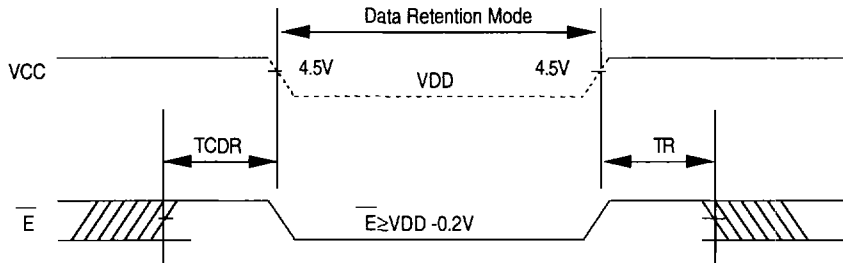
(TA = -55°C to +125°C)

| Characteristic | Sym | Test Conditions | Min | Typ | Max | Unit |
|--|-------|---------------------------|--------|-----|-----|---------|
| Data Retention Voltage | VDD | VDD = 2.0V | 2 | -- | -- | V |
| Data Retention Quiescent Current | ICCDR | $\bar{E} \geq VDD - 0.2V$ | -- | -- | 400 | μA |
| Chip Disable to Data Retention Time(1) | TCDR | VIN \geq VDD - 0.2V | 0 | -- | -- | ns |
| Operation Recovery Time (1) | TR | or VIN \leq 0.2V | TAVAV* | | -- | ns |

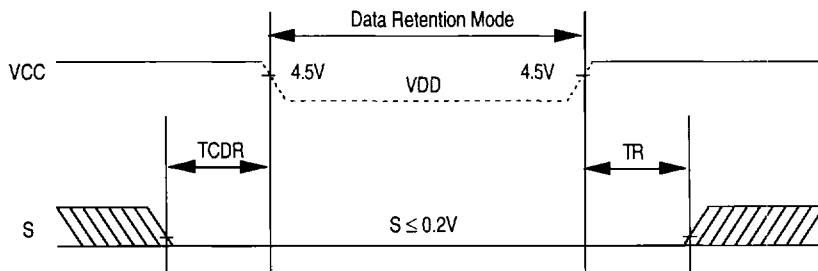
Note 1: Parameter guaranteed, but not tested.

*Read Cycle Time

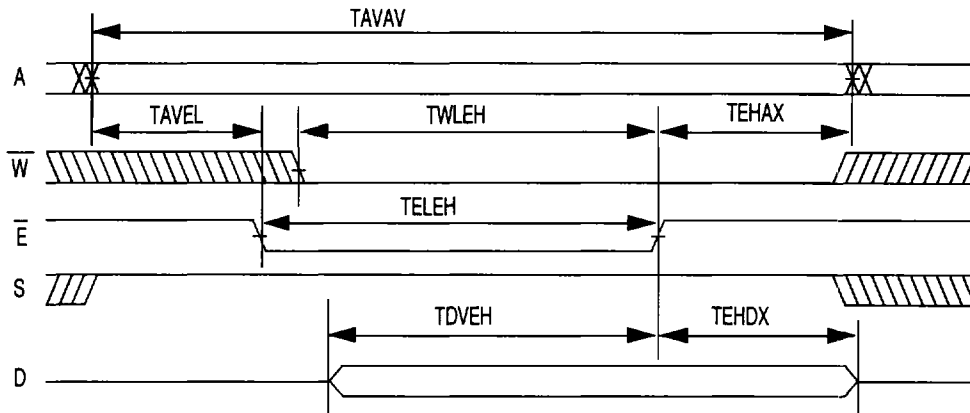
Data Retention E Controlled



Data Retention S Controlled

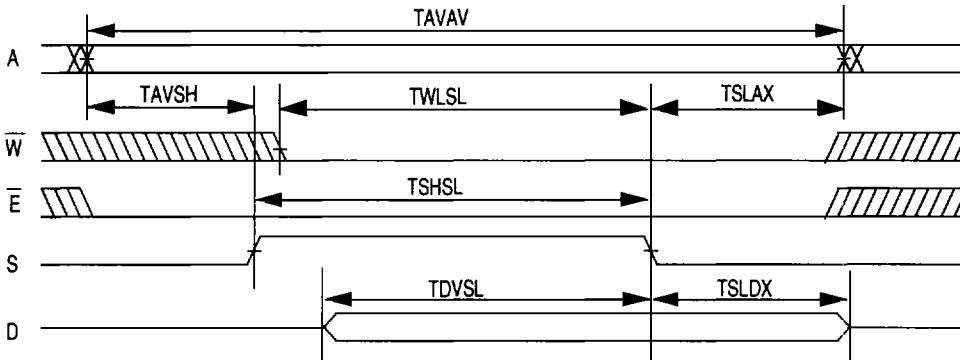


Write Cycle 2 - Early Write E Controlled



2

Write Cycle 3 - Early Write S Controlled



Ordering Information

Single Chip Enable, Military

| | Speed | Package |
|-----------------------|-------|---------|
| Standard Power | ns | No. |
| EDI88128C70CB | 70 | 9 |
| EDI88128C85CB | 85 | 9 |
| EDI88128C100CB | 100 | 9 |
| EDI88128C70NB | 70 | 140 |
| EDI88128C85NB | 85 | 140 |
| EDI88128C100NB | 100 | 140 |
| EDI88128C70ZB | 70 | 100 |
| EDI88128C85ZB | 85 | 100 |
| EDI88128C100ZB | 100 | 100 |

| | Speed | Package |
|------------------|-------|---------|
| Low Power | ns | No. |
| EDI88128LP70CB | 70 | 9 |
| EDI88128LP85CB | 85 | 9 |
| EDI88128LP100CB | 100 | 9 |
| EDI88128LP70NB | 70 | 140 |
| EDI88128LP85NB | 85 | 140 |
| EDI88128LP100NB | 100 | 140 |
| EDI88128LP70ZB | 70 | 100 |
| EDI88128LP85ZB | 85 | 100 |
| EDI88128LP100ZB | 100 | 100 |

2

Dual Chip Enable, Military

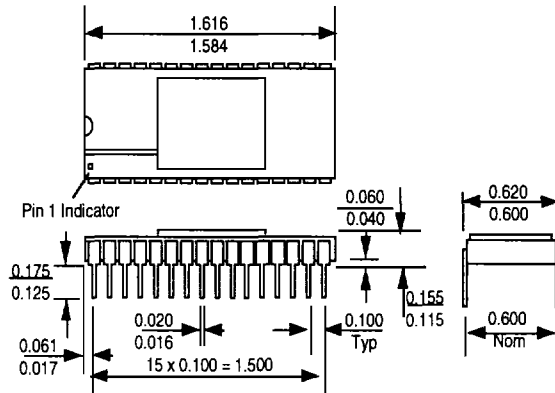
| | Speed | Package |
|-----------------------|-------|---------|
| Standard Power | ns | No. |
| EDI88130C70CB | 70 | 9 |
| EDI88130C85CB | 85 | 9 |
| EDI88130C100CB | 100 | 9 |
| EDI88130C70NB | 70 | 140 |
| EDI88130C85NB | 85 | 140 |
| EDI88130C100NB | 100 | 140 |
| EDI88130C70ZB | 70 | 100 |
| EDI88130C85ZB | 85 | 100 |
| EDI88130C100ZB | 100 | 100 |

| | Speed | Package |
|------------------|-------|---------|
| Low Power | ns | No. |
| EDI88130LP70CB | 70 | 9 |
| EDI88130LP85CB | 85 | 9 |
| EDI88130LP100CB | 100 | 9 |
| EDI88130LP70NB | 70 | 140 |
| EDI88130LP85NB | 85 | 140 |
| EDI88130LP100NB | 100 | 140 |
| EDI88130LP70ZB | 70 | 100 |
| EDI88130LP85ZB | 85 | 100 |
| EDI88130LP100ZB | 100 | 100 |

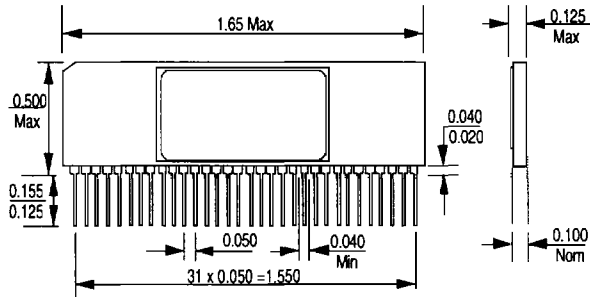
For Commercial, Industrial or Military grade product use C, I or M respectively, to replace B in the suffix of the part number, e.g. EDI88128C70CB becomes EDI88128C70CC (Commercial temp. range), EDI88128C70CI (Industrial temp. range), or EDI88128C70CM (Military temp range).

Package Description

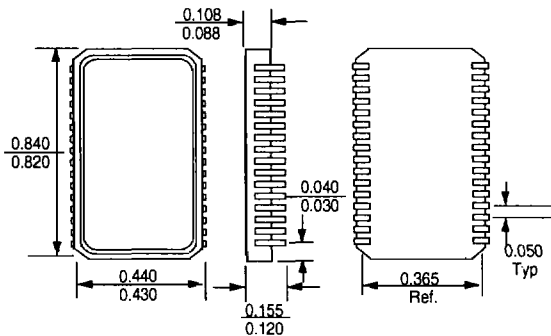
Package No. 9
32 Pin Ceramic Sidebrazed
Dual-in-line Package
600 mils wide



Package No. 100
32 pin Ceramic Zip



Package No. 140
32 lead CSOJ,
Ceramic J-Leaded
Chip Carrier



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