Document Title

Multi-Chip Package MEMORY

64M Bit (8Mx8/4Mx16) Dual Bank NOR Flash *2 / 128M Bit (8Mx16) NAND Flash / 64M Bit (4Mx16) UtRAM

Revision History

Revision No.	History	Draft Date	Remark
0.0	Initial Draft	October 15, 2002	Preliminary
1.0	Changed UtRAM Parameters - Icc1u(max): 10mA to 15mA - Icc2u(max): 40mA to 45mA - Isb2u(typ): 80uA to 150uA - Isb2u(max): 100uA to 200uA - t_{PC}(Page Cycle): 25ns to 30ns - t_{PA}(Page Access Time): 20ns to 25ns	January 6, 2003	Final
1.1	<NAND Flash> Changed Parameters - Eudurance Cycles : 1,000 to 10,000 Program/Erase Cycles Maximum without ECC - Number Of Partial Program(NOP) : 2Cycles(Main)/ 3Cycles(Spare) to 1Cycle/1Cycle(Main & Spare) <U*t*RAM> - Changed I_{SBD} (max) from 10uA to 20uA - Errata correction Changed U*t*RAM Standby Current in Standby Mode Characteristic(U*t*RAM) from 100uA into 200uA	June 10, 2003	Final
1.2	Revised(NOR) - Release the stand-by current from typ. 5uA(max.18uA) to typ. 10uA(max. 30uA).	June 19, 2003	Final

Note : For more detailed features and specifications including FAQ, please refer to Samsung's web site.
http://samsungelectronics.com/semiconductors/products/products_index.html

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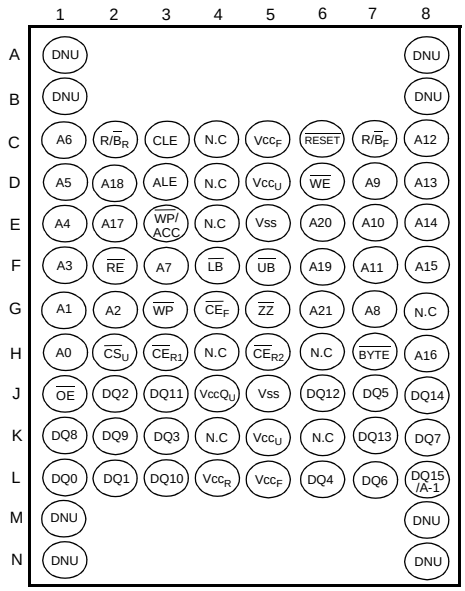
64M Bit (8Mx8/4Mx16) Dual Bank NOR Flash *2 / 128M Bit (8Mx16) NAND Flash / 64M Bit (4Mx16) UtRAM

FEATURES

- Power Supply Voltage : 2.7V~3.1V
- Organization
  - NOR Flash : 8,388,608 x 8 bit *2 / 4,194,304 x 16 bit *2
  - NAND Flash : (8M + 256K)bit x 16bit
  - UtRAM : 4Mbit x 16 bit
- Access Time
  - NOR Flash : 70ns(Max.)
  - NAND Flash : Random - 10us(Max.), Serial - 50ns(Min.)
  - UtRAM : 70ns
- Power Consumption (typical value)
  - NOR Flash(each device) Read Current : 14mA (@5MHz)
    Program/Erase Current : 15mA
    Read while Program or Read while Erase : 35mA
    Standby Mode/Autosleep Mode : 10µA
  - NAND Flash Read Current : 10mA(@20MHz)
    Program/Erase Current : 10mA
    Standby Current : 10µA
  - UtRAM Operating Current : 35mA
    Standby Current : 150µA
- NOR Flash Secode(Security Code) Block : Extra 64KB Block
- NOR Flash Block Group Protection / Unprotection
- NOR Flash Bank Size : 16Mb / 48Mb
- NAND Flash Automatic Program and Erase
  Page Program: (256 + 8)Word, Block Erase: (8K + 256)Word
- NAND Flash Fast Write Cycle Time
  Program time : 200µs(Typ.)
  Block Erase Time : 2ms(Typ.)
- Endurance
  NOR : 100,000 Program/Erase Cycles Minimum
  NAND : 100,000 Program/Erase Cycles Minimum with ECC
  : 10,000 Program/Erase Cycles Maximum without ECC
- Data Retention : 10 years
- Operating Temperature : -25°C ~ 85°C
- Package : 80 - Ball TBGA Type - 8 x 13mm, 0.8 mm pitch

BALL CONFIGURATION



80 Ball TBGA , 0.8mm Pitch
Top View (Ball Down)

GENERAL DESCRIPTION

The KBB0xA500M featuring single 3.0V power supply is a Multi Chip Package Memory which combines two 64Mbit NOR Flash, 128Mbit NAND Flash and 64Mbit Unit Transistor CMOS RAM. 64Mbit NOR Flash memory is organized as 8M x8 or 4M x16 bit, 128Mbit NAND Flash memory is organized as 8M x16 bit and 64Mbit UtRAM is organized as 4M x16 bit. The memory architecture of NOR Flash memory is designed to divide its memory arrays into 135 blocks and this provides highly flexible erase and program capability. This device is capable of reading data from one bank while programming or erasing in the other bank with dual bank organization. NOR Flash memory performs a program operation in units of 8 bits (Byte) or 16 bits (Word) and erases in units of a block. Single or multiple blocks can be erased. The block erase operation is completed for typically 0.7sec.

In 128Mbit NAND Flash a 256-word page program can be typically achieved within 200µs and an 8K-word block erase can be typically achieved within 2ms. In serial read operation, a byte can be read by 50ns. DQ pins serve as the ports for address and data input/output as well as command inputs. The KBB0xA500M is suitable for the memory of mobile communication system to reduce not only mount area but also power consumption. This device is available in 80-ball TBGA package.

BALL DESCRIPTION

Ball Name	Description
A0 to A21	Address Input Balls (NOR, UtRAM)
A-1	Address Input Balls (NOR)
DQ0 to DQ7	Data Input/Output Balls (Common)
DQ8 to DQ15	Data Input/Output Balls (Common)
Vcc_R	Power Supply (NOR)
Vcc_F	Power Supply (NAND)
Vcc_U	Power Supply (UtRAM)
$VccQ_U$	Data Output Buffer Power (UtRAM)
Vss	Ground (Common)
$\overline{WE}$	Write Enable (Common)
$\overline{OE}$	Output Enable (NOR,UtRAM)
$\overline{CE}_{R1}$	Chip Enable (NOR)
$\overline{CE}_{R2}$	Chip Enable (NOR)
$\overline{CE}_F$	Chip Enable (NAND)
$\overline{CS}_U$	Chip Enable (UtRAM)
$\overline{RESET}$	Hardware Reset (NOR)
$\overline{WP}$/ACC	Hardware Write Protection/Program Acceleration (NOR)
$\overline{BYTE}$	Byte Control (NOR)
$R/\overline{B}_R$	Read/Busy (NOR)
$\overline{WP}$	Write Protection (NAND)
CLE	Command Latch Enable(NAND)
ALE	Address Latch Enable(NAND)
$R/\overline{B}_F$	Read/Busy (NAND)
$\overline{RE}$	Output Enable (NAND)
$\overline{ZZ}$	Deep Power Down (UtRAM)
$\overline{UB}$	Upper Byte Enable (UtRAM)
$\overline{LB}$	Lower Byte Enable (UtRAM)
N.C	No Connection
DNU	Do Not Use

ORDERING INFORMATION

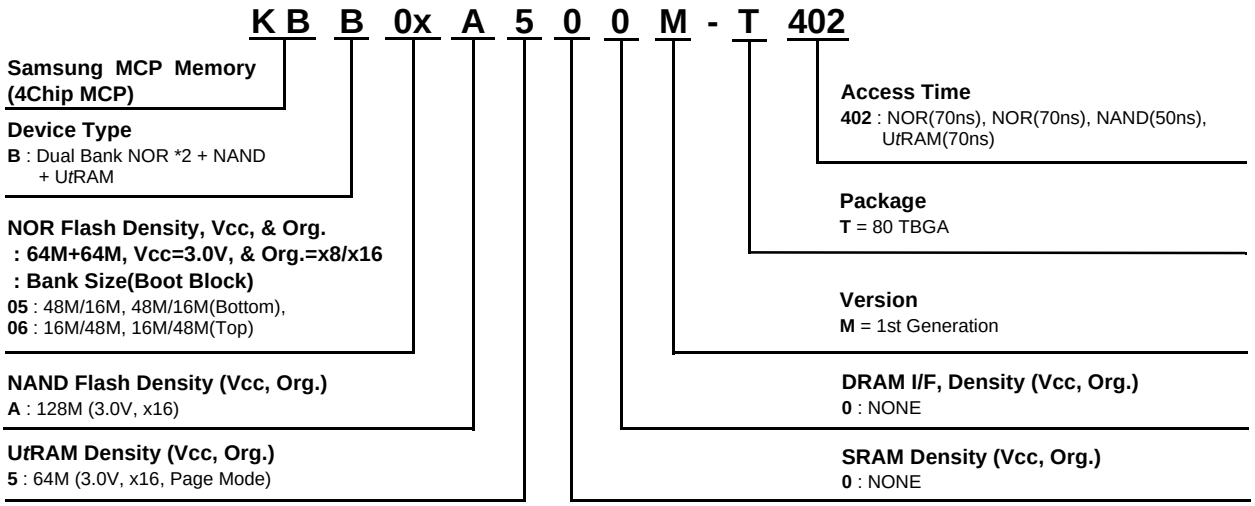


Figure 1. FUNCTIONAL BLOCK DIAGRAM

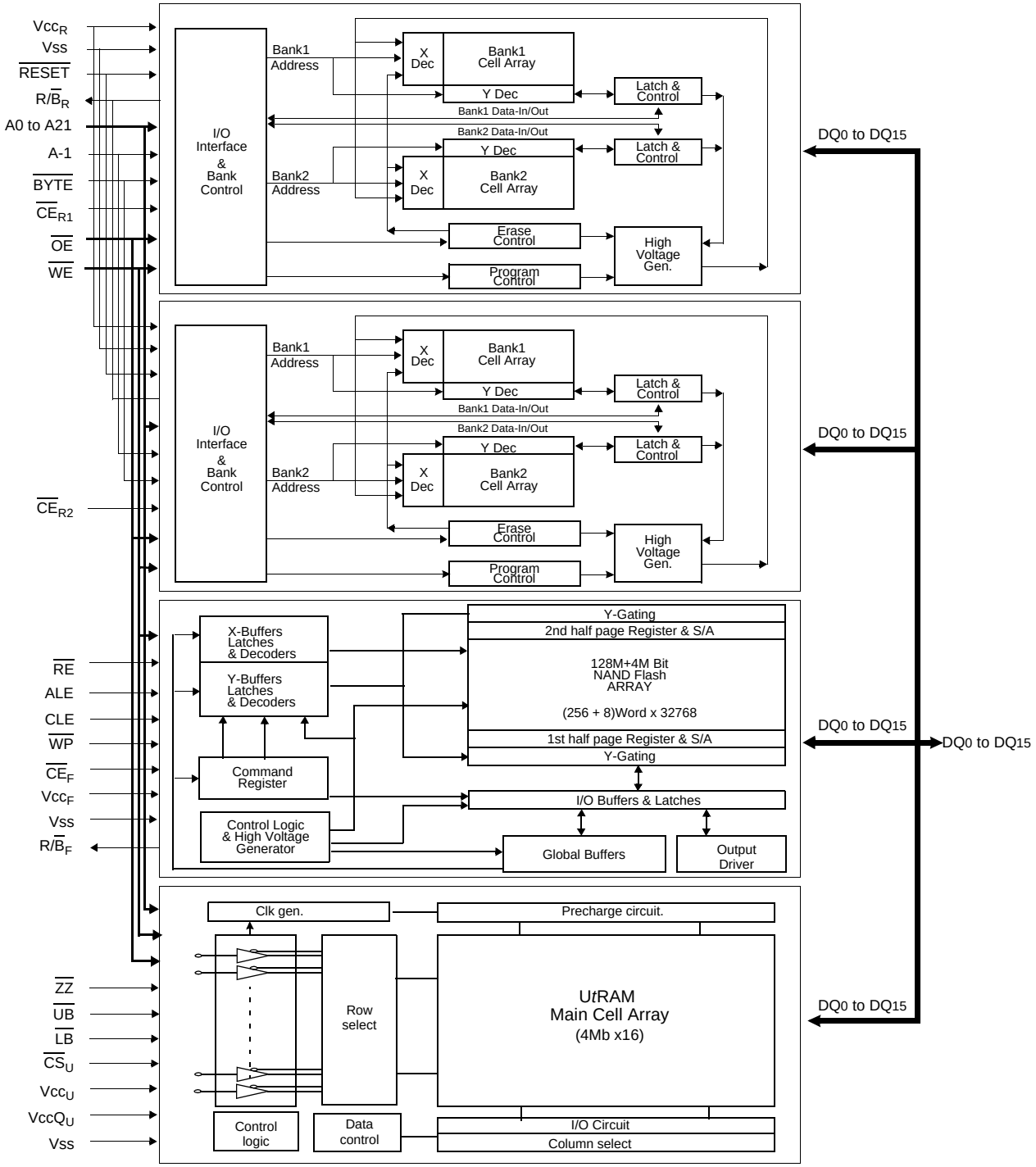
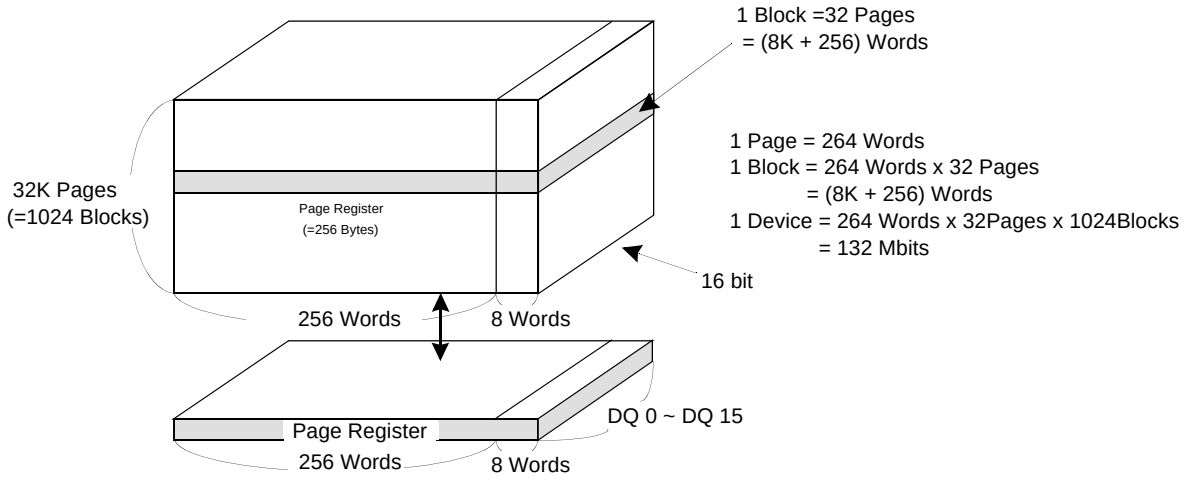


Figure 2. NAND Flash ARRAY ORGANIZATION



	DQ 0	DQ 1	DQ 2	DQ 3	DQ 4	DQ 5	DQ 6	DQ 7	DQ8 to 15	
1st Cycle	A_0	A_1	A_2	A_3	A_4	A_5	A_6	A_7	*L	**Column Address**
2nd Cycle	A_9	A_{10}	A_{11}	A_{12}	A_{13}	A_{14}	A_{15}	A_{16}	*L	**Row Address**
3rd Cycle	A_{17}	A_{18}	A_{19}	A_{20}	A_{21}	A_{22}	A_{23}	*L	*L	**(Page Address)**

NOTE: Column Address : Starting Address of the Register.

* L must be set to "Low"

Table 1. NOR Flash Memory Top Boot Block Address (KBB06A500)

KBB06A500	Block	Block Address										Block Size (KB/KW)	Address Range	
		A21	A20	A19	A18	A17	A16	A15	A14	A13	A12		Byte Mode	Word Mode
Bank1	BA134	1	1	1	1	1	1	1	1	1	1	8/4	7FE000H-7FFFFFH	3FF000H-3FFFFFH
	BA133	1	1	1	1	1	1	1	1	1	0	8/4	7FC000H-7FDFFFH	3FE000H-3FEFFFH
	BA132	1	1	1	1	1	1	1	1	0	1	8/4	7FA000H-7FBFFFH	3FD000H-3FDFFFH
	BA131	1	1	1	1	1	1	1	1	0	0	8/4	7F8000H-7F9FFFH	3FC000H-3FCFFFH
	BA130	1	1	1	1	1	1	1	0	1	1	8/4	7F6000H-7F7FFFH	3FB000H-3FBFFFH
	BA129	1	1	1	1	1	1	1	0	1	0	8/4	7F4000H-7F5FFFH	3FA000H-3FAFFFH
	BA128	1	1	1	1	1	1	1	0	0	1	8/4	7F2000H-7F3FFFH	3F9000H-3F9FFFH
	BA127	1	1	1	1	1	1	1	0	0	0	8/4	7F0000H-7F1FFFH	3F8000H-3F8FFFH
	BA126	1	1	1	1	1	1	0	X	X	X	64/32	7E0000H-7EFFFFH	3F0000H-3F7FFFH
	BA125	1	1	1	1	1	0	1	X	X	X	64/32	7D0000H-7DFFFFH	3E8000H-3EFFFFH
	BA124	1	1	1	1	1	0	0	X	X	X	64/32	7C0000H-7CFFFFH	3E0000H-3E7FFFH
	BA123	1	1	1	1	0	1	1	X	X	X	64/32	7B0000H-7BFFFFH	3D8000H-3DFFFFH
	BA122	1	1	1	1	0	1	0	X	X	X	64/32	7A0000H-7AFFFFH	3D0000H-3D7FFFH
	BA121	1	1	1	1	0	0	1	X	X	X	64/32	790000H-79FFFFH	3C8000H-3CFFFFH
	BA120	1	1	1	1	0	0	0	X	X	X	64/32	780000H-78FFFFH	3C0000H-3C7FFFH
	BA119	1	1	1	0	1	1	1	X	X	X	64/32	770000H-77FFFFH	3B8000H-3BFFFFH
	BA118	1	1	1	0	1	1	0	X	X	X	64/32	760000H-76FFFFH	3B0000H-3B7FFFH
	BA117	1	1	1	0	1	0	1	X	X	X	64/32	750000H-75FFFFH	3A8000H-3AFFFFH
	BA116	1	1	1	0	1	0	0	X	X	X	64/32	740000H-74FFFFH	3A0000H-3A7FFFH
	BA115	1	1	1	0	0	1	1	X	X	X	64/32	730000H-73FFFFH	398000H-39FFFFH
	BA114	1	1	1	0	0	1	0	X	X	X	64/32	720000H-72FFFFH	390000H-397FFFH
	BA113	1	1	1	0	0	0	1	X	X	X	64/32	710000H-71FFFFH	388000H-38FFFFH
	BA112	1	1	1	0	0	0	0	X	X	X	64/32	700000H-70FFFFH	380000H-387FFFH
	BA111	1	1	0	1	1	1	1	X	X	X	64/32	6F0000H-6FFFFFH	378000H-37FFFFH
	BA110	1	1	0	1	1	1	0	X	X	X	64/32	6E0000H-6EFFFFH	370000H-377FFFH
	BA109	1	1	0	1	1	0	1	X	X	X	64/32	6D0000H-6DFFFFH	368000H-36FFFFH
	BA108	1	1	0	1	1	0	0	X	X	X	64/32	6C0000H-6CFFFFH	360000H-367FFFH
	BA107	1	1	0	1	0	1	1	X	X	X	64/32	6B0000H-6BFFFFH	358000H-35FFFFH
	BA106	1	1	0	1	0	1	0	X	X	X	64/32	6A0000H-6AFFFFH	350000H-357FFFH
	BA105	1	1	0	1	0	0	1	X	X	X	64/32	690000H-69FFFFH	348000H-34FFFFH
	BA104	1	1	0	1	0	0	0	X	X	X	64/32	680000H-68FFFFH	340000H-347FFFH
	BA103	1	1	0	0	1	1	1	X	X	X	64/32	670000H-67FFFFH	338000H-33FFFFH
	BA102	1	1	0	0	1	1	0	X	X	X	64/32	660000H-66FFFFH	330000H-337FFFH
	BA101	1	1	0	0	1	0	1	X	X	X	64/32	650000H-65FFFFH	328000H-32FFFFH
	BA100	1	1	0	0	1	0	0	X	X	X	64/32	640000H-64FFFFH	320000H-327FFFH
	BA99	1	1	0	0	0	1	1	X	X	X	64/32	630000H-63FFFFH	318000H-31FFFFH

Table 1. NOR Flash Memory Top Boot Block Address (KBB06A500)

KBB06A500	Block	Block Address										Block Size (KB/KW)	Address Range	
		A21	A20	A19	A18	A17	A16	A15	A14	A13	A12		Byte Mode	Word Mode
Bank1	BA98	1	1	0	0	0	1	0	X	X	X	64/32	620000H-62FFFFH	310000H-317FFFH
	BA97	1	1	0	0	0	0	1	X	X	X	64/32	610000H-61FFFFH	308000H-30FFFFH
	BA96	1	1	0	0	0	0	0	X	X	X	64/32	600000H-60FFFFH	300000H-307FFFH
Bank2	BA95	1	0	1	1	1	1	1	X	X	X	64/32	5F0000H-5FFFFFH	2F8000H-2FFFFFH
	BA94	1	0	1	1	1	1	0	X	X	X	64/32	5E0000H-5EFFFFH	2F0000H-2F7FFFH
	BA93	1	0	1	1	1	0	1	X	X	X	64/32	5D0000H-5DFFFFH	2E8000H-2EFFFFH
	BA92	1	0	1	1	1	0	0	X	X	X	64/32	5C0000H-5CFFFFH	2E0000H-2E7FFFH
	BA91	1	0	1	1	0	1	1	X	X	X	64/32	5B0000H-5BFFFFH	2D8000H-2DFFFFH
	BA90	1	0	1	1	0	1	0	X	X	X	64/32	5A0000H-5AFFFFH	2D0000H-2D7FFFH
	BA89	1	0	1	1	0	0	1	X	X	X	64/32	590000H-59FFFFH	2C8000H20CFFFFH
	BA88	1	0	1	1	0	0	0	X	X	X	64/32	580000H-58FFFFH	2C0000H-2C7FFFH
	BA87	1	0	1	0	1	1	1	X	X	X	64/32	570000H-57FFFFH	2B8000H-2BFFFFH
	BA86	1	0	1	0	1	1	0	X	X	X	64/32	560000H-56FFFFH	2B0000H-2B7FFFH
	BA85	1	0	1	0	1	0	1	X	X	X	64/32	550000H-55FFFFH	2A8000H-2AFFFFH
	BA84	1	0	1	0	1	0	0	X	X	X	64/32	540000H-54FFFFH	2A0000H-2A7FFFH
	BA83	1	0	1	0	0	1	1	X	X	X	64/32	530000H-53FFFFH	298000H-29FFFFH
	BA82	1	0	1	0	0	1	0	X	X	X	64/32	520000H-52FFFFH	290000H-297FFFH
	BA81	1	0	1	0	0	0	1	X	X	X	64/32	510000H-51FFFFH	288000H-28FFFFH
	BA80	1	0	1	0	0	0	0	X	X	X	64/32	500000H-50FFFFH	280000H-287FFFH
	BA79	1	0	0	1	1	1	1	X	X	X	64/32	4F0000H-4FFFFFH	278000H-27FFFFH
	BA78	1	0	0	1	1	1	0	X	X	X	64/32	4E0000H-4EFFFFH	270000H-277FFFH
	BA77	1	0	0	1	1	0	1	X	X	X	64/32	4D0000H-4DFFFFH	268000H-26FFFFH
	BA76	1	0	0	1	1	0	0	X	X	X	64/32	4C0000H-4CFFFFH	260000H-267FFFH
	BA75	1	0	0	1	0	1	1	X	X	X	64/32	4B0000H-4BFFFFH	258000H-25FFFFH
	BA74	1	0	0	1	0	1	0	X	X	X	64/32	4A0000H-4AFFFFH	250000H-257FFFH
	BA73	1	0	0	1	0	0	1	X	X	X	64/32	490000H-49FFFFH	248000H-24FFFFH
	BA72	1	0	0	1	0	0	0	X	X	X	64/32	480000H-48FFFFH	240000H-247FFFH
	BA71	1	0	0	0	1	1	1	X	X	X	64/32	470000H-47FFFFH	238000H-23FFFFH

Table 1. NOR Flash Memory Top Boot Block Address (KBB06A500)

KBB06A500	Block	Block Address										Block Size (KB/KW)	Address Range	
		A21	A20	A19	A18	A17	A16	A15	A14	A13	A12		Byte Mode	Word Mode
Bank2	BA70	1	0	0	0	1	1	0	X	X	X	64/32	460000H-46FFFFH	230000H-237FFFH
	BA69	1	0	0	0	1	0	1	X	X	X	64/32	450000H-45FFFFH	228000H-22FFFFH
	BA68	1	0	0	0	1	0	0	X	X	X	64/32	440000H-44FFFFH	220000H-227FFFH
	BA67	1	0	0	0	0	1	1	X	X	X	64/32	430000H-43FFFFH	218000H-21FFFFH
	BA66	1	0	0	0	0	1	0	X	X	X	64/32	420000H-42FFFFH	210000H-217FFFH
	BA65	1	0	0	0	0	0	1	X	X	X	64/32	410000H-41FFFFH	208000H-20FFFFH
	BA64	1	0	0	0	0	0	0	X	X	X	64/32	400000H-3FFFFFH	200000H-207FFFH
	BA63	0	1	1	1	1	1	1	X	X	X	64/32	3F0000H-3FFFFFH	1F8000H-1FFFFFH
	BA62	0	1	1	1	1	1	0	X	X	X	64/32	3E0000H-3EFFFFH	1F0000H-1F7FFFH
	BA61	0	1	1	1	1	0	1	X	X	X	64/32	3D0000H-3DFFFFH	1E8000H-1EFFFFH
	BA60	0	1	1	1	1	0	0	X	X	X	64/32	3C0000H-3CFFFFH	1E0000H-1E7FFFH
	BA59	0	1	1	1	0	1	1	X	X	X	64/32	3B0000H-3BFFFFH	1D8000H-1DFFFFH
	BA58	0	1	1	1	0	1	0	X	X	X	64/32	3A0000H-3AFFFFH	1D0000H-1D7FFFH
	BA57	0	1	1	1	0	0	1	X	X	X	64/32	390000H-39FFFFH	1C8000H-1CFFFFH
	BA56	0	1	1	1	0	0	0	X	X	X	64/32	380000H-38FFFFH	1C0000H-1C7FFFH
	BA55	0	1	1	0	1	1	1	X	X	X	64/32	370000H-37FFFFH	1B8000H-1BFFFFH
	BA54	0	1	1	0	1	1	0	X	X	X	64/32	360000H-36FFFFH	1B0000H-1B7FFFH
	BA53	0	1	1	0	1	0	1	X	X	X	64/32	350000H-35FFFFH	1A8000H-1AFFFFH
	BA52	0	1	1	0	1	0	0	X	X	X	64/32	340000H-34FFFFH	1A0000H-1A7FFFH
	BA51	0	1	1	0	0	1	1	X	X	X	64/32	330000H-33FFFFH	198000H-19FFFFH
	BA50	0	1	1	0	0	1	0	X	X	X	64/32	320000H-32FFFFH	190000H-197FFFH
	BA49	0	1	1	0	0	0	1	X	X	X	64/32	310000H-31FFFFH	188000H-18FFFFH
	BA48	0	1	1	0	0	0	0	X	X	X	64/32	300000H-30FFFFH	180000H-187FFFH
	BA47	0	1	0	1	1	1	1	X	X	X	64/32	2F0000H-2FFFFFH	178000H-17FFFFH
	BA46	0	1	0	1	1	1	0	X	X	X	64/32	2E0000H-2EFFFFH	170000H-177FFFH
	BA45	0	1	0	1	1	0	1	X	X	X	64/32	2D0000H-2DFFFFH	168000H-16FFFFH
	BA44	0	1	0	1	1	0	0	X	X	X	64/32	2C0000H-2CFFFFH	160000H-167FFFH
	BA43	0	1	0	1	0	1	1	X	X	X	64/32	2B0000H-2BFFFFH	158000H-15FFFFH
	BA42	0	1	0	1	0	1	0	X	X	X	64/32	2A0000H-2AFFFFH	150000H-157FFFH
	BA41	0	1	0	1	0	0	1	X	X	X	64/32	290000H-29FFFFH	148000H-14FFFFH
	BA40	0	1	0	1	0	0	0	X	X	X	64/32	280000H-28FFFFH	140000H-147FFFH
	BA39	0	1	0	0	1	1	1	X	X	X	64/32	270000H-27FFFFH	138000H-13FFFFH
	BA38	0	1	0	0	1	1	0	X	X	X	64/32	260000H-26FFFFH	130000H-137FFFH
	BA37	0	1	0	0	1	0	1	X	X	X	64/32	250000H-25FFFFH	128000H-12FFFFH
	BA36	0	1	0	0	1	0	0	X	X	X	64/32	240000H-24FFFFH	120000H-127FFFH
	BA35	0	1	0	0	0	1	1	X	X	X	64/32	230000H-23FFFFH	118000H-11FFFFH

Table 1. NOR Flash Memory Top Boot Block Address (KBB06A500)

KBB06A500	Block	Block Address										Block Size (KB/KW)	Address Range	
		A21	A20	A19	A18	A17	A16	A15	A14	A13	A12		Byte Mode	Word Mode
Bank2	BA34	0	1	0	0	0	1	0	X	X	X	64/32	220000H-22FFFFH	110000H-117FFFH
	BA33	0	1	0	0	0	0	1	X	X	X	64/32	210000H-21FFFFH	108000H-10FFFFH
	BA32	0	1	0	0	0	0	0	X	X	X	64/32	200000H-20FFFFH	100000H-107FFFH
	BA31	0	0	1	1	1	1	1	X	X	X	64/32	1F0000H-1FFFFFH	0F8000H-0FFFFFH
	BA30	0	0	1	1	1	1	0	X	X	X	64/32	1E0000H-1EFFFFH	0F0000H-0F7FFFH
	BA29	0	0	1	1	1	0	1	X	X	X	64/32	1D0000H-1DFFFFH	0E8000H-0EFFFFH
	BA28	0	0	1	1	1	0	0	X	X	X	64/32	1C0000H-1CFFFFH	0E0000H-0E7FFFH
	BA27	0	0	1	1	0	1	1	X	X	X	64/32	1B0000H-1BFFFFH	0D8000H-0DFFFFH
	BA26	0	0	1	1	0	1	0	X	X	X	64/32	1A0000H-1AFFFFH	0D0000H-0D7FFFH
	BA25	0	0	1	1	0	0	1	X	X	X	64/32	190000H-19FFFFH	0C8000H-0CFFFFH
	BA24	0	0	1	1	0	0	0	X	X	X	64/32	180000H-18FFFFH	0C0000H-0C7FFFH
	BA23	0	0	1	0	1	1	1	X	X	X	64/32	170000H-17FFFFH	0B8000H-0BFFFFH
	BA22	0	0	1	0	1	1	0	X	X	X	64/32	160000H-16FFFFH	0B0000H-0B7FFFH
	BA21	0	0	1	0	1	0	1	X	X	X	64/32	150000H-15FFFFH	0A8000H-0AFFFFH
	BA20	0	0	1	0	1	0	0	X	X	X	64/32	140000H-14FFFFH	0A0000H-0A7FFFH
	BA19	0	0	1	0	0	1	1	X	X	X	64/32	130000H-13FFFFH	098000H-09FFFFH
	BA18	0	0	1	0	0	1	0	X	X	X	64/32	120000H-12FFFFH	090000H-097FFFH
	BA17	0	0	1	0	0	0	1	X	X	X	64/32	110000H-11FFFFH	088000H-08FFFFH
	BA16	0	0	1	0	0	0	0	X	X	X	64/32	100000H-10FFFFH	080000H-087FFFH
	BA15	0	0	0	1	1	1	1	X	X	X	64/32	0F0000H-0FFFFFH	078000H-07FFFFH
	BA14	0	0	0	1	1	1	0	X	X	X	64/32	0E0000H-0EFFFFH	070000H-077FFFH
	BA13	0	0	0	1	1	0	1	X	X	X	64/32	0D0000H-0DFFFFH	068000H-06FFFFH
	BA12	0	0	0	1	1	0	0	X	X	X	64/32	0C0000H-0CFFFFH	060000H-067FFFH
	BA11	0	0	0	1	0	1	1	X	X	X	64/32	0B0000H-0BFFFFH	058000H-05FFFFH
	BA10	0	0	0	1	0	1	0	X	X	X	64/32	0A0000H-0AFFFFH	050000H-057FFFH
	BA9	0	0	0	1	0	0	1	X	X	X	64/32	090000H-09FFFFH	048000H-04FFFFH
	BA8	0	0	0	1	0	0	0	X	X	X	64/32	080000H-08FFFFH	040000H-047FFFH
	BA7	0	0	0	0	1	1	1	X	X	X	64/32	070000H-07FFFFH	038000H-03FFFFH
	BA6	0	0	0	0	1	1	0	X	X	X	64/32	060000H-06FFFFH	030000H-037FFFH
	BA5	0	0	0	0	1	0	1	X	X	X	64/32	050000H-05FFFFH	028000H-02FFFFH
	BA4	0	0	0	0	1	0	0	X	X	X	64/32	040000H-04FFFFH	020000H-027FFFH
	BA3	0	0	0	0	0	1	1	X	X	X	64/32	030000H-03FFFFH	018000H-01FFFFH
	BA2	0	0	0	0	0	1	0	X	X	X	64/32	020000H-02FFFFH	010000H-017FFFH
	BA1	0	0	0	0	0	0	1	X	X	X	64/32	010000H-01FFFFH	008000H-00FFFFH
	BA0	0	0	0	0	0	0	0	X	X	X	64/32	000000H-00FFFFH	000000H-007FFFH

NOTE: The bank address bits are A21 ~ A20 for KBB06A500.

Table 2. Secode Block Addresses for Top Boot Devices

Device	Block Address A21-A12	Block Size	(X8) Address Range	(X16) Address Range
KBB06A500	1111111xxx	64/32	7F0000H-7FFFFFH	3F8000H-3FFFFFH

Table 3. NOR Flash Memory Bottom Boot Block Address (KBB05A500)

KBB05A500	Block	Block Address										Block Size (KB/KW)	Address Range	
		A21	A20	A19	A18	A17	A16	A15	A14	A13	A12		Byte Mode	Word Mode
Bank2	BA134	1	1	1	1	1	1	1	X	X	X	64/32	7F0000H-7FFFFFH	3F8000H-3FFFFFH
	BA133	1	1	1	1	1	1	0	X	X	X	64/32	7E0000H-7EFFFFH	3F0000H-3F7FFFH
	BA132	1	1	1	1	1	0	1	X	X	X	64/32	7D0000H-7DFFFFH	3E8000H-3EFFFFH
	BA131	1	1	1	1	1	0	0	X	X	X	64/32	7C0000H-7CFFFFH	3E0000H-3E7FFFH
	BA130	1	1	1	1	0	1	1	X	X	X	64/32	7B0000H-7BFFFFH	3D8000H-3DFFFFH
	BA129	1	1	1	1	0	1	0	X	X	X	64/32	7A0000H-7AFFFFH	3D0000H-3D7FFFH
	BA128	1	1	1	1	0	0	1	X	X	X	64/32	790000H-79FFFFH	3C8000H-3CFFFFH
	BA127	1	1	1	1	0	0	0	X	X	X	64/32	780000H-78FFFFH	3C0000H-3C7FFFH
	BA126	1	1	1	0	1	1	1	X	X	X	64/32	770000H-77FFFFH	3B8000H-3BFFFFH
	BA125	1	1	1	0	1	1	0	X	X	X	64/32	760000H-76FFFFH	3B0000H-3B7FFFH
	BA124	1	1	1	0	1	0	1	X	X	X	64/32	750000H-75FFFFH	3A8000H-3AFFFFH
	BA123	1	1	1	0	1	0	0	X	X	X	64/32	740000H-74FFFFH	3A0000H-3A7FFFH
	BA122	1	1	1	0	0	1	1	X	X	X	64/32	730000H-73FFFFH	398000H-39FFFFH
	BA121	1	1	1	0	0	1	0	X	X	X	64/32	720000H-72FFFFH	390000H-397FFFH
	BA120	1	1	1	0	0	0	1	X	X	X	64/32	710000H-71FFFFH	388000H-38FFFFH
	BA119	1	1	1	0	0	0	0	X	X	X	64/32	700000H-70FFFFH	380000H-387FFFH
	BA118	1	1	0	1	1	1	1	X	X	X	64/32	6F0000H-6F1FFFH	378000H-37FFFFH
	BA117	1	1	0	1	1	1	0	X	X	X	64/32	6E0000H-6EFFFFH	370000H-377FFFH
	BA116	1	1	0	1	1	0	1	X	X	X	64/32	6D0000H-6DFFFFH	368000H-36FFFFH
	BA115	1	1	0	1	1	0	0	X	X	X	64/32	6C0000H-6CFFFFH	360000H-367FFFH
	BA114	1	1	0	1	0	1	1	X	X	X	64/32	6B0000H-6BFFFFH	358000H-35FFFFH
	BA113	1	1	0	1	0	1	0	X	X	X	64/32	6A0000H-6AFFFFH	350000H-357FFFH
	BA112	1	1	0	1	0	0	1	X	X	X	64/32	690000H-69FFFFH	348000H-34FFFFH
	BA111	1	1	0	1	0	0	0	X	X	X	64/32	680000H-68FFFFH	340000H-347FFFH
	BA110	1	1	0	0	1	1	1	X	X	X	64/32	670000H-67FFFFH	338000H-33FFFFH
	BA109	1	1	0	0	1	1	0	X	X	X	64/32	660000H-66FFFFH	330000H-337FFFH
	BA108	1	1	0	0	1	0	1	X	X	X	64/32	650000H-65FFFFH	328000H-32FFFFH
	BA107	1	1	0	0	1	0	0	X	X	X	64/32	640000H-64FFFFH	320000H-327FFFH
	BA106	1	1	0	0	0	1	1	X	X	X	64/32	630000H-63FFFFH	318000H-31FFFFH
	BA105	1	1	0	0	0	1	0	X	X	X	64/32	620000H-62FFFFH	310000H-317FFFH
	BA104	1	1	0	0	0	0	1	X	X	X	64/32	610000H-61FFFFH	308000H-30FFFFH
	BA103	1	1	0	0	0	0	0	X	X	X	64/32	600000H-60FFFFH	300000H-307FFFH
	BA102	1	0	1	1	1	1	1	X	X	X	64/32	5F0000H-5FFFFFH	2F8000H-2FFFFFH
	BA101	1	0	1	1	1	1	0	X	X	X	64/32	5E0000H-5EFFFFH	2F0000H-2F7FFFH
	BA100	1	0	1	1	1	0	1	X	X	X	64/32	5D0000H-5DFFFFH	2E8000H-2EFFFFH
	BA99	1	0	1	1	1	0	0	X	X	X	64/32	5C0000H-5CFFFFH	2E0000H-2E7FFFH

Table 3. NOR Flash Memory Bottom Block Address (KBB05A500)

KBB05A500	Block	Block Address										Block Size (KB/KW)	Address Range	
		A21	A20	A19	A18	A17	A16	A15	A14	A13	A12		Byte Mode	Word Mode
Bank2	BA98	1	0	1	1	0	1	1	X	X	X	64/32	5B0000H-5BFFFFH	2D8000H-2DFFFFH
	BA97	1	0	1	1	0	1	0	X	X	X	64/32	5A0000H-5AFFFFH	2D0000H-2D7FFFH
	BA96	1	0	1	1	0	0	1	X	X	X	64/32	590000H-59FFFFH	2C8000H-2CFFFFH
	BA95	1	0	1	1	0	0	0	X	X	X	64/32	580000H-58FFFFH	2C0000H-2C7FFFH
	BA94	1	0	1	0	1	1	1	X	X	X	64/32	570000H-57FFFFH	2B8000H-2BFFFFH
	BA93	1	0	1	0	1	1	0	X	X	X	64/32	560000H-56FFFFH	2B0000H-2B7FFFH
	BA92	1	0	1	0	1	0	1	X	X	X	64/32	550000H-55FFFFH	2A8000H-2AFFFFH
	BA91	1	0	1	0	1	0	0	X	X	X	64/32	540000H-54FFFFH	2A0000H-2A7FFFH
	BA90	1	0	1	0	0	1	1	X	X	X	64/32	530000H-53FFFFH	298000H-29FFFFH
	BA89	1	0	1	0	0	1	0	X	X	X	64/32	520000H-52FFFFH	290000H-297FFFH
	BA88	1	0	1	0	0	0	1	X	X	X	64/32	510000H-51FFFFH	288000H-28FFFFH
	BA87	1	0	1	0	0	0	0	X	X	X	64/32	500000H-50FFFFH	280000H-287FFFH
	BA86	1	0	0	1	1	1	1	X	X	X	64/32	4F0000H-4FFFFFH	278000H-27FFFFH
	BA85	1	0	0	1	1	1	0	X	X	X	64/32	4E0000H-4EFFFFH	270000H-277FFFH
	BA84	1	0	0	1	1	0	1	X	X	X	64/32	4D0000H-4DFFFFH	268000H-26FFFFH
	BA83	1	0	0	1	1	0	0	X	X	X	64/32	4C0000H-4CFFFFH	260000H-267FFFH
	BA82	1	0	0	1	0	1	1	X	X	X	64/32	4B0000H-4BFFFFH	258000H-25FFFFH
	BA81	1	0	0	1	0	1	0	X	X	X	64/32	4A0000H-4AFFFFH	250000H-257FFFH
	BA80	1	0	0	1	0	0	1	X	X	X	64/32	490000H-49FFFFH	248000H-24FFFFH
	BA79	1	0	0	1	0	0	0	X	X	X	64/32	480000H-48FFFFH	240000H-247FFFH
	BA78	1	0	0	0	1	1	1	X	X	X	64/32	470000H-47FFFFH	238000H-23FFFFH
	BA77	1	0	0	0	1	1	0	X	X	X	64/32	460000H-46FFFFH	230000H-237FFFH
	BA76	1	0	0	0	1	0	1	X	X	X	64/32	450000H-45FFFFH	228000H-22FFFFH
	BA75	1	0	0	0	1	0	0	X	X	X	64/32	440000H-44FFFFH	220000H-227FFFH
	BA74	1	0	0	0	0	1	1	X	X	X	64/32	430000H-43FFFFH	218000H-21FFFFH
	BA73	1	0	0	0	0	1	0	X	X	X	64/32	420000H-42FFFFH	210000H-217FFFH
	BA72	1	0	0	0	0	0	1	X	X	X	64/32	410000H-41FFFFH	208000H-20FFFFH
	BA71	1	0	0	0	0	0	0	X	X	X	64/32	400000H-40FFFFH	200000H-207FFFH

Table 3. NOR Flash Memory Bottom Boot Block Address (KBB05A500)

KBB05A500	Block	Block Address										Block Size (KB/KW)	Address Range	
		A21	A20	A19	A18	A17	A16	A15	A14	A13	A12		Byte Mode	Word Mode
Bank2	BA70	0	1	1	1	1	1	1	X	X	X	64/32	3F0000H-3FFFFFH	1F8000H-1FFFFFH
	BA69	0	1	1	1	1	1	0	X	X	X	64/32	3E0000H-3EFFFFH	1F0000H-1F7FFFH
	BA68	0	1	1	1	1	0	1	X	X	X	64/32	3D0000H-3DFFFFH	1E8000H-1EFFFFH
	BA67	0	1	1	1	1	0	0	X	X	X	64/32	3C0000H-3CFFFFH	1E0000H-1E7FFFH
	BA66	0	1	1	1	0	1	1	X	X	X	64/32	3B0000H-3BFFFFH	1D8000H-1DFFFFH
	BA65	0	1	1	1	0	1	0	X	X	X	64/32	3A0000H-3AFFFFH	1D0000H-1D7FFFH
	BA64	0	1	1	1	0	0	1	X	X	X	64/32	390000H-39FFFFH	1C8000H-1CFFFFH
	BA63	0	1	1	1	0	0	0	X	X	X	64/32	380000H-38FFFFH	1C0000H-1C7FFFH
	BA62	0	1	1	0	1	1	1	X	X	X	64/32	370000H-37FFFFH	1B8000H-1BFFFFH
	BA61	0	1	1	0	1	1	0	X	X	X	64/32	360000H-36FFFFH	1B0000H-1B7FFFH
	BA60	0	1	1	0	1	0	1	X	X	X	64/32	350000H-35FFFFH	1A8000H-1AFFFFH
	BA59	0	1	1	0	1	0	0	X	X	X	64/32	340000H-34FFFFH	1A0000H-1A7FFFH
	BA58	0	1	1	0	0	1	1	X	X	X	64/32	330000H-33FFFFH	198000H-19FFFFH
	BA57	0	1	1	0	0	1	0	X	X	X	64/32	320000H-32FFFFH	190000H-197FFFH
	BA56	0	1	1	0	0	0	1	X	X	X	64/32	310000H-31FFFFH	188000H-18FFFFH
	BA55	0	1	1	0	0	0	0	X	X	X	64/32	300000H-30FFFFH	180000H-187FFFH
	BA54	0	1	0	1	1	1	1	X	X	X	64/32	2F0000H-2F1FFFH	178000H-17FFFFH
	BA53	0	1	0	1	1	1	0	X	X	X	64/32	2E0000H-2EFFFFH	170000H-177FFFH
	BA52	0	1	0	1	1	0	1	X	X	X	64/32	2D0000H-2DFFFFH	168000H-16FFFFH
	BA51	0	1	0	1	1	0	0	X	X	X	64/32	2C0000H-2CFFFFH	160000H-167FFFH
	BA50	0	1	0	1	0	1	1	X	X	X	64/32	2B0000H-2BFFFFH	158000H-15FFFFH
	BA49	0	1	0	1	0	1	0	X	X	X	64/32	2A0000H-2AFFFFH	150000H-157FFFH
	BA48	0	1	0	1	0	0	1	X	X	X	64/32	290000H-29FFFFH	148000H-14FFFFH
	BA47	0	1	0	1	0	0	0	X	X	X	64/32	280000H-28FFFFH	140000H-147FFFH
	BA46	0	1	0	0	1	1	1	X	X	X	64/32	270000H-27FFFFH	138000H-13FFFFH
	BA45	0	1	0	0	1	1	0	X	X	X	64/32	260000H-26FFFFH	130000H-137FFFH
	BA44	0	1	0	0	1	0	1	X	X	X	64/32	250000H-25FFFFH	128000H-12FFFFH
	BA43	0	1	0	0	1	0	0	X	X	X	64/32	240000H-24FFFFH	120000H-127FFFH
	BA42	0	1	0	0	0	1	1	X	X	X	64/32	230000H-23FFFFH	118000H-11FFFFH
	BA41	0	1	0	0	0	1	0	X	X	X	64/32	220000H-22FFFFH	110000H-117FFFH
	BA40	0	1	0	0	0	0	1	X	X	X	64/32	210000H-21FFFFH	108000H-10FFFFH
	BA39	0	1	0	0	0	0	0	X	X	X	64/32	200000H-20FFFFH	100000H-107FFFH
Bank1	BA38	0	0	1	1	1	1	1	X	X	X	64/32	1F0000H-1FFFFFH	0F8000H-0FFFFFH
	BA37	0	0	1	1	1	1	0	X	X	X	64/32	1E0000H-1EFFFFH	0F0000H-0F7FFFH
	BA36	0	0	1	1	1	0	1	X	X	X	64/32	1D0000H-1DFFFFH	0E8000H-0EFFFFH
	BA35	0	0	1	1	1	0	0	X	X	X	64/32	1C0000H-1CFFFFH	0E0000H-0E7FFFH

Table 3. NOR Flash Memory Bottom Block Address (KBB05A500)

KBB05A500	Block	Block Address										Block Size (KB/KW)	Address Range	
		A21	A20	A19	A18	A17	A16	A15	A14	A13	A12		Byte Mode	Word Mode
Bank1	BA34	0	0	1	1	0	1	1	X	X	X	64/32	1B0000H-1BFFFFH	0D8000H-0DFFFFH
	BA33	0	0	1	1	0	1	0	X	X	X	64/32	1A0000H-1AFFFFH	0D0000H-0D7FFFH
	BA32	0	0	1	1	0	0	1	X	X	X	64/32	190000H-19FFFFH	0C8000H-0CFFFFH
	BA31	0	0	1	1	0	0	0	X	X	X	64/32	180000H-18FFFFH	0C0000H-0C7FFFH
	BA30	0	0	1	0	1	1	1	X	X	X	64/32	170000H-17FFFFH	0B8000H-0BFFFFH
	BA29	0	0	1	0	1	1	0	X	X	X	64/32	160000H-16FFFFH	0B0000H-0B7FFFH
	BA28	0	0	1	0	1	0	1	X	X	X	64/32	150000H-15FFFFH	0A8000H-0AFFFFH
	BA27	0	0	1	0	1	0	0	X	X	X	64/32	140000H-14FFFFH	0A0000H-0A7FFFH
	BA26	0	0	1	0	0	1	1	X	X	X	64/32	130000H-13FFFFH	098000H-09FFFFH
	BA25	0	0	1	0	0	1	0	X	X	X	64/32	120000H-12FFFFH	090000H-097FFFH
	BA24	0	0	1	0	0	0	1	X	X	X	64/32	110000H-11FFFFH	088000H-08FFFFH
	BA23	0	0	1	0	0	0	0	X	X	X	64/32	100000H-10FFFFH	080000H-087FFFH
	BA22	0	0	0	1	1	1	1	X	X	X	64/32	0F0000H-0FFFFFH	078000H-07FFFFH
	BA21	0	0	0	1	1	1	0	X	X	X	64/32	0E0000H-0EFFFFH	070000H-077FFFH
	BA20	0	0	0	1	1	0	1	X	X	X	64/32	0D0000H-0DFFFFH	068000H-06FFFFH
	BA19	0	0	0	1	1	0	0	X	X	X	64/32	0C0000H-0CFFFFH	060000H-067FFFH
	BA18	0	0	0	1	0	1	1	X	X	X	64/32	0B0000H-0BFFFFH	058000H-05FFFFH
	BA17	0	0	0	1	0	1	0	X	X	X	64/32	0A0000H-0AFFFFH	050000H-057FFFH
	BA16	0	0	0	1	0	0	1	X	X	X	64/32	090000H-09FFFFH	048000H-04FFFFH
	BA15	0	0	0	1	0	0	0	X	X	X	64/32	080000H-08FFFFH	040000H-047FFFH
	BA14	0	0	0	0	1	1	1	X	X	X	64/32	070000H-07FFFFH	038000H-03FFFFH
	BA13	0	0	0	0	1	1	0	X	X	X	64/32	060000H-06FFFFH	030000H-037FFFH
	BA12	0	0	0	0	1	0	1	X	X	X	64/32	050000H-05FFFFH	028000H-02FFFFH
	BA11	0	0	0	0	1	0	0	X	X	X	64/32	040000H-04FFFFH	020000H-027FFFH
	BA10	0	0	0	0	0	1	1	X	X	X	64/32	030000H-03FFFFH	018000H-01FFFFH
	BA9	0	0	0	0	0	1	0	X	X	X	64/32	020000H-02FFFFH	010000H-017FFFH
	BA8	0	0	0	0	0	0	1	X	X	X	64/32	010000H-01FFFFH	008000H-00FFFFH
	BA7	0	0	0	0	0	0	0	1	1	1	8/4	00E000H-00FFFFH	007000H-007FFFH
	BA6	0	0	0	0	0	0	0	1	1	0	8/4	00C000H-00DFFFH	006000H-006FFFH
	BA5	0	0	0	0	0	0	0	1	0	1	8/4	00A000H-00BFFFH	005000H-005FFFH
	BA4	0	0	0	0	0	0	0	1	0	0	8/4	008000H-009FFFH	004000H-004FFFH
	BA3	0	0	0	0	0	0	0	0	1	1	8/4	006000H-007FFFH	003000H-003FFFH
	BA2	0	0	0	0	0	0	0	0	1	0	8/4	004000H-005FFFH	002000H-002FFFH
	BA1	0	0	0	0	0	0	0	0	0	1	8/4	002000H-003FFFH	001000H-001FFFH
	BA0	0	0	0	0	0	0	0	0	0	0	8/4	000000H-001FFFH	000000H-000FFFH

NOTE: The bank address bits are A21 ~ A20 for KBB05A500.

Table 4. Secode Block Addresses for Bottom Boot Devices

Device	Block Address A21-A12	Block Size	(X8) Address Range	(X16) Address Range
KBB05A500	0000000xxx	64/32	000000H-00FFFFH	000000H-007FFFH

NOR FLASH MEMORY COMMAND DEFINITIONS

The NOR Flash Memory operates by selecting and executing its operational modes. Each operational mode has its own command set. In order to select a certain mode, a proper command with specific address and data sequences must be written into the command register. Writing incorrect information which include address and data or writing an improper command will reset the device to the read mode. The defined valid register command sequences are stated in Table 5. Note that Erase Suspend (B0H) and Erase Resume (30H) commands are valid only while the Block Erase Operation is in progress.

Table 5. Command Sequences

Command Sequence		Cycle	1st Cycle		2nd Cycle		3rd Cycle		4th Cycle		5th Cycle		6th Cycle	
			Word	Byte	Word	Byte	Word	Byte	Word	Byte	Word	Byte	Word	Byte
Read	Addr	1	RA											
	Data		RD											
Reset	Addr	1	XXXH											
	Data		F0H											
Autoselect Manufacturer ID (2,3)	Addr	4	555H	AAAH	2AAH	555H	DA/ 555H	DA/ AAAH	DA/ X00H	DA/ X00H				
	Data		AAH		55H		90H		ECH					
Autoselect Device Code (2,3)	Addr	4	555H	AAAH	2AAH	555H	DA/ 555H	DA/ AAAH	DA/ X01H	DA/ X02H				
	Data		AAH		55H		90H		(See Table 9)					
Autoselect Block Group Protect Verify (2,3)	Addr	4	555H	AAAH	2AAH	555H	DA/ 555H	DA/ AAAH	BA / X02H	BA/ X04H				
	Data		AAH		55H		90H		(See Table 9)					
Auto Select Secode Block Factory Protect Verify (2,3)	Addr	4	555H	AAAH	2AAH	555H	DA/ 555H	DA/ AAAH	DA / X03H	DA/ X06H				
	Data		AAH		55H		90H		(See Table 9)					
Enter Secode Block Region	Addr	3	555H	AAAH	2AAH	555H	555H	AAAH						
	Data		AAH		55H		88H							
Exit Secode Block Region	Addr	4	555H	AAAH	2AAH	555H	555H	AAAH	XXXH					
	Data		AAH		55H		90H		00H					
Program	Addr	4	555H	AAAH	2AAH	555H	555H	AAAH	PA					
	Data		AAH		55H		A0H		PD					
Unlock Bypass	Addr	3	555H	AAAH	2AAH	555H	555H	AAAH						
	Data		AAH		55H		20H							
Unlock Bypass Program	Addr	2	XXXH		PA									
	Data		A0H		PD									
Unlock Bypass Reset	Addr	2	XXXH		XXXH									
	Data		90H		00H									
Chip Erase	Addr	6	555H	AAAH	2AAH	555H	555H	AAAH	555H	AAAH	2AAH	555H	555H	AAAH
	Data		AAH		55H		80H		AAH		55H		10H	
Block Erase	Addr	6	555H	AAAH	2AAH	555H	555H	AAAH	555H	AAAH	2AAH	555H	BA	
	Data		AAH		55H		80H		AAH		55H		30H	
Block Erase Suspend (4, 5)	Addr	1	XXXH											
	Data		B0H											
Block Erase Resume	Addr	1	XXXH											
	Data		30H											
CFI Query (6)	Addr	1	55H	AAH										
	Data		98H											

NOTES: 1. RA : Read Address, PA : Program Address, RD : Read Data, PD : Program Data
DA : Dual Bank Address (A20 - A21), BA : Block Address (A12 - A21), X = Don't care .
2. To terminate the Autoselect Mode, it is necessary to write Reset command to the register.
3. The 4th cycle data of Autoselect mode is output data.
The 3rd and 4th cycle bank addresses of Autoselect mode must be same.
4. The Read / Program operations at non-erasing blocks and the autoselect mode are allowed in the Erase Suspend mode.
5. The Erase Suspend command is applicable only to the Block Erase operation.
6. Command is valid when the device is in read mode or Autoselect mode.
7. DQ8 - DQ15 are don't care in command sequence, but RD and PD is excluded.
8. A11 - A21 are also don't care, except for the case of special notice.

Table 6. NOR Flash Memory Autoselect Codes

Description	DQ8 to DQ15		DQ7 to DQ0
	$\overline{BYTE} = V_{IH}$	$\overline{BYTE} = V_{IL}$	
Manufacturer ID	X	X	ECH
Device Code KBB06A500 (Top Boot Block)	22H	X	E0H
Device Code KBB05A500 (Bottom Boot Block)	22H	X	E2H
Block Protection Verification	X	X	01H (Protected), 00H (Unprotected)
Secode Block Indicator Bit (DQ7)	X	X	80H (Factory locked), 00H (Not factory locked)

NOTES: 1. L=Logic Low=V_{IL}, H=Logic High=V_{IH}, DA=Dual Bank Address, BA=Block Address, X=Don't care.

2. Secode Block : Security Code Block.

NAND FLASH PRODUCT INTRODUCTION

The NAND Flash Memory is a 132Mbit(138,412,032 bit) memory organized as 32,768 rows(pages) by 264 columns. Spare 8 columns are located in 256 to 263 column address. A 264-word data register is connected to memory cell arrays accommodating data transfer between the I/O buffers and memory during page read and page program operations. The memory array is made up of 16 cells that are serially connected like NAND structure. Each of the 16 cells resides in a different page. A block consists of the 32 pages formed by one NAND structures, totaling 8,448 NAND structures of 16 cells. The array organization is shown in Figure 2. Program and read operations are executed on a page basis, while erase operation is executed on a block basis. The memory array consists of 1024 blocks, and a block is separately erasable by 8K-word unit. It indicates that the bit by bit erase operation is prohibited on the NAND Flash Memory.

The NAND Flash Memory has addresses multiplexed with lower 8 I/O′s. The NAND Flash Memory allows sixteen bit wide data transfer into and out of page registers. This scheme dramatically reduces pin counts and allows systems upgrades to future densities by maintaining consistency in system board design. Command, address and data are all written through I/O′s by bringing $\overline{WE}$ to low while $\overline{CE}$ is low. Data is latched on the rising edge of $\overline{WE}$. Command Latch Enable(CLE) and Address Latch Enable(ALE) are used to multiplex command and address respectively, via the I/O pins. All commands require one bus cycle except Page Program command and Block Erase command which require two cycles: one cycle for setup and another for execution. The 8M word physical space requires 24 addresses, thereby requiring three cycles for byte-level addressing: column address, low row address and high row address, in that order. Page Read and Page Program need the same three address cycles following required command input. In Block Erase operation, however, only two row address cycles are used. Device operations are selected by writing specific commands into command register. Table 7 defines the specific commands of the NAND Flash Memory.

Table 7. Command Sets

Function	1st. Cycle	2nd. Cycle	Acceptable Command during Busy
Read 1	00h	-	
Read 2	50h	-	
Read ID	90h	-	
Reset	FFh	-	O
Page Program	80h	10h	
Block Erase	60h	D0h	
Read Status	70h	-	O

Table 8. NOR Flash Operations Table

Operation		$\overline{CE}_R$	$\overline{OE}$	$\overline{WE}$	$\overline{BYTE}$	$\overline{WP}$/ ACC	A9	A6	A1	A0	DQ15/ A-1	DQ8/ DQ14	DQ0/ DQ7	$\overline{RESET}$
Read	word	L	L	H	H	L/H	A9	A6	A1	A0	DQ15	D_{OUT}	D_{OUT}	H
	byte	L	L	H	L		A9	A6	A1	A0	A-1	High-Z	D_{OUT}	H
Stand-by		$Vcc_R \pm 0.3V$	X	X	X	(2)	X	X	X	X	High-Z	High-Z	High-Z	(2)
Output Disable		L	H	H	X	L/H	X	X	X	X	High-Z	High-Z	High-Z	H
Reset		X	X	X	X	L/H	X	X	X	X	High-Z	High-Z	High-Z	L
Write	word	L	H	L	H	(4)	A9	A6	A1	A0	D_{IN}	D_{IN}	D_{IN}	H
	byte	L	H	L	L		A9	A6	A1	A0	A-1	High-Z	D_{IN}	H
Enable Block Group Protect (3)		L	H	L	X	L/H	X	L	H	L	X	X	D_{IN}	V_{ID}
Enable Block Group Unprotect (3)		L	H	L	X	(4)	X	H	H	L	X	X	D_{IN}	V_{ID}
Temporary Block Group		X	X	X	X	(4)	X	X	X	X	X	X	X	V_{ID}

NOTES:
1. L = V_{IL} (Low), H = V_{IH} (High), V_{ID} = 8.5V~12.5V, D_{IN} = Data in, D_{OUT} = Data out, X = Don't care.
2. $\overline{WP}$/ACC and $\overline{RESET}$ pin are asserted at $Vcc_R \pm 0.3$ V or $Vss \pm 0.3$ V in the Stand-by mode.
3. Addresses must be composed of the Block address (A12 - A21).
   The Block Protect and Unprotect operations may be implemented via programming equipment too.
   Refer to the "Block Group Protection and Unprotection".
4. If $\overline{WP}$/ACC=V_{IL}, the two outermost boot blocks is protected. If $\overline{WP}$/ACC=V_{IH}, the two outermost boot block protection depends on whether those blocks were last protected or unprotected using the method described in "Block Group Protection and Unprotection". If $\overline{WP}$/ACC=V_{HH}, all blocks will be temporarily unprotected.

Table 9. NAND Flash Operations Table

CLE	ALE	$\overline{CE}_R$	$\overline{WE}$	$\overline{RE}$	$\overline{WP}$	Mode	
H	L	L	↑	H	X	Read Mode	Command Input
L	H	L	↑	H	X		Address Input(3clock)
H	L	L	↑	H	H	Write Mode	Command Input
L	H	L	↑	H	H		Address Input(3clock)
L	L	L	↑	H	H	Data Input	
L	L	L	H	↓	X	Data Output	
X	X	X	X	H	X	During Read(Busy)	
X	X	X	X	X	H	During Program(Busy)	
X	X	X	X	X	H	During Erase(Busy)	
X	X(1)	X	X	X	L	Write Protect	
X	X	H	X	X	0V/Vcc_F(2)	Stand-by	

NOTE: 1. X can be V_{IL} or V_{IH}.
2. $\overline{WP}$ should be biased to CMOS high or CMOS low for standby.

Table 10. U*t*RAM Operations Table

$\overline{CS}$u	$\overline{ZZ}$	$\overline{OE}$	$\overline{WE}$	$\overline{LB}$	$\overline{UB}$	I/O0~7	I/O8~15	Mode	Power
H	H	X1)	X1)	X1)	X1)	High-Z	High-Z	Deselected	Standby
X1)	L	X1)	X1)	X1)	X1)	High-Z	High-Z	Deselected	Deep Power Down
L	H	X1)	X1)	H	H	High-Z	High-Z	Deselected	Standby
L	H	H	H	L	X1)	High-Z	High-Z	Output Disabled	Active
L	H	H	H	X1)	L	High-Z	High-Z	Output Disabled	Active
L	H	L	H	L	H	Dout	High-Z	Lower Byte Read	Active
L	H	L	H	H	L	High-Z	Dout	Upper Byte Read	Active
L	H	L	H	L	L	Dout	Dout	Word Read	Active
L	H	X1)	L	L	H	Din	High-Z	Lower Byte Write	Active
L	H	X1)	L	H	L	High-Z	Din	Upper Byte Write	Active
L	H	X1)	L	L	L	Din	Din	Word Write	Active

1. X = V_{IL} or V_{IH}

NOR FLASH DEVICE OPERATION

Byte/Word Mode

If the $\overline{BYTE}$ pin is set at logical "1" , the device is in word mode, DQ0-DQ15 are active. Otherwise the $\overline{BYTE}$ pin is set at logical "0" , the device is in byte mode, DQ0-DQ7 are active. DQ8-DQ14 are in the High-Z state and DQ15 pin is used as an input for the LSB (A-1) address pin.

Read Mode

The NOR Flash memory is controlled by Chip Enable ($\overline{CE_R}$), Output Enable ($\overline{OE}$) and Write Enable ($\overline{WE}$). When $\overline{CE_R}$ and $\overline{OE}$ are low and $\overline{WE}$ is high, the data stored at the specified address location,will be the output of the device. The outputs are in high impedance state whenever $\overline{CE_R}$ or $\overline{OE}$ is high.

Standby Mode

The NOR Flash memory features Stand-by Mode to reduce power consumption. This mode puts the device on hold when the device is deselected by making $\overline{CE_R}$ high ($\overline{CE_R} = V_{IH}$). Refer to the DC characteristics for more details on stand-by modes.

Output Disable

The device outputs are disabled when $\overline{OE}$ is High ($\overline{OE} = V_{IH}$). The output pins are in high impedance state.

Automatic Sleep Mode

The NOR Flash Memory features Automatic Sleep Mode to minimize the device power consumption. Since the device typically draws 5μA of the current in Automatic Sleep Mode, this feature plays an extremely important role in battery-powered applications. When addresses remain steady for t_{AA}+50ns, the device automatically activates the Automatic Sleep Mode. In the sleep mode, output data is latched and always available to the system. When addresses are changed, the device provides new data without wait time.

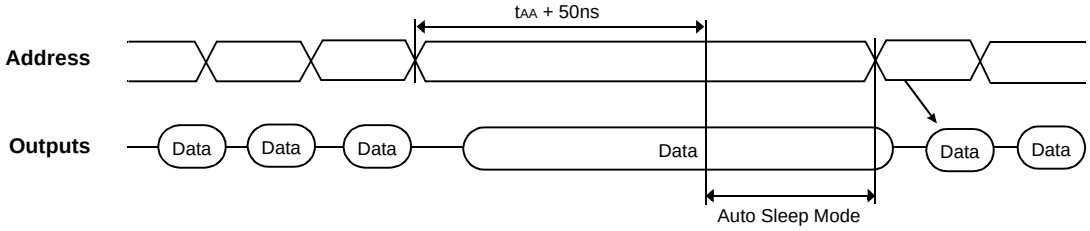
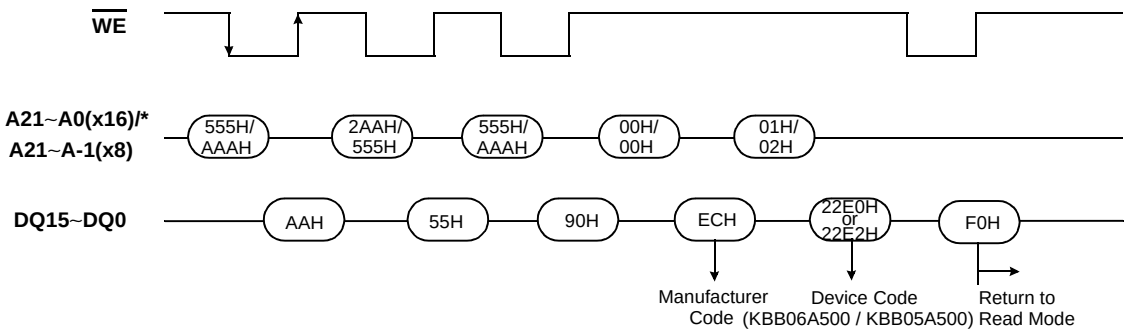


Figure 3. Auto Sleep Mode Operation

Autoselect Mode

The NOR Flash memory offers the Autoselect Mode to identify manufacturer and device type by reading a binary code. The Autoselect Mode allows programming equipment to automatically match the device to be programmed with its corresponding programming algorithm. In addition, this mode allows the verification of the status of write protected blocks. The manufacturer and device code can be read via the command register. The Command Sequence is shown in Table 5 and Figure 4. The autoselect operation of block protect verification is initiated by first writing two unlock cycle. The third cycle must contain the bank address and autoselect command (90H). If Block address while (A6, A1, A0) = (0,1,0) is finally asserted on the address ball, it will produce a logical "1" at the device output DQ0 to indicate a write protected block or a logical "0" at the device output DQ0 to indicate a write unprotected block. To terminate the autoselect operation, write Reset command (F0H) into the command register.



NOTE: The 3rd Cycle and 4th Cycle address must include the same bank address. Please refer to Table 6 for device code.

Figure 4. Autoselect Operation

Write (Program/Erase) Mode

The NOR Flash memory executes its program/erase operations by writing commands into the command register. In order to write the commands to the register, $\overline{CE}_R$ and $\overline{WE}$ must be low and $\overline{OE}$ must be high. Addresses are latched on the falling edge of $\overline{CE}_R$ or $\overline{WE}$ (whichever occurs last) and the data are latched on the rising edge of $\overline{CE}_R$ or $\overline{WE}$ (whichever occurs first). The device uses standard microprocessor write timing.

Program

The NOR Flash memory can be programmed in units of a word or a byte. Programming is writing 0's into the memory array by executing the Internal Program Routine. In order to perform the Internal Program Routine, a four-cycle command sequence is necessary. The first two cycles are unlock cycles. The third cycle is assigned for the program setup command. In the last cycle, the address of the memory location and the data to be programmed at that location are written. The device automatically generates adequate program pulses and verifies the programmed cell margin by the Internal Program Routine. During the execution of the Routine, the system is not required to provide further controls or timings.
During the Internal Program Routine, commands written to the device will be ignored. Note that a hardware reset during a program operation will cause data corruption at the corresponding location.

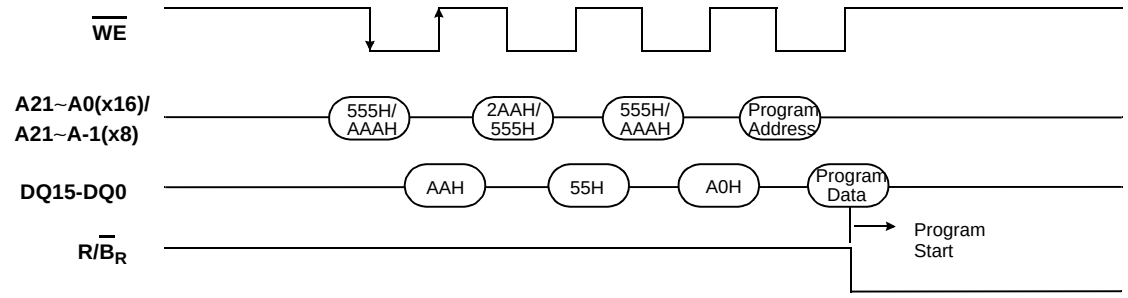


Figure 5. Program Command Sequence

Unlock Bypass

The NOR Flash memory provides the unlock bypass mode to save its program time. The mode is invoked by the unlock bypass command sequence. Unlike the standard program command sequence that contains four bus cycles, the unlock bypass program command sequence comprises only two bus cycles.
The unlock bypass mode is engaged by issuing the unlock bypass command sequence which is comprised of three bus cycles. Writing first two unlock cycles is followed by a third cycle containing the unlock bypass command (20H). Once the device is in the unlock bypass mode, the unlock bypass program command sequence is necessary to program in this mode. The unlock bypass program command sequence is comprised of only two bus cycles; writing the unlock bypass program command (A0H) is followed by the program address and data. This command sequence is the only valid one for programming the device in the unlock bypass mode.
The unlock bypass reset command sequence is the only valid command sequence to exit the unlock bypass mode. The unlock bypass reset command sequence consists of two bus cycles. The first cycle must contain the data (90H). The second cycle contains only the data (00H). Then, the device returns to the read mode.

Chip Erase

To erase a chip is to write 1′s into the entire memory array by executing the Internal Erase Routine. The Chip Erase requires six bus cycles to write the command sequence. The erase set-up command is written after first two "unlock" cycles. Then, there are two more write cycles prior to writing the chip erase command. The Internal Erase Routine automatically pre-programs and verifies the entire memory for an all zero data pattern prior to erasing. The automatic erase begins on the rising edge of the last $\overline{WE}$ or $\overline{CE}_R$ pulse in the command sequence and terminates when DQ7 is "1". After that the device returns to the read mode.

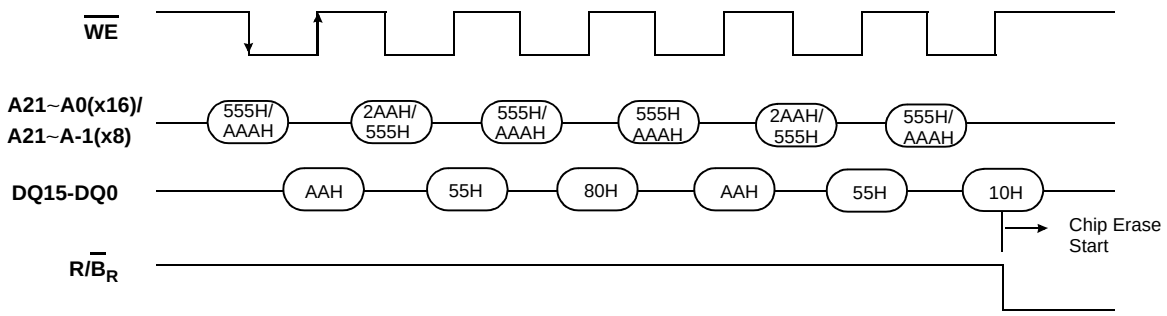


Figure 6. Chip Erase Command Sequence

Block Erase

To erase a block is to write 1′s into the desired memory block by executing the Internal Erase Routine. The Block Erase requires six bus cycles to write the command sequence shown in Table 5. After the first two "unlock" cycles, the erase setup command (80H) is written at the third cycle. Then there are two more "unlock" cycles followed by the Block Erase command. The Internal Erase Routine automatically pre-programs and verifies the entire memory prior to erasing it. The block address is latched on the falling edge of $\overline{WE}$ or $\overline{CE}_R$, while the Block Erase command is latched on the rising edge of $\overline{WE}$ or $\overline{CE}_R$.
Multiple blocks can be erased sequentially by writing the six bus-cycle operation in Fig 7. Upon completion of the last cycle for the Block Erase, additional block address and the Block Erase command (30H) can be written to perform the Multi-Block Erase. An 50us (typical) "time window" is required between the Block Erase command writes. The Block Erase command must be written within the 50us "time window", otherwise the Block Erase command will be ignored. The 50us "time window" is reset when the falling edge of the $\overline{WE}$ occurs within the 50us of "time window" to latch the Block Erase command. During the 50us of "time window", any command other than the Block Erase or the Erase Suspend command written to the device will reset the device to read mode. After the 50 us of "time window", the Block Erase command will initiate the Internal Erase Routine to erase the selected blocks. Any Block Erase address and command following the exceeded "time window" may or may not be accepted. No other commands will be recognized except the Erase Suspend command.

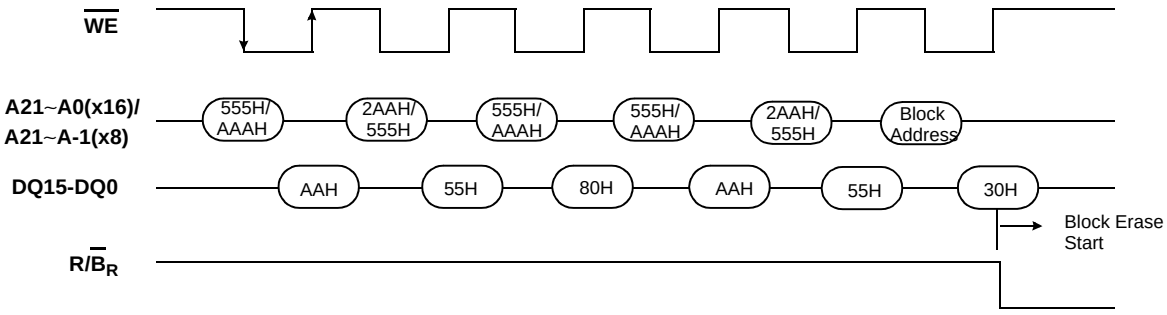


Figure 7. Block Erase Command Sequence

Erase Suspend / Resume

The Erase Suspend command interrupts the Block Erase to read or program data in a block that is not being erased. The Erase Suspend command is only valid during the Block Erase operation including the time window of 50µs. The Erase Suspend command is not valid while the Chip Erase or the Internal Program Routine sequence is running.
When the Erase Suspend command is written during a Block Erase operation, the device requires a maximum of 20µs to suspend the erase operation. But, when the Erase Suspend command is written during the block erase time window (50µs) , the device immediately terminates the block erase time window and suspends the erase operation.
After the erase operation has been suspended, the device is availble for reading or programming data in a block that is not being erased. The system may also write the autoselect command sequence when the device is in the Erase Suspend mode.
When the Erase Resume command is executed, the Block Erase operation will resume. When the Erase Suspend or Erase Resume command is executed, the addresses are in Don't Care state.

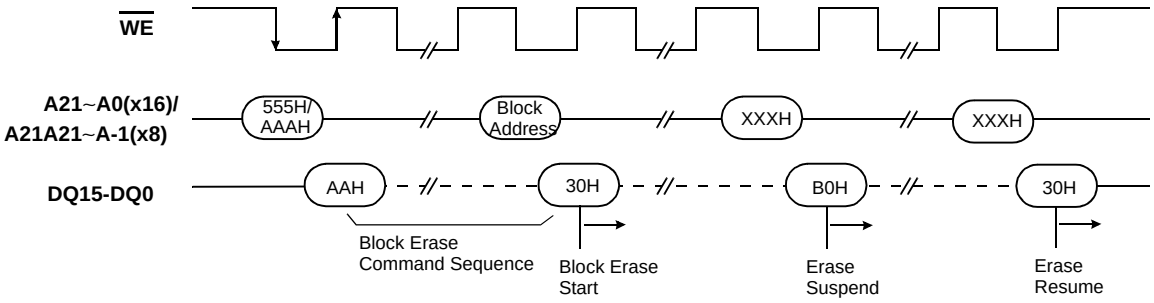


Figure 8. Erase Suspend/Resume Command Sequence

Read While Write

The NOR Flash memory provides dual bank memory architecture that divides the memory array into two banks. The device is capable of reading data from one bank and writing data to the other bank simultaneously. This is so called the Read While Write operation with dual bank architecture; this feature provides the capability of executing the read operation during Program/Erase or Erase-Suspend-Program operation.
The Read While Write operation is prohibited during the chip erase operation. It is also allowed during erase operation when either single block or multiple blocks from same bank are loaded to be erased. It means that the Read While Write operation is prohibited when blocks from Bank1 and another blocks from Bank2 are loaded all together for the multi-block erase operation.

Block Group Protection & Unprotection

The NOR Flash memory feature hardware block group protection. This feature will disable both program and erase operations in any combination of forty one block groups of memory. Please refer to Tables 12 and 13. The block group protection feature is enabled using programming equipment at the user's site. The device is shipped with all block groups unprotected.
This feature can be hardware protected or unprotected. If a block is protected, program or erase command in the protected block will be ignored by the device. The protected block can only be read. This is useful method to preserve an important program data. The block group unprotection allows the protected blocks to be erased or programed. All blocks must be protected before unprotect operation is executing. The block protection and unprotection can be implemented by the following method.

Table 11. Block Group Protection & Unprotection

Operation	$\overline{CE}_R$	$\overline{OE}$	$\overline{WE}$	$\overline{BYTE}$	A9	A6	A1	A0	DQ15/ A-1	DQ8/ DQ14	DQ0/ DQ7	$\overline{RESET}$
Block Group Protect	L	H	L	X	X	L	H	L	X	X	D_{IN}	V_{ID}
Block Group Unprotect	L	H	L	X	X	H	H	L	X	X	D_{IN}	V_{ID}

Address must be inputted to the block group address (A12~A21) during block group protection operation. Please refer to Figure 10 (Algorithm) and Switching Waveforms of Block Group Protect & Unprotect Operations.

Temporary Block Group Unprotect

The protected blocks of the NOR Flash memory can be temporarily unprotected by applying high voltage (V_{ID} = 8.5V ~ 12.5V) to the $\overline{RESET}$ ball. In this mode, previously protected blocks can be programmed or erased with the program or erase command routines. When the $\overline{RESET}$ ball goes high ($\overline{RESET}$ = V_{IH}), all the previously protected blocks will be protected again. If the $\overline{WP}$/ACC ball is asserted at V_{IL} , the two outermost boot blocks remain protected.

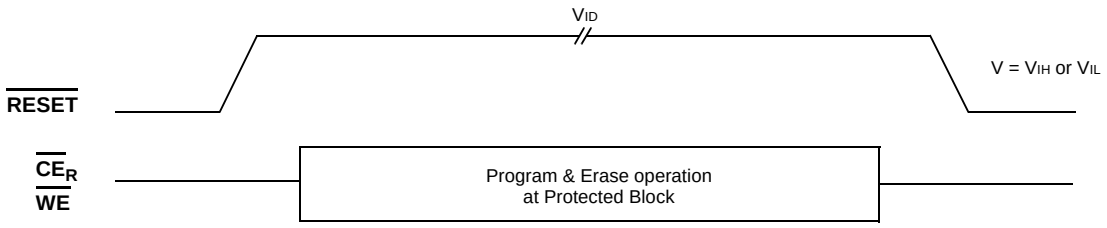
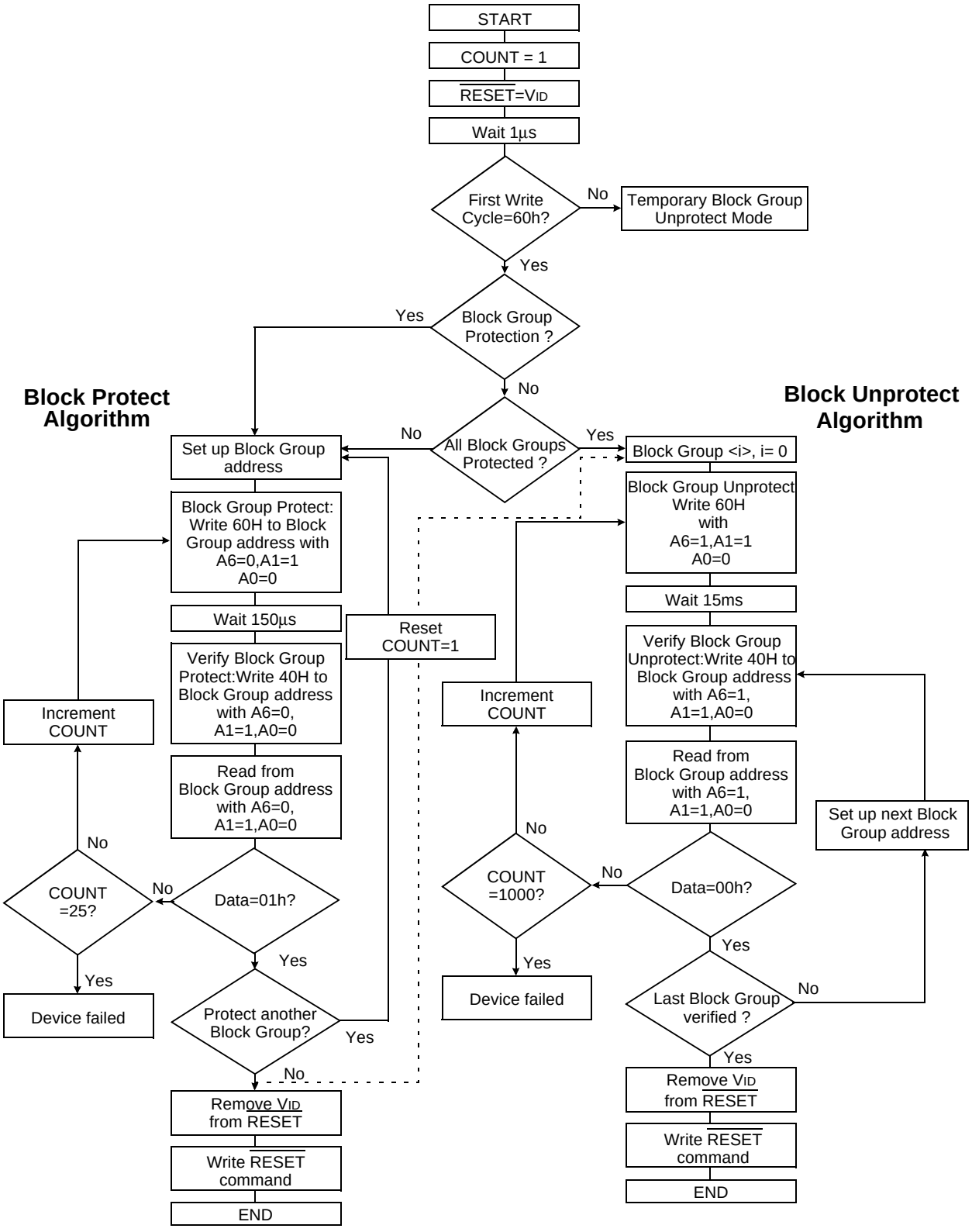


Figure 9. Temporary Block Group Unprotect Sequence



NOTE: All blocks must be protected before unprotect operation is executing.

Figure 10. Block Group Protection & Unprotection Algorithms

Table 12. NOR Flash Memory Block Group Address (Top Boot Block)

Block Group	Block Address										Block
	A21	A20	A19	A18	A17	A16	A15	A14	A13	A12	
BGA0	0	0	0	0	0	0	0	X	X	X	BA0
BGA1	0	0	0	0	0	0	1	X	X	X	BA1 to BA3
						1	0				
						1	1				
BGA2	0	0	0	0	1	X	X	X	X	X	BA4 to BA7
BGA3	0	0	0	1	0	X	X	X	X	X	BA8 to BA11
BGA4	0	0	0	1	1	X	X	X	X	X	BA12 to BA15
BGA5	0	0	1	0	0	X	X	X	X	X	BA16 to BA19
BGA6	0	0	1	0	1	X	X	X	X	X	BA20 to BA23
BGA7	0	0	1	1	0	X	X	X	X	X	BA24 to BA27
BGA8	0	0	1	1	1	X	X	X	X	X	BA28 to BA31
BGA9	0	1	0	0	0	X	X	X	X	X	BA32 to BA35
BGA10	0	1	0	0	1	X	X	X	X	X	BA36 to BA39
BGA11	0	1	0	1	0	X	X	X	X	X	BA40 to BA43
BGA12	0	1	0	1	1	X	X	X	X	X	BA44 to BA47
BGA13	0	1	1	0	0	X	X	X	X	X	BA48 to BA51
BGA14	0	1	1	0	1	X	X	X	X	X	BA52 to BA55
BGA15	0	1	1	1	0	X	X	X	X	X	BA56 to BA59
BGA16	0	1	1	1	1	X	X	X	X	X	BA60 to BA63
BGA17	1	0	0	0	0	X	X	X	X	X	BA64 to BA67
BGA18	1	0	0	0	1	X	X	X	X	X	BA68 to BA71
BGA19	1	0	0	1	0	X	X	X	X	X	BA72 to BA75
BGA20	1	0	0	1	1	X	X	X	X	X	BA76 to BA79
BGA21	1	0	1	0	0	X	X	X	X	X	BA80 to BA83
BGA22	1	0	1	0	1	X	X	X	X	X	BA84 to BA87
BGA23	1	0	1	1	0	X	X	X	X	X	BA88 to BA91
BGA24	1	0	1	1	1	X	X	X	X	X	BA92 to BA95
BGA25	1	1	0	0	0	X	X	X	X	X	BA96 to BA99
BGA26	1	1	0	0	1	X	X	X	X	X	BA100 to BA103
BGA27	1	1	0	1	0	X	X	X	X	X	BA104 to BA107
BGA28	1	1	0	1	1	X	X	X	X	X	BA108 to BA111
BGA29	1	1	1	0	0	X	X	X	X	X	BA112 to BA115
BGA30	1	1	1	0	1	X	X	X	X	X	BA116 to BA119
BGA31	1	1	1	1	0	X	X	X	X	X	BA120 to BA123
BGA32	1	1	1	1	1	0	0	X	X	X	BA124 to BA126
						0	1				
						1	0				
BGA33	1	1	1	1	1	1	1	0	0	0	BA127
BGA34	1	1	1	1	1	1	1	0	0	1	BA128
BGA35	1	1	1	1	1	1	1	0	1	0	BA129
BGA36	1	1	1	1	1	1	1	0	1	1	BA130
BGA37	1	1	1	1	1	1	1	1	0	0	BA131
BGA38	1	1	1	1	1	1	1	1	0	1	BA132
BGA39	1	1	1	1	1	1	1	1	1	0	BA133
BGA40	1	1	1	1	1	1	1	1	1	1	BA134

Table 13. NOR Flash Memory Block Group Address (Bottom Boot Block)

Block Group	Block Address										Block
	A21	A20	A19	A18	A17	A16	A15	A14	A13	A12	
BGA0	0	0	0	0	0	0	0	0	0	0	BA0
BGA1	0	0	0	0	0	0	0	0	0	1	BA1
BGA2	0	0	0	0	0	0	0	0	1	0	BA2
BGA3	0	0	0	0	0	0	0	0	1	1	BA3
BGA4	0	0	0	0	0	0	0	1	0	0	BA4
BGA5	0	0	0	0	0	0	0	1	0	1	BA5
BGA6	0	0	0	0	0	0	0	1	1	0	BA6
BGA7	0	0	0	0	0	0	0	1	1	1	BA7
BGA8	0	0	0	0	0	0	1	X	X	X	BA8 to BA10
						1	0				
						1	1				
BGA9	0	0	0	0	1	X	X	X	X	X	BA11 to BA14
BGA10	0	0	0	1	0	X	X	X	X	X	BA15 to BA18
BGA11	0	0	0	1	1	X	X	X	X	X	BA19 to BA22
BGA12	0	0	1	0	0	X	X	X	X	X	BA23 to BA26
BGA13	0	0	1	0	1	X	X	X	X	X	BA27 to BA30
BGA14	0	0	1	1	0	X	X	X	X	X	BA31 to BA34
BGA15	0	0	1	1	1	X	X	X	X	X	BA35 to BA38
BGA16	0	1	0	0	0	X	X	X	X	X	BA39 to BA42
BGA17	0	1	0	0	1	X	X	X	X	X	BA43 to BA46
BGA18	0	1	0	1	0	X	X	X	X	X	BA47 to BA50
BGA19	0	1	0	1	1	X	X	X	X	X	BA51 to BA54
BGA20	0	1	1	0	0	X	X	X	X	X	BA55 to BA58
BGA21	0	1	1	0	1	X	X	X	X	X	BA59 to BA62
BGA22	0	1	1	1	0	X	X	X	X	X	BA63 to BA66
BGA23	0	1	1	1	1	X	X	X	X	X	BA67 to BA70
BGA24	1	0	0	0	0	X	X	X	X	X	BA71 to BA74
BGA25	1	0	0	0	1	X	X	X	X	X	BA75 to BA78
BGA26	1	0	0	1	0	X	X	X	X	X	BA79 to BA82
BGA27	1	0	0	1	1	X	X	X	X	X	BA83 to BA86
BGA28	1	0	1	0	0	X	X	X	X	X	BA87to BA90
BGA29	1	0	1	0	1	X	X	X	X	X	BA91 to BA94
BGA30	1	0	1	1	0	X	X	X	X	X	BA95 to BA98
BGA31	1	0	1	1	1	X	X	X	X	X	BA99 to BA102
BGA32	1	1	0	0	0	X	X	X	X	X	BA103 to BA106
BGA33	1	1	0	0	1	X	X	X	X	X	BA107 to BA110
BGA34	1	1	0	1	0	X	X	X	X	X	BA111 to BA114
BGA35	1	1	0	1	1	X	X	X	X	X	BA115 to BA118
BGA36	1	1	1	0	0	X	X	X	X	X	BA119 to BA122
BGA37	1	1	1	0	1	X	X	X	X	X	BA123 to BA126
BGA38	1	1	1	1	0	X	X	X	X	X	BA127 to BA130
BGA39	1	1	1	1	1	0	0	X	X	X	BA131 to BA133
						0	1				
						1	0				
BGA40	1	1	1	1	1	1	1	X	X	X	BA134

Write Protect ($\overline{WP}$)

The $\overline{WP}$/ACC ball has two useful functions. The one is that certain boot block is protected by the hardware method not to use V_{ID}. The other is that program operation is accelerated to reduce the program time (Refer to Accelerated program Operation Paragraph).
When the $\overline{WP}$/ACC ball is asserted at V_{IL}, the device can not perform program and erase operation in the two "outermost" 8K byte boot blocks independently of whether those blocks were protected or unprotected using the method described in "Block Group protection/Unprotection".
The write protected blocks can only be read. This is useful method to preserve an important program data.
The two outermost 8K byte boot blocks are the two blocks containing the lowest addresses in a bottom-boot-configured device, or the two blocks containing the highest addresses in a top-boot-congfigured device.
(KBB06A500 : BA133 and BA134, KBB05A500 : BA0 and BA1)
When the $\overline{WP}$/ACC ball is asserted at V_{IH}, the device reverts to whether the two outermost 8K byte boot blocks were last set to be protected or unprotected. That is, block protection or unprotection for these two blocks depends on whether they were last protected or unprotected using the method described in "Block Group protection/unprotection".
Recommend that the $\overline{WP}$/ACC ball must not be in the state of floating or unconnected, otherwise the device may be led to malfunction.

Secode(Security Code) Block Region

The Secode Block feature provides a NOR Flash memory region to be stored unique and permanent identification code, that is, Electronic Serial Number (ESN), customer code and so on. This is primarily intended for customers who wish to use an Electronic Serial Number (ESN) in the device with the ESN protected against modification. Once the Secode Block region is protected, any further modification of that region is impossible. This ensures the security of the ESN once the product is shipped to the field.
The Secode Block is factory locked or customer lockable. Before the device is shipped, the factory locked Secode Block is written on the special code and it is protected. The Secode Indicator bit (DQ7) is permanently fixed at "1" and it is not changed. The customer lockable Secode Block is unprotected, therefore it is programmed and erased. The Secode Indicator bit (DQ7) of it is permanently fixed at "0" and it is not changed. but once it is protected, there is no procedure to unprotect and modify the Secode Block.
The Secode Block region is 64K bytes in length and is accessed through a new command sequence (see Table 8). After the system has written the Enter Secode Block command sequence, the system may read the Secode Block region by using the same addresses of the boot blocks (8KBx8). The KBB06A500 occupies the address of the byte mode 7F0000H to 7FFFFFH (word mode 3F8000H to 3FFFFFH) and the KBB05A500 type occupies the address of the byte mode 000000H to 00FFFFH (word mode 000000H to 007FFFH). This mode of operation continues until the system issues the Exit Secode Block command sequence, or until power is removed from the device. On power-up, or following a hardware reset, the device reverts to read mode.

Accelerated Program Operation

Accelerated program operation reduces the program time through the ACC function. This is one of two functions provided by the $\overline{WP}$/ACC ball. When the $\overline{WP}$/ACC ball is asserted as V_{HH}, the device automatically enters the aforementioned Unlock Bypass mode, temporarily unprotecting any protected blocks, and reduces the program operation time. The system would use a two-cycle program command sequence as required by the Unlock Bypass mode. Removing V_{HH} from the $\overline{WP}$/ACC ball returns the device to normal operation. **Recommend that the WP/ACC ball must not be asserted at V_{HH} except on accelerated program operation, or the device may be damaged. In addition, the WP/ACC ball must not be in the state of floating or unconnected, otherwise the device may be led to malfunction.**

Software Reset

The reset command provides that the device is reseted to read mode or erase-suspend-read mode. The addresses are in Don't Care state. The reset command is vaild between the sequence cycles in an erase command sequence before erasing begins, or in a program command sequence before programming begins. This resets the bank in which was operating to read mode. if the device is be erasing or programming, the reset command is invalid until the operation is completed. Also, the reset command is valid between the sequence cycles in an autoselect command sequence. In the autoselect mode, the reset command returns the bank to read mode. If a bank entered the autoselect mode in the Erase Suspend mode, the reset command returns the bank to erase-suspend-read mode. If DQ5 is high on erase or program operation, the reset command return the bank to read mode or erase-suspend-read mode if the bank was in the Erase Suspend state.

Hardware Reset

The NOR Flash memory offers a reset feature by driving the $\overline{RESET}$ ball to V_{IL}. The $\overline{RESET}$ ball must be kept low (V_{IL}) for at least 500ns. When the $\overline{RESET}$ ball is driven low, any operation in progress will be terminated and the internal state machine will be reset to the standby mode after 20us. If a hardware reset occurs during a program operation, the data at that particular location will be lost. Once the $\overline{RESET}$ ball is taken high, the device requires 200ns of wake-up time until outputs are valid for read access. Also, note that all the data output balls are tri-stated for the duration of the $\overline{RESET}$ pulse.
The $\overline{RESET}$ ball may be tied to the system reset ball. If a system reset occurs during the Internal Program and Erase Routine, the device will be automatically reset to the read mode ; this will enable the systems microprocessor to read the boot-up firmware from the NOR Flash memory.

Power-up Protection

To avoid initiation of a write cycle during Vcc_R Power-up, $\overline{RESET}$ low must be asserted during power-up. After $\overline{RESET}$ goes high, the device is reset to the read mode.

Low Vcc_R Write Inhibit

To avoid initiation of a write cycle during Vcc_R power-up and power-down, a write cycle is locked out for Vcc_R less than 1.8V. If Vcc_R < V_{LKO} (Lock-Out Voltage), the command register and all internal program/erase circuits are disabled. Under this condition the device will reset itself to the read mode. Subsequent writes will be ignored until the Vcc_R level is greater than V_{LKO}. It is the user′s responsibility to ensure that the control balls are logically correct to prevent unintentional writes when Vcc_R is above 1.8V.

Write Pulse Glitch Protection

Noise pulses of less than 5ns(typical) on $\overline{CE}_R$, $\overline{OE}$, or $\overline{WE}$ will not initiate a write cycle.

Logical Inhibit

Writing is inhibited under any one of the following conditions : $\overline{OE}$ = V_{IL}, $\overline{CE}_R$ = V_{IH} or $\overline{WE}$ = V_{IH}. To initiate a write, $\overline{CE}_R$ and $\overline{WE}$ must be "0", while $\overline{OE}$ is "1".

Commom NOR Flash Memory Interface

Common Flash Momory Interface is contrived to increase the compatibility of host system software. It provides the specific information of the device, such as memory size, byte/word configuration, and electrical features. Once this information has been obtained, the system software will know which command sets to use to enable flash writes, block erases, and control the flash component.
When the system writes the CFI command(98H) to address 55H in word mode(or address AAH in byte mode), the device enters the CFI mode. And then if the system writes the address shown in Table 14, the system can read the CFI data. Query data are always presented on the lowest-order data outputs(DQ0-7) only. In word(x16) mode, the upper data outputs(DQ8-15) is 00h. To terminate this operation, the system must write the reset command.

Table 14. Common NOR Flash Memory Interface Code

Description	Addresses (Word Mode)	Addresses (Byte Mode)	Data
Query Unique ASCII string "QRY"	10H 11H 12H	20H 22H 24H	0051H 0052H 0059H
Primary OEM Command Set	13H 14H	26H 28H	0002H 0000H
Address for Primary Extended Table	15H 16H	2AH 2CH	0040H 0000H
Alternate OEM Command Set (00h = none exists)	17H 18H	2EH 30H	0000H 0000H
Address for Alternate OEM Extended Table (00h = none exists)	19H 1AH	32H 34H	0000H 0000H
Vcc_R Min. (write/erase) D7-D4: volt, D3-D0: 100 millivolt	1BH	36H	0027H
Vcc_R Max. (write/erase) D7-D4: volt, D3-D0: 100 millivolt	1CH	38H	0036H
Vpp Min. voltage(00H = no Vpp pin present)	1DH	3AH	0000H
Vpp Max. voltage(00H = no Vpp pin present)	1EH	3CH	0000H
Typical timeout per single byte/word write 2^N us	1FH	3EH	0004H
Typical timeout for Min. size buffer write 2^N us(00H = not supported)	20H	40H	0000H
Typical timeout per individual block erase 2^N ms	21H	42H	000AH
Typical timeout for full chip erase 2^N ms(00H = not supported)	22H	44H	0000H
Max. timeout for byte/word write 2^N times typical	23H	46H	0005H
Max. timeout for buffer write 2^N times typical	24H	48H	0000H
Max. timeout per individual block erase 2^N times typical	25H	4AH	0004H
Max. timeout for full chip erase 2^N times typical(00H = not supported)	26H	4CH	0000H
Device Size = 2^N byte	27H	4EH	0017H
Flash Device Interface description	28H 29H	50H 52H	0002H 0000H
Max. number of byte in multi-byte write = 2^N	2AH 2BH	54H 56H	0000H 0000H
Number of Erase Block Regions within device	2CH	58H	0002H
Erase Block Region 1 Information	2DH 2EH 2FH 30H	5AH 5CH 5EH 60H	0007H 0000H 0020H 0000H
Erase Block Region 2 Information	31H 32H 33H 34H	62H 64H 66H 68H	007EH 0000H 0000H 0001H
Erase Block Region 3 Information	35H 36H 37H 38H	6AH 6CH 6EH 70H	0000H 0000H 0000H 0000H
Erase Block Region 4 Information	39H 3AH 3BH 3CH	72H 74H 76H 78H	0000H 0000H 0000H 0000H

Table 14. Common NOR Flash Memory Interface Code

Description	Addresses (Word Mode)	Addresses (Byte Mode)	Data
Query-unique ASCII string "PRI"	40H 41H 42H	80H 82H 84H	0050H 0052H 0049H
Major version number, ASCII	43H	86H	0030H
Minor version number, ASCII	44H	88H	0030H
Address Sensitive Unlock(Bits 1-0) 0 = Required, 1= Not Required Silcon Revision Number(Bits 7-2)	45H	8AH	0000H
Erase Suspend 0 = Not Supported, 1 = To Read Only, 2 = To Read & Write	46H	8CH	0002H
Block Protect 0 = Not Supported, 1 = Supported	47H	8EH	0001H
Block Temporary Unprotect 00 = Not Supported, 01 = Supported	48H	90H	0001H
Block Protect/Unprotect scheme 04 = K8D1x16U mode	49H	92H	0004H
Simultaneous Operation (1) 00 = Not Supported, XX = Number of Blocks in Bank2	4AH	94H	00XXH
Burst Mode Type 00 = Not Supported, 01 = Supported	4BH	96H	0000H
Page Mode Type 00=Not supported, 01=4word page, 02=8word page	4CH	98H	0000H
ACC(Acceleration) Supply Minimum 00 = Not Supported, D7 - D4 : Volt, D3 - D0 : 100mV	4DH	9AH	0085H
ACC(Acceleration) Supply Maximum 00 = Not Supported, D7 - D4 : Volt, D3 - D0 : 100mV	4EH	9CH	00C5H
Top/Bottom Boot Block Flag 02H = Bottom Boot , 03H = Top Boot	4FH	9EH	000XH

NOTE:

1. The number of blocks in Bank2 is device dependent.
   KBB06A500(16Mb/48Mb) = 60h (96blocks)
   KBB05A500(48Mb/16Mb) = 40h (64blocks)

NOR FLASH DEVICE STATUS FLAGS

The NOR Flash memory has means to indicate its status of operation in the bank where a program or erase operation is in processes. Address must include bank address being excuted internal routine operation. The status is indicated by raising the device status flag via corresponding DQ balls or the $R/\overline{B}_R$ ball. The corresponding DQ balls are DQ7, DQ6, DQ5, DQ3 and DQ2. The status is as follows :

Table 15. Hardware Sequence Flags

	Status		DQ7	DQ6	DQ5	DQ3	DQ2	$R/\overline{B}_R$
In Progress	Programming		$\overline{DQ7}$	Toggle	0	0	1	0
	Block Erase or Chip Erase		0	Toggle	0	1	Toggle	0
	Erase Suspend Read	Erase Suspended Block	1	1	0	0	Toggle (Note 1)	1
	Erase Suspend Read	Non-Erase Suspended Block	Data	Data	Data	Data	Data	1
	Erase Suspend Program	Non-Erase Suspended Block	$\overline{DQ7}$	Toggle	0	0	1	0
Exceeded Time Limits	Programming		$\overline{DQ7}$	Toggle	1	0	No Toggle	0
	Block Erase or Chip Erase		0	Toggle	1	1	(Note 2)	0
	Erase Suspend Program		$\overline{DQ7}$	Toggle	1	0	No Toggle	0

NOTES:
1. DQ2 will toggle when the device performs successive read operations from the erase suspended block.
2. If DQ5 is High (exceeded timing limits), successive reads from a problem block will cause DQ2 to toggle.

DQ7 : $\overline{\text{Data}}$ Polling

When an attempt to read the device is made while executing the Internal Program, the complement of the data is written to DQ7 as an indication of the Routine in progress. When the Routine is completed an attempt to access to the device will produce the true data written to DQ7. When a user attempts to read the device during the Erase operation, DQ7 will be low. If the device is placed in the Erase Suspend Mode, the status can be detected via the DQ7 ball. If the system tries to read an address which belongs to a block that is being erased, DQ7 will be high. If a non-erased block address is read, the device will produce the true data to DQ7. If an attempt is made to program a protected block, DQ7 outputs complements the data for approximately 1µs and the device then returns to the Read Mode without changing data in the block. If an attempt is made to erase a protected block, DQ7 outputs complement data in approximately 100us and the device then returns to the Read Mode without erasing the data in the block.

DQ6 : Toggle Bit

Toggle bit is another option to detect whether an Internal Routine is in progress or completed. Once the device is at a busy state, DQ6 will toggle. Toggling DQ6 will stop after the device completes its Internal Routine. If the device is in the Erase Suspend Mode, an attempt to read an address that belongs to a block that is being erased will produce a high output of DQ6. If an address belongs to a block that is not being erased, toggling is halted and valid data is produced at DQ6.
If an attempt is made to program a protected block, DQ6 toggles for approximately 1us and the device then returns to the Read Mode without changing the data in the block. If an attempt is made to erase a protected block, DQ6 toggles for approximately 100µs and the device then returns to the Read Mode without erasing the data in the block.

DQ5 : Exceed Timing Limits

If the Internal Program/Erase Routine extends beyond the timing limits, DQ5 will go High, indicating program/erase failure.

DQ3 : Block Erase Timer

The status of the multi-block erase operation can be detected via the DQ3 pin. DQ3 will go High if 50µs of the block erase time window expires. In this case, the Internal Erase Routine will initiate the erase operation.Therefore, the device will not accept further write commands until the erase operation is completed. DQ3 is Low if the block erase time window is not expired. Within the block erase time window, an additional block erase command (30H) can be accepted. To confirm that the block erase command has been accepted, the software may check the status of DQ3 following each block erase command.

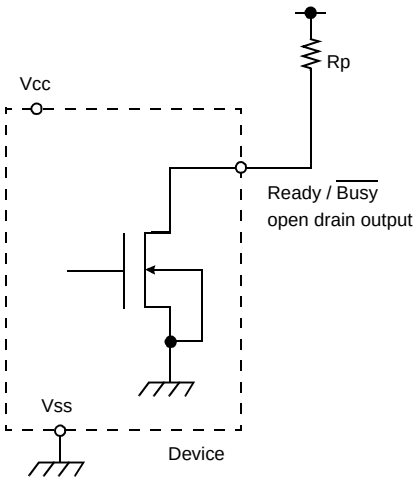
DQ2 : Toggle Bit 2

The device generates a toggling pulse in DQ2 only if an Internal Erase Routine or an Erase Suspend is in progress. When the device executes the Internal Erase Routine, DQ2 toggles only if an erasing block is read. Although the Internal Erase Routine is in the Exceeded Time Limits, DQ2 toggles only if an erasing block in the Exceeded Time Limits is read. When the device is in the Erase Suspend mode, DQ2 toggles only if an address in the erasing block is read. If a non-erasing block address is read during the Erase Suspend mode, then DQ2 will produce valid data. DQ2 will go High if the user tries to program a non-erase suspend block while the device is in the Erase Suspend mode. Combination of the status in DQ6 and DQ2 can be used to distinguish the erase operation from the program operation.

$R/\overline{B}_R$: Ready/$\overline{Busy}$

The NOR Flash memory has a Ready / $\overline{Busy}$ output that indicates either the completion of an operation or the status of Internal Algorithms. If the output is Low, the device is busy with either a program or an erase operation. If the output is High, the device is ready to accept any read/write or erase operation. When the $R/\overline{B}_R$ pin is low, the device will not accept any additional program or erase commands with the exception of the Erase Suspend command. If the NOR Flash memory is placed in an Erase Suspend mode, the $R/\overline{B}_R$ output will be High. For programming, the RY/ $\overline{BY}$ is valid ($R/\overline{B}_R$ = 0) after the rising edge of the fourth $\overline{WE}$ pulse in the four write pulse sequence. For Chip Erase, $R/\overline{B}_R$ is also valid after the rising edge of $\overline{WE}$ pulse in the six write pulse sequence. For Block Erase, $R/\overline{B}_R$ is also valid after the rising edge of the sixth $\overline{WE}$ pulse.

The pin is an open drain output, allowing two or more Ready/ $\overline{Busy}$ outputs to be OR-tied. An appropriate pull-up resistor is required for proper operation.



$$Rp = \frac{Vcc\ (Max.) - V_{OL}\ (Max.)}{I_{OL} + \Sigma I_L} = \frac{2.7\ V}{2.1mA + \Sigma I_L}$$

where ΣI_L is the sum of the input currents of all devices tied to the Ready / $\overline{Busy}$ pin.

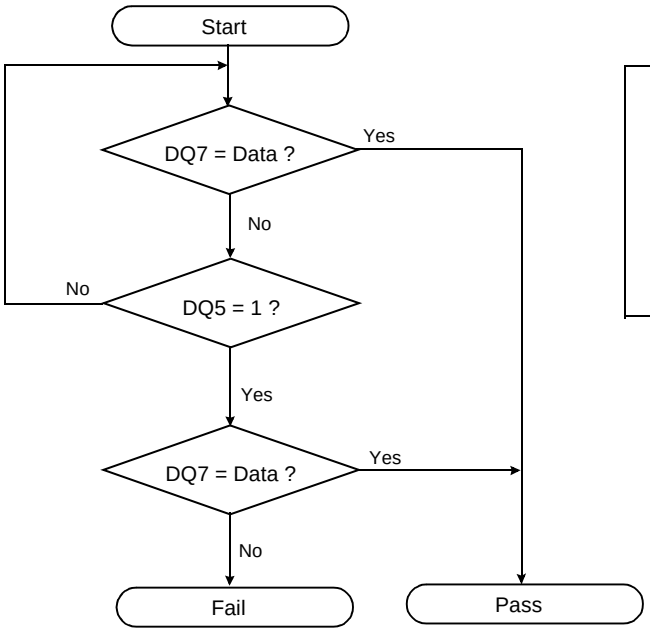


Figure 11. Data Polling Algorithms

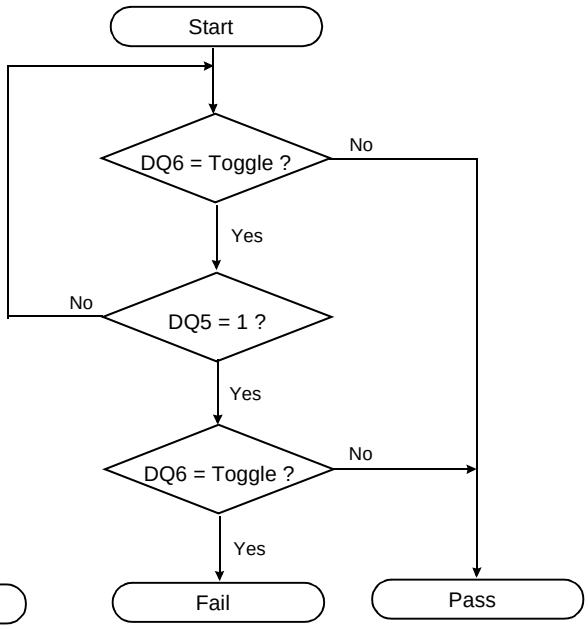
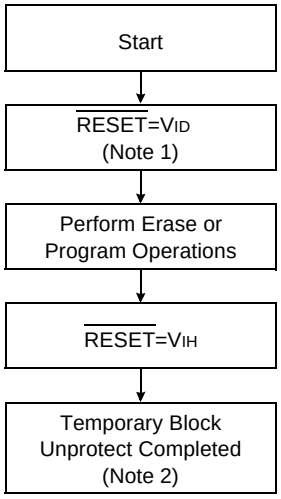


Figure 12. Toggle Bit Algorithms



NOTES:
1. All protected block groups are unprotected.
   (If $\overline{WP}$/ACC = V_{IL} , the two outermost boot blocks remain protected)
2. All previously protected block groups are protected once again.

Figure 13. Temporary Block Group Unprotect Routine

NAND FLASH MEMORY OPERATION

PAGE READ

Upon initial device power up, the device status is initially Read1 command(00h) latched. This operation is also initiated by writing 00h to the command register along with three address cycles. Once the command is latched, it does not need to be written for the following page read operation. Two types of operation are available : random read, serial page read. The random read mode is enabled when the page address is changed. The 264 words of data within the selected page are transferred to the data registers in less than 10μs(tR). The system controller can detect the completion of this data transfer(tR) by analyzing the output of R/$\overline{B}$ pin. Once the data in a page is loaded into the registers, they may be read out by sequential $\overline{RE}$ pulse of 50n period cycle. High to low transitions of the $\overline{RE}$ clock take out the data from the selected column address up to the last column address.

Read1 and Read2 commands determine pointer which selects either main area or spare area. The spare area(256 to 263 words) may be selectively accessed by writing the Read2 command. Addresses A_0 to A_2 set the starting address of spare area while addresses A_3 to A_7 must be "L". To move the pointer back to the main area, Read1 command(00h) is needed. Figures 16 through 21 show typical sequence and timing for each read operation.

Figure 14,15 details the sequence.

Figure 14. Read1 Operation

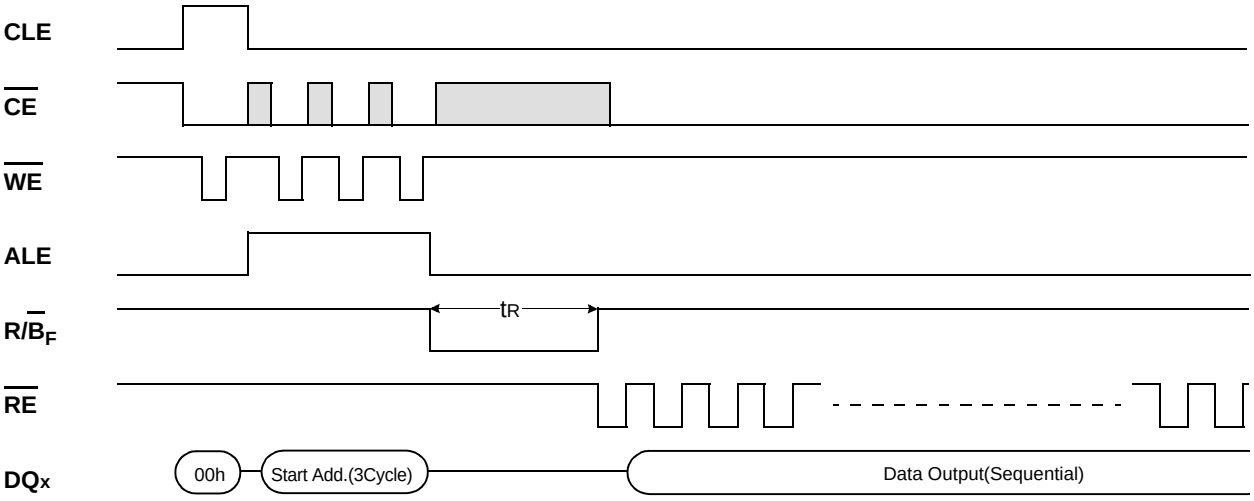
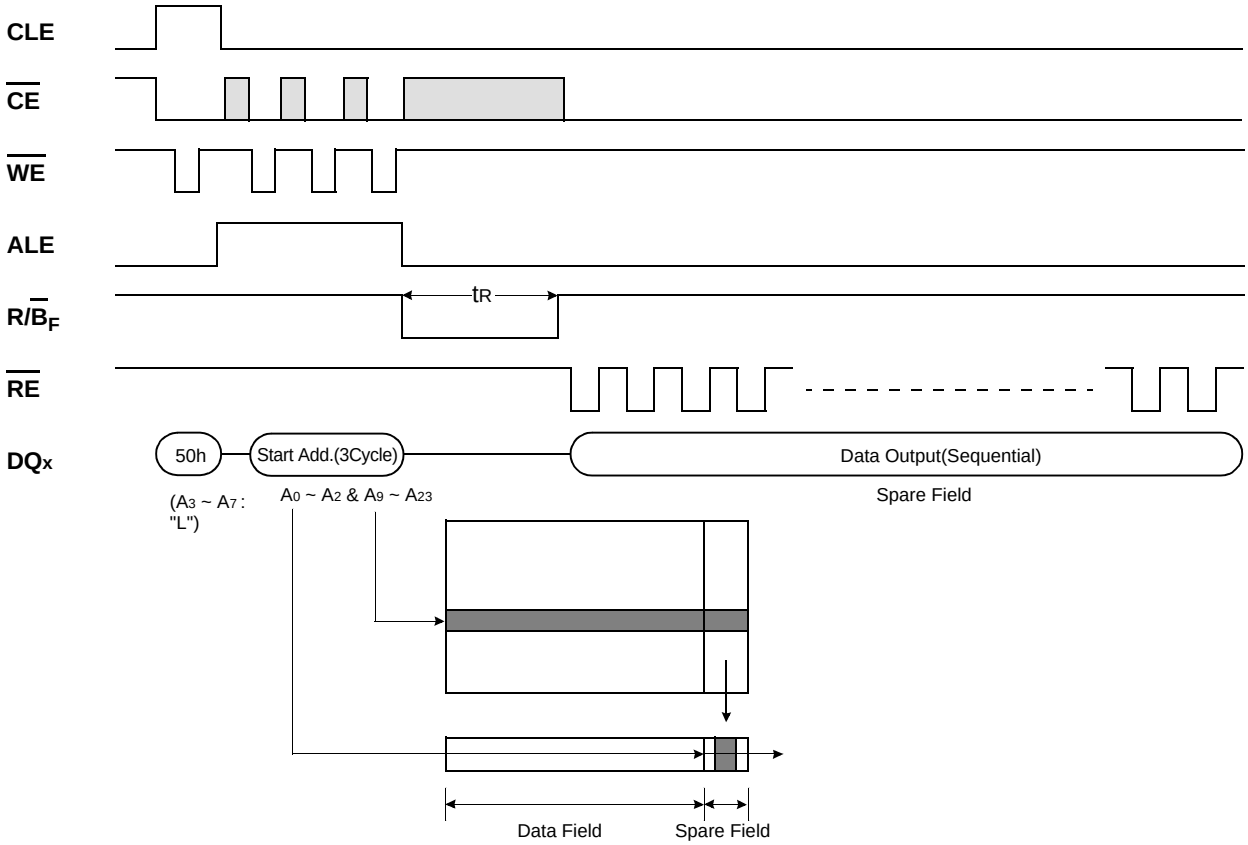


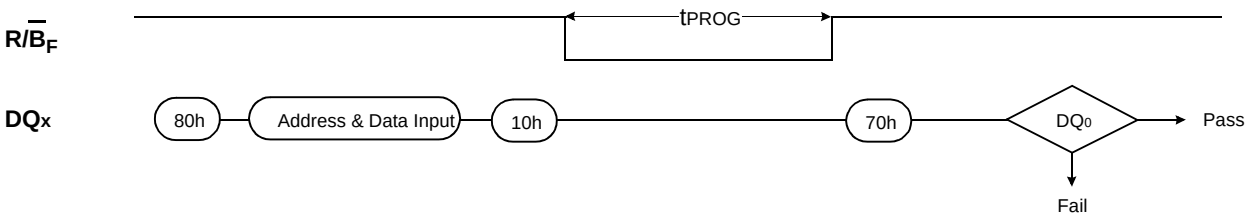
Figure 15. Read2 Operation



PAGE PROGRAM

The device is programmed basically on a page basis, but it allows multiple partial page program of one word or consecutive words up to 264, in a single page program cycle. The number of consecutive partial page program operation within the same page without intervening erase operation should not exceed 2 for main array and 3 for spare array. The addressing may be done in any random order in a block. Page program cycle consists of a serial data loading(up to 264 words of data) into the page register, and program of loaded data into the appropriate cell. Serial data loading can start in 2nd half array by moving pointer. About the pointer operation, please refer to the attached technical notes. Serial data loading is executed by entering the Serial Data Input command(80h) and three cycle address input and then serial data loading. The bytes except those to be programmed need not to be loaded. The Page Program confirm command(10h) initiates the programming process. Writing 10h alone without previously entering 80h will not initiate program process. The internal write controller automatically executes the algorithms and timings necessary for program and verification, thereby freeing the CPU for other tasks. Once the program process starts, the Read Status Register command may be entered, with $\overline{RE}$ and $\overline{CE}$ low, to read the status register. The CPU can detect the completion of a program cycle by monitoring the R/$\overline{B}$ output, or the Status bit(I/O 6) of the Status Register. Only the Read Status command and Reset command are valid while programming is in progress. When the Page Program is completed, the Write Status Bit(I/O 0) may be checked(Figure 16). The internal write verification detects only errors for "1"s that are not successfully programmed to "0"s. The command register remains in Read Status command mode until another valid command is written to the command register.
Figure 16 details the sequence.

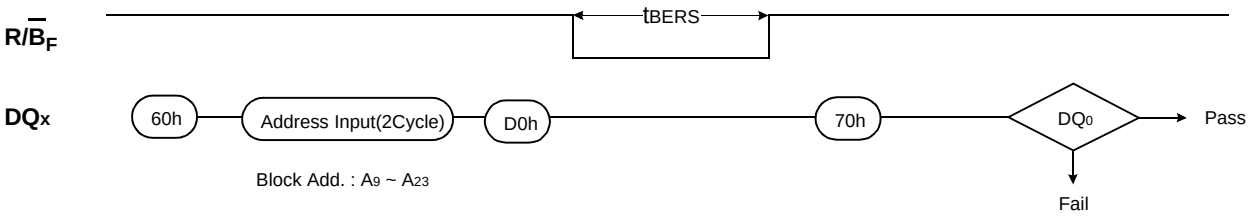
Figure 16. Program & Read Status Operation



BLOCK ERASE

The Erase operation is done on a block(16K Bytes) basis. Block Erase is executed by entering Erase Setup command(60h) and 2 cycle block addresses and Erase Confirm command(D0h). Only address A14 to A23 is valid while A9 to A13 is ignored. This two-step sequence of setup followed by execution command ensures that memory contents are not accidentally erased due to external noise condition. At the rising edge of $\overline{WE}$ after erase confirm command input, internal write controller handles erase and erase-verification. When the erase operation is completed, the Write Status Bit(I/O 0) may be checked.
Figure 6 details the sequence.

Figure 17. Block Erase Operation



READ STATUS

The device contains a Status Register which may be read to find out whether program or erase operation is completed, and whether the program or erase operation is completed successfully. After writing 70h command to command register, a read cycle takes out the content of the Status Register to the I/O pins on the falling edge of $\overline{CE_F}$ or $\overline{RE}$. This two line control allows the system to poll the progress of each device in multiple memory connections even when R/$\overline{B}$ pins are common-wired. $\overline{RE}$ or $\overline{CE_F}$ does not need to be toggled for updated status. Refer to table 16 for specific Status Register definitions. The command register remains in Status Read mode until further commands are issued to it. Therefore, if the status register is read during a random read cycle, a read command(00h or 50h) should be given before sequential page read cycle.

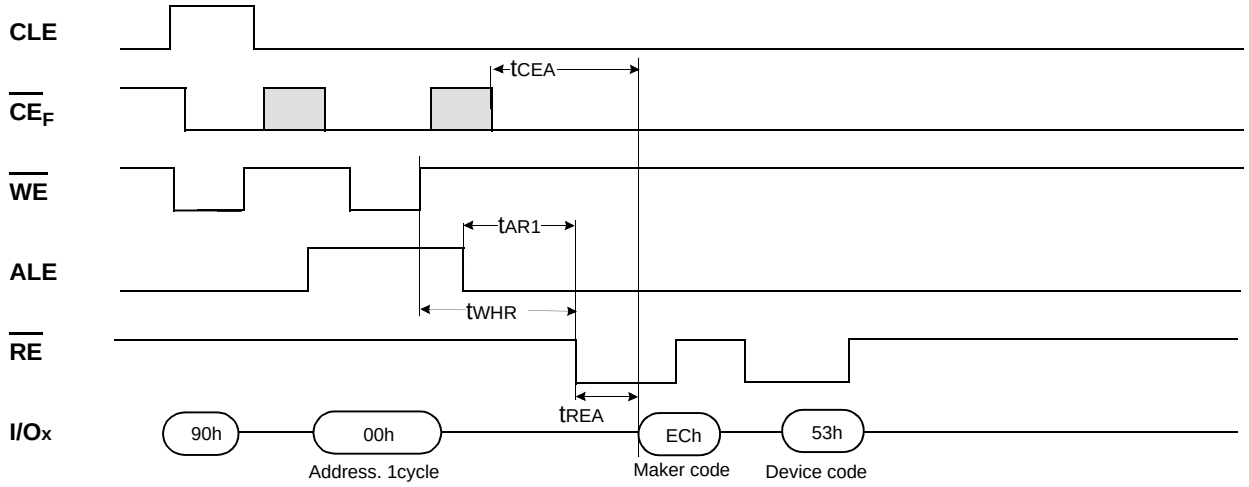
Table 16. Read Status Register Definition

DQ #	Status	Definition
DQ_0	Program / Erase	"0" : Successful Program / Erase
		"1" : Error in Program / Erase
DQ_1	Reserved for Future Use	"0"
DQ_2		"0"
DQ_3		"0"
DQ_4		"0"
DQ_5		"0"
DQ_6	Device Operation	"0" : Busy "1" : Ready
DQ_7	Write Protect	"0" : Protected "1" : Not Protected
$DQ_{8\sim15}$	Not use	Don't care

READ ID

The device contains a product identification mode, initiated by writing 90h to the command register, followed by an address input of 00h. Two read cycles sequentially output the manufacture code(ECh), and the device code (53h) respectively. The command register remains in Read ID mode until further commands are issued to it. Figure 18 shows the operation sequence.

Figure 18. Read ID Operation



RESET

The device offers a reset feature, executed by writing FFh to the command register. When the device is in Busy state during random read, program or erase mode, the reset operation will abort these operations. The contents of memory cells being altered are no longer valid, as the data will be partially programmed or erased. The command register is cleared to wait for the next command, and the Status Register is cleared to value C0h when $\overline{WP}$ is high. Refer to table 17 for device status after reset operation. If the device is already in reset state, new reset command will not be accepted by the command register. The R/$\overline{B}$ pin transitions to low for tRST after the Reset command is written. Reset command is not necessary for normal operation. Refer to Figure 19 below.

Figure 19. RESET Operation

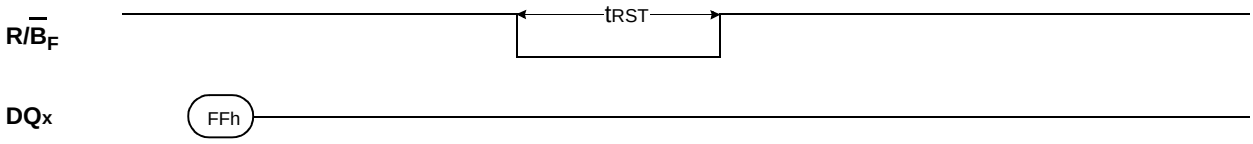


Table 17. Device Status

	After Power-up	After Reset
Operation Mode	Read 1	Waiting for next command

READY/$\overline{BUSY}$

The device has a R/$\overline{B}_F$ output that provides a hardware method of indicating the completion of a page program, erase and random read completion. The R/$\overline{B}_F$ pin is normally high but transitions to low after program or erase command is written to the command register or random read is started after address loading. It returns to high when the internal controller has finished the operation. The pin is an open-drain driver thereby allowing two or more R/$\overline{B}_F$ outputs to be Or-tied. Because pull-up resistor value is related to tr(R/$\overline{B}_F$) and current drain during busy(ibusy) , an appropriate value can be obtained with the following reference chart(Fig 20). Its value can be determined by the following guidance.

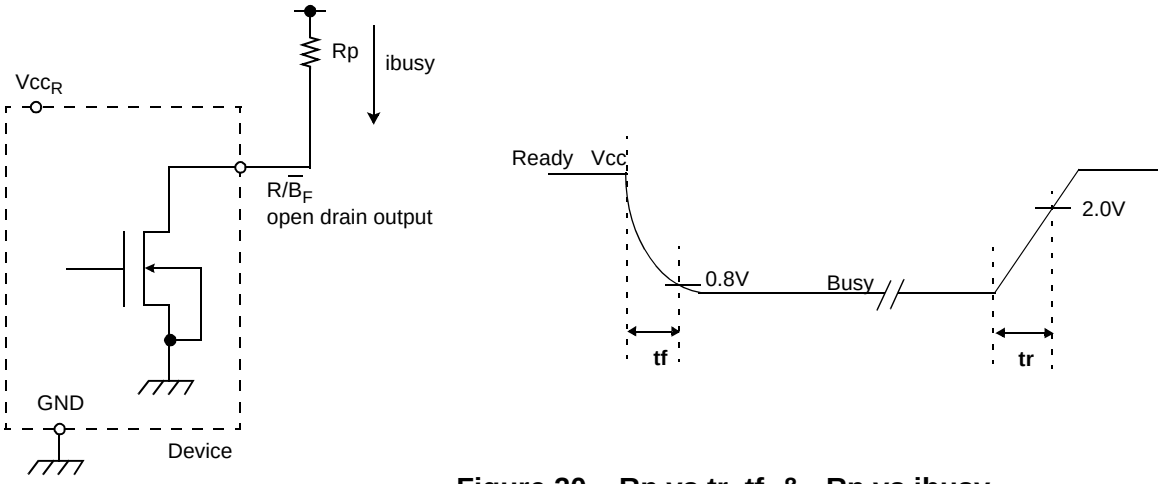
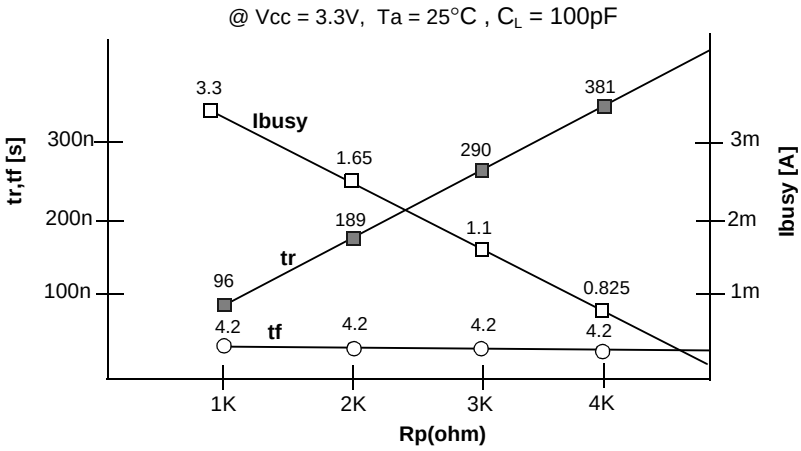


Figure 20. Rp vs tr ,tf & Rp vs ibusy



Rp value guidance

$$Rp = \frac{V_{CC}(Max.) - V_{OL}(Max.)}{I_{OL} + \Sigma I_L} = \frac{2.7V}{8mA + \Sigma I_L}$$

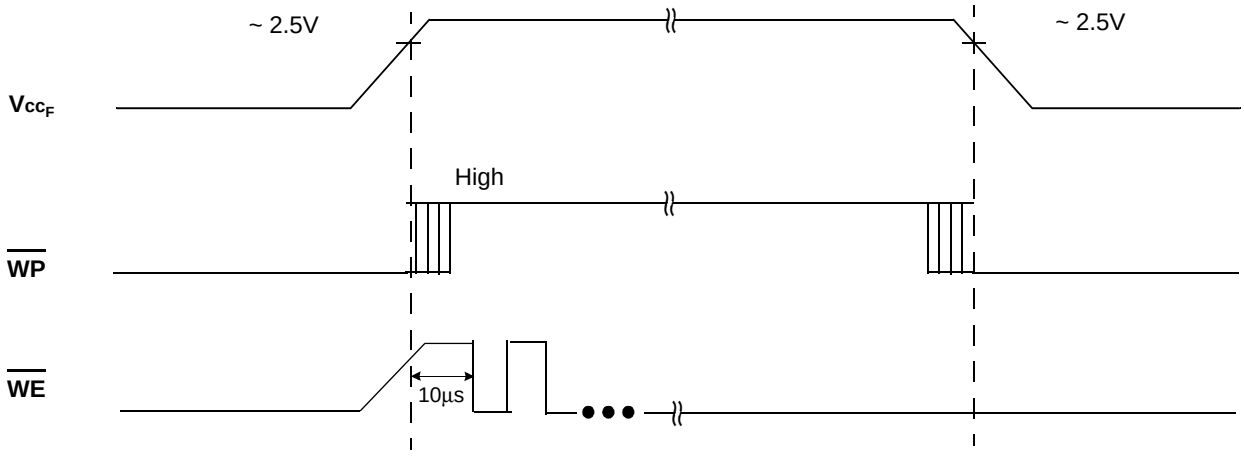
where I_L is the sum of the input currents of all devices tied to the R/$\overline{B}$ pin.

Rp(max) is determined by maximum permissible limit of tr

Data Protection & Powerup sequence

The device is designed to offer protection from any involuntary program/erase during power-transitions. An internal voltage detector disables all functions whenever Vcc_F is below about 1.3V. $\overline{WP}$ pin provides hardware protection and is recommended to be kept at V_{IL} during power-up and power-down and recovery time of minimum 1µs is required before internal circuit gets ready for any command sequences as shown in Figure 21. The two step command sequence for program/erase provides additional software protection.

Figure 21. AC Waveforms for Power Transition



NAND Flash Technical Notes

Invalid Block(s)

Invalid blocks are defined as blocks that contain one or more invalid bits whose reliability is not guaranteed by Samsung. The information regarding invalid block(s) is so called as the invalid block information. Devices ,regardless of having invalid block(s), have the same quality level because all valid blocks have same AC and DC characteristics. An invalid block(s) does not affect the performance of valid block(s) because it's bit line and common source line is isolated by a select transistor. The system design must be able to mask out invalid block(s) via address mapping. The 1st block, which is placed on 00h block address, is fully guaranteed to be a valid block, does not require Error Correction.

Identifying Invalid Block(s)

All device locations are erased(FFh) except locations where the invalid block(s) information is written prior to shipping. The invalid block(s) status is defined by the 1st and 6th word in the spare area. Samsung makes sure that either 1st and 2nd page of every invalid block has non-FFFFh data at the column address of 256 and 261. Since invalid block information is also erasable in most cases, it is impossible to recover the information once it was erased. Therefore, system must be able to recognize the invalid block(s) based on the original invalid block information and create invalid block table via the following suggested flow chart(Figure 22). Any intentional erasure of the original invalid block information is prohibited.

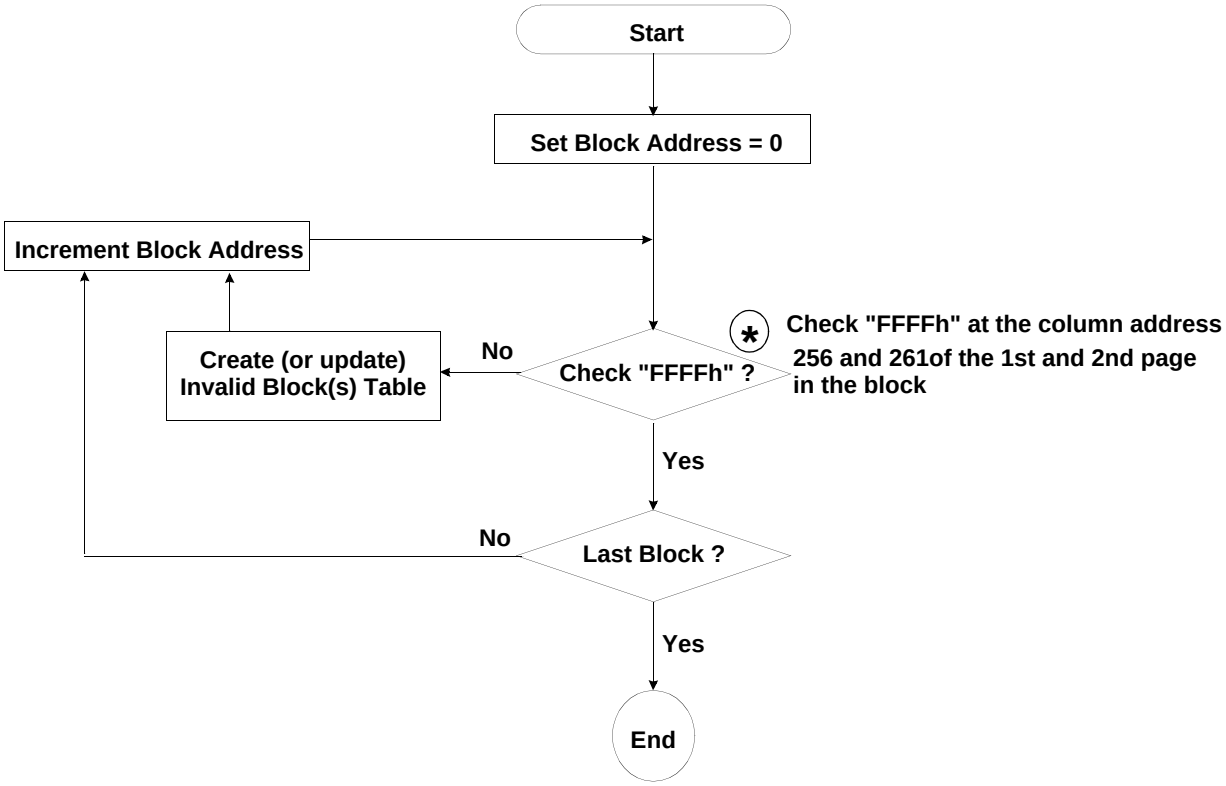


Figure 22. Flow chart to create invalid block table

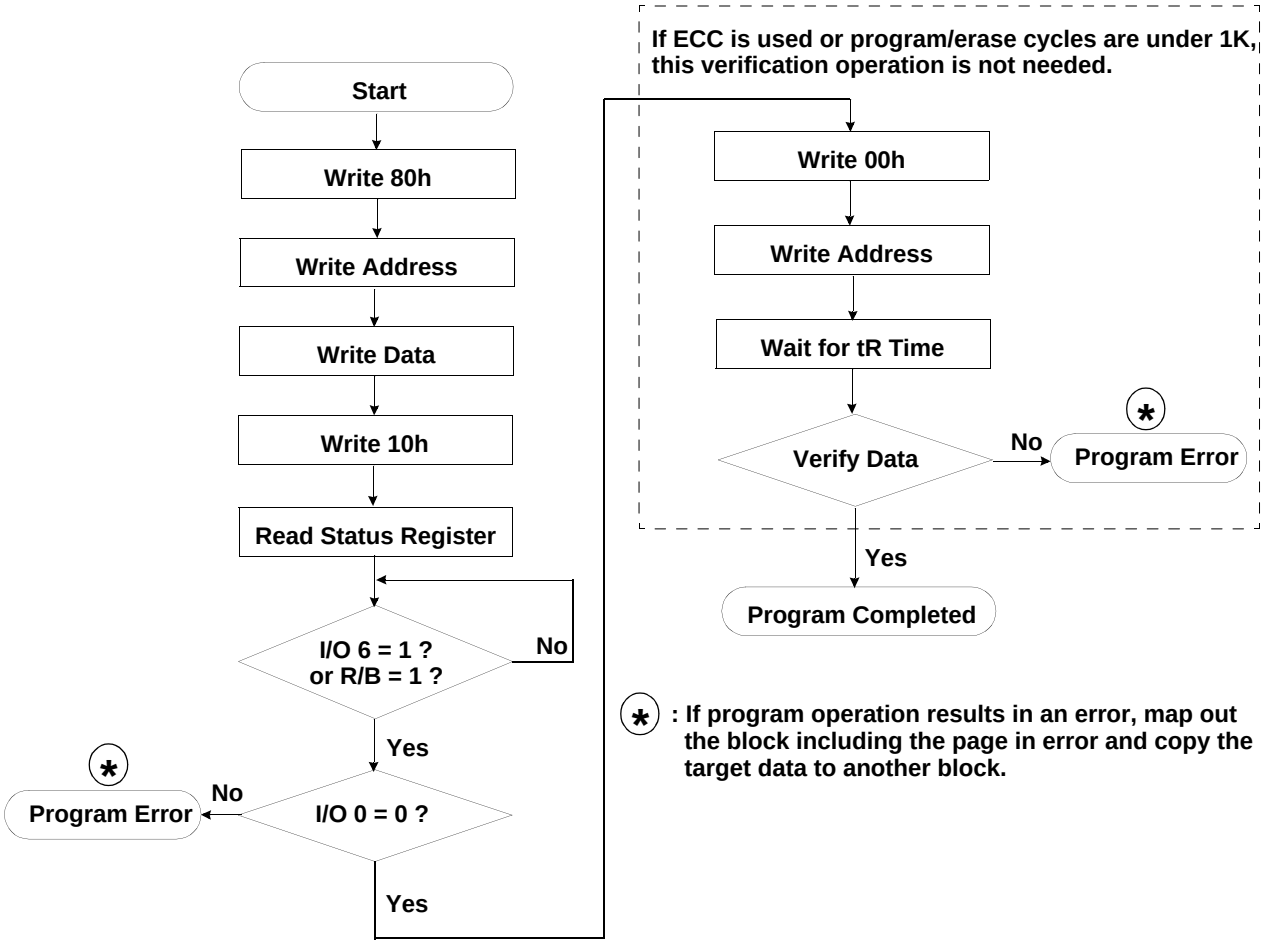
NAND Flash Technical Notes

Error in write operation

Over its life time, the additional invalid blocks may develop with NAND Flash memory. Refer to the qualification report for actual data. The following possible failure modes should be considered to implement a highly reliable system. In the case of status read failure after erase or program, block replacement should be done. Because program status fail during a page program does not affect the data of the other pages in the same block, block replacement can be executed with a page-sized buffer by finding an erased empty block and reprogramming the current target data and copying the rest of the replaced block. The said additional block failure rate does not include those reclaimed blocks.

Failure Mode		Detection and Countermeasure sequence
Write	Erase Failure	Status Read after Erase --> Block Replacement
	Program Failure	Status Read after Program --> Block Replacement Read back (Verify after Program) --> Block Replacement

Figure 24. Flash Program Flow Chart



NAND Flash Technical Notes

Figure 24. Flash Erase Flow Chart

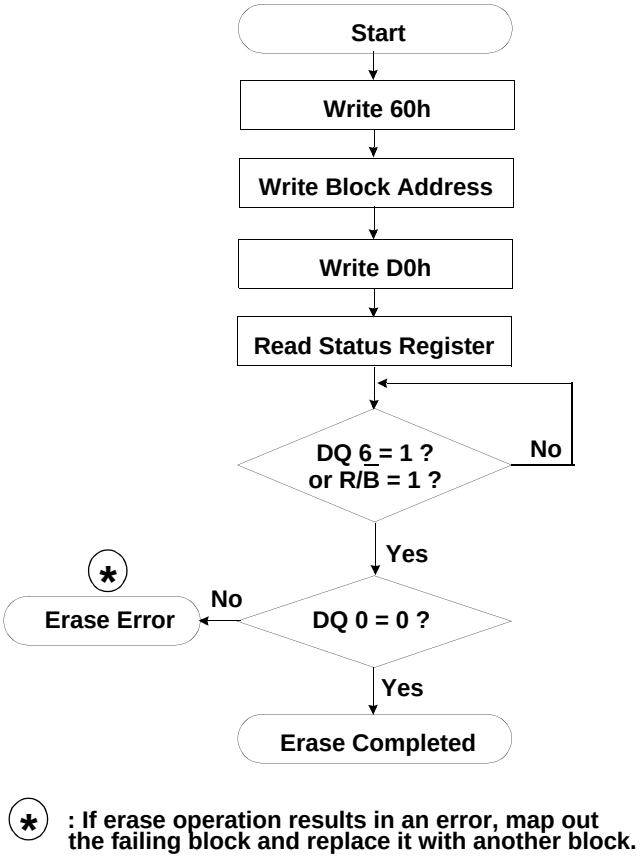
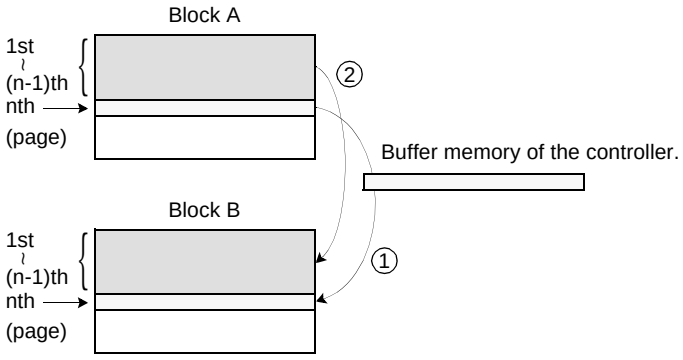


Figure 25. Block Replacement



* Step1
When an error happens in the nth page of the Block 'A' during erase or program operation.
* Step2
Copy the nth page data of the Block 'A' in the buffer memory to the nth page of another free block. (Block 'B')
* Step3
Then, Copy the 1st ~ (n-1)th data to the same location of the Block 'B'.
* Step4
Do not further erase Block 'A' by creating a 'invalid Block' table or other appropriate scheme.

NAND Flash Technical Notes

Pointer Operation of NAND Flash

Samsung NAND Flash(x16) has two address pointer commands as a substitute for the two most significant column addresses. '00h' command sets the pointer to 'A' area(0~255word), and '50h' command sets the pointer to 'B' area(256~263word). With these commands, the starting column address can be set to any of a whole page(0~263word). '00h' or '50h' is sustained until another address pointer command is inputted. To program data starting from 'A' or 'B' area, '00h' or '50h' command must be inputted before '80h' command is written. A complete read operation prior to '80h' command is not necessary.

Table 18. Destination of the pointer

Command	Pointer position	Area
00h 50h	0 ~ 255 word 256 ~ 263 word	main array(A) spare array(B)

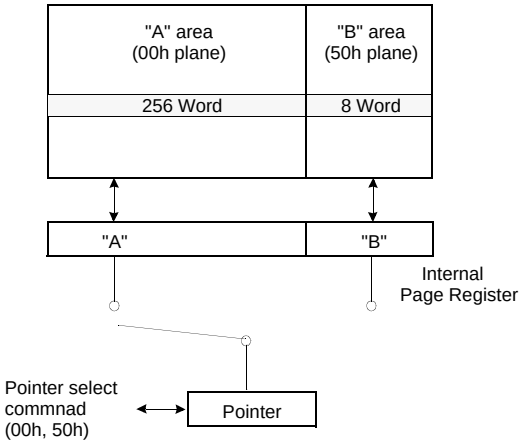
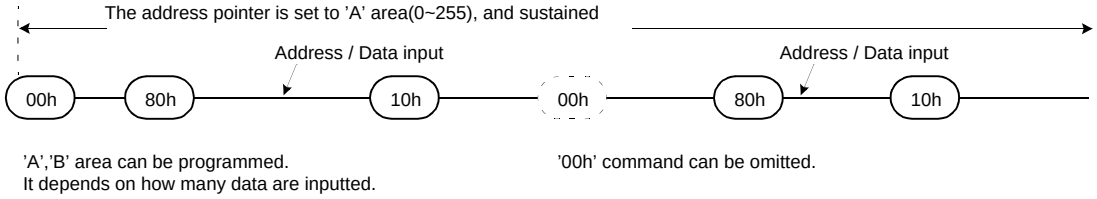


Figure 26. Block Diagram of Pointer Operation

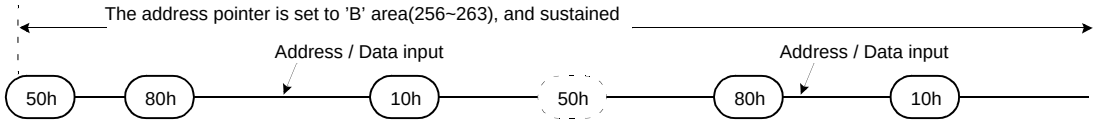
(1) Command input sequence for programming 'A' area



'A','B' area can be programmed.
It depends on how many data are inputted.

'00h' command can be omitted.

(2) Command input sequence for programming 'B' area



Only 'B' area can be programmed.

'50h' command can be omitted.

NAND Flash Technical Notes

System Interface Using $\overline{CE}$ don't-care.

For an easier system interface, $\overline{CE}_F$ may be inactive during data-loading or sequential data-reading as shown below. The internal 264word page registers are utilized as seperate buffers for this operation and the system design gets more flexible. In addition, for voice or audio applications which use slow cycle time on the order of u-seconds, de-activating $\overline{CE}_F$ during the data-loading and reading would provide significant saving in power consumption.

Figure 27. Program Operation with $\overline{CE}_F$ don't-care.

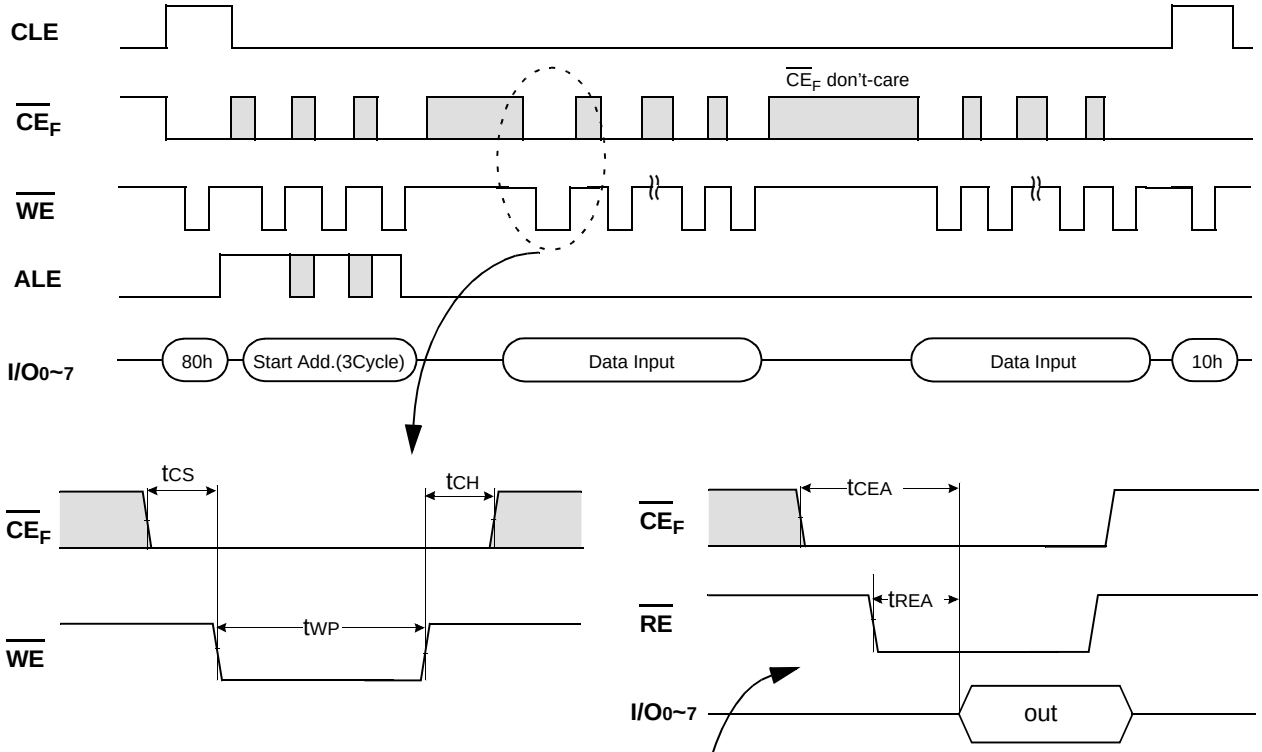
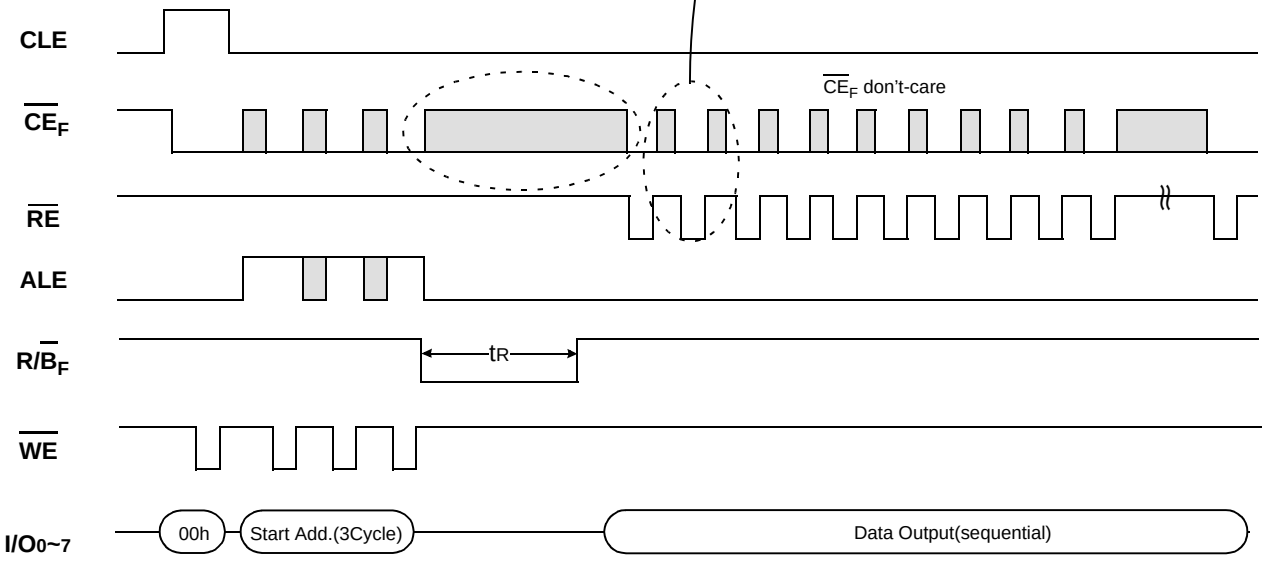


Figure 28. Read Operation with $\overline{CE}_F$ don't-care.



ABSOLUTE MAXIMUM RATINGS

Parameter		Symbol	Rating	Unit
Voltage on any pin relative to V_{SS}	Vcc	Vcc_R,Vcc_F,Vcc_U,$VccQ_U$	-0.2 to Vcc+0.3	V
	$\overline{RESET}$	V_{IN}	-0.2 to 12.5V	
	$\overline{WP}$/ACC		-0.2 to 12.5V	
	Other Balls		-0.2 to 3.6V	
Temperature Under Bias		T_{BIAS}	-40 to + 125	°C
Storage Temperature		T_{STG}	-65 to + 150	
Operating Temperature		T_A	-25 to + 85	

NOTE:
1. Minimum DC voltage is -0.2V on input/output balls. During transitions, this level may undershoot to -1.0V for periods <20ns. Maximum DC voltage on input/output balls is V_{CC}+0.3V which, during transitions, may overshoot to V_{CC}+1.0V for periods <20ns.
2. Minimum DC voltage is -0.2V on Reset and WP/ACC balls. During transitions, this level may undershoot to -1.0V for periods <20ns. Maximum DC voltage on on Reset and WP/ACC balls is 12.5V which, during transitions, may overshoot to 14.0V for periods <20ns.
3. Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED OPERATING CONDITIONS

(Voltage reference to Vss, T_A=-25 to 85°C)

Parameter	Symbol	Min	Typ.	Max	Unit
Supply Voltage	Vcc_R,Vcc_F,Vcc_U,$VccQ_U$	2.7	2.9	3.1	V
Supply Voltage	V_{SS}	0	0	0	V

DC AND OPERATING CHARACTERISTICS(Recommended operating conditions otherwise noted.)

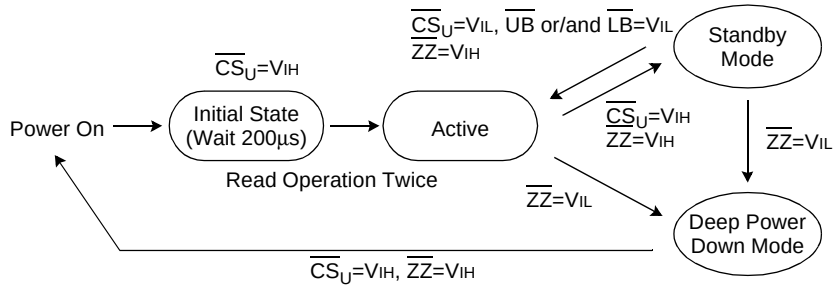
Parameter	Symbol	Test Conditions	Min	Max	Unit
Input LeaKAge Current	I_{LI}	V_{IN}=Vss to Vcc, Vcc=Vcc_{max}	-10	10	µA
Output LeaKAge Current	I_{LO}	V_{OUT}=Vss to Vcc, Vcc=Vcc_{max}, $\overline{OE}$=V_{IH}	-10	10	µA
Input Low Voltage Level	V_{IL}		-0.3	0.5	V
Input High Voltage Level	V_{IH}		2.2	Vcc+0.3	
Output Low Voltage Level	V_{OL}	I_{OL}= 2.1mA, Vcc = Vcc_{min}	-	0.4	
Output High Voltage Level	V_{OH}	I_{OH}= -1.0mA, Vcc = Vcc_{min}	2.3	-	

DC AND OPERATING CHARACTERISTICS

Parameter		Symbol	Test Conditions		Min	Typ	Max	Unit
NOR Flash (each device)	$\overline{RESET}$ Input Leakage Current	I_{LIT}	$Vcc_R=Vcc_{Rmax}$, $\overline{RESET}$=12.5V		-	-	35	µA
	$\overline{WP}$/ACC Input Leakage Current	I_{LIW}	$Vcc_R=Vcc_{Rmax}$, $\overline{WP}$/ACC=12.5V		-	-	35	µA
	Active Read Current (1)	I_{CC1}	$\overline{CE}_R=V_{IL}$, $\overline{OE}=V_{IH}$	5MHz	-	14	20	mA
				1MHz	-	3	6	
	Active Write Current (2)	I_{CC2}	$\overline{CE}_R=V_{IL}$, $\overline{OE}=V_{IH}$		-	15	30	mA
	Read While Program Current (3)	I_{CC3}	$\overline{CE}_R=V_{IL}$, $\overline{OE}=V_{IH}$		-	25	50	mA
	Read While Erase Current (3)	I_{CC4}	$\overline{CE}_R=V_{IL}$, $\overline{OE}=V_{IH}$		-	25	50	mA
	Program While Erase Suspend Current	I_{CC5}	$\overline{CE}_R=V_{IL}$, $\overline{OE}=V_{IH}$		-	15	35	mA
	ACC Accelerated Program Current	I_{ACC}	$\overline{CE}_R=V_{IL}$, $\overline{OE}=V_{IH}$	ACC Ball	-	5	10	mA
				Vcc_R Ball	-	15	30	mA
	Standby Current	I_{SB1}	$Vcc_R=Vcc_R$max, $\overline{CE}_R=Vcc_R\pm$ 0.3V, $\overline{RESET}=Vcc_R\pm$ 0.3V, $\overline{WP}$/ACC=$Vcc_R\pm$ 0.3V or Vss± 0.3V		-	10	30	µA
	Standby Curren During Reset	I_{SB2}	$Vcc_R=Vcc_{Rmax}$, $\overline{RESET}$=Vss±0.3V, $\overline{WP}$/ACC=$Vcc_R\pm$ 0.3V or Vss± 0.3V		-	10	30	µA
	Automatic Sleep Mode	I_{SB3}	$V_{IH}=Vcc_R\pm$ 0.3V, V_{IL}=Vss ± 0.3V, $\overline{OE}=V_{IL}$, $I_{OL}=I_{OH}$=0		-	10	30	µA
	Voltage for $\overline{WP}$/ACC Block Temporarily Unprotect and Program Acceleration (4)	V_{HH}	Vcc_R= 2.9V ± 0.2V		8.5	-	12.5	V
	Voltage for Autoselect and Block Protect (4)	V_{ID}	Vcc_R= 2.9V ± 0.2V		8.5	-	12.5	V
	Low Vcc_R Lock-out Voltage (5)	V_{LKO}			1.8	-	2.5	V
NAND Flash	Active Sequential Read Currnt	I_{CC1f}	tRC=50ns,$\overline{CE}_F=V_{IL}$, I_{OUT}=0mA, $Vcc_F=Vcc_F$max		-	10	20	mA
	Active Program Current	I_{CC2f}	$Vcc_F=Vcc_F$max		-	10	20	mA
	Active Erase Current	I_{CC3f}	$Vcc_F=Vcc_F$max		-	10	20	mA
	Stand_by Current(CMOS)	I_{SB2f}	$\overline{CE}_F=Vcc_F$, $\overline{WP}$=0V/Vcc_F		-	10	50	µA
U*t*RAM	Operating Current	I_{CC1u}	Cycle time=1µs, 100% duty, I_{IO}=0mA, $\overline{CS}_U\leq$0.2V, $\overline{ZZ}\geq VccQ_U$-0.2V, $V_{IN}\leq$0.2V or $V_{IN}\geq VccQ_U$-0.2V		-	6	15	mA
		I_{CC2u}	Cycle time=tRC+3tPC, 100% duty, I_{IO}=0mA, $\overline{CS}_U$=VIL, $\overline{ZZ}=V_{IH}$, $V_{IN}=V_{IL}$ or V_{IH}		-	35	45	mA
	Stand_by Current(CMOS)	I_{SB1u}	$\overline{CS}u\geq VccQ_U$-0.2V, $\overline{ZZ}\geq VccQ_U$-0.2V, Other inputs =0~$VccQ_U$		-	150	200	µA
	Deep Power Down	I_{SBD}	$\overline{ZZ}\leq$0.2V, Other input =0~$VccQ_U$		-	10	20	µA

NOTES:
1. The I_{CC} current listed includes both the DC operating current and the frequency dependent component(at 5 MHz).
   The read current is typically 14 mA (@ Vcc_R=2.9V , $\overline{OE}$ at V_{IH}.)
2. I_{CC} active during Internal Routine(program or erase) is in progress.
3. I_{CC} active during Read while Write is in progress.
4. The high voltage (V_{HH} or V_{ID}) must be used in the range of Vcc_R = 2.9V ± 0.2V
5. Not 100% tested.
6. Typical values are measured at Vcc = 2.9V, Ta=25°C, not 100% tested.

Standby Mode State Machines(U*t*RAM)



Standby Mode Characteristic(U*t*RAM)

Power Mode	Memory Cell Data	Standby Current(μA)	Wait Time(μs)
Standby	Valid	200	0
Deep Power Down	Invaild	20	200

CAPACITANCE (T_A = 25 °C, V_{CC} = 2.9V, f = 1.0MHz)

Item	Symbol	Test Condition	Min	Max	Unit
Input Capacitance	C_{IN}	V_{IN}=0V	-	40	pF
Input/Output Capacitance	C_{IO}	V_{IO}=0V	-	40	pF

NOTE: Capacitance is periodically sampled and not 100% tested.

VALID BLOCK OF NAND FLASH MEMORY

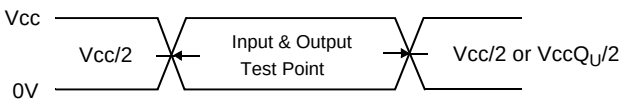
Parameter	Symbol	Min	Typ.	Max	Unit
Valid Block Number	N_{VB}	1004	-	1024	Blocks

NOTE:
1. The NAND Flash memory may include invalid blocks when first shipped. Additional invalid blocks may develop while being used. The number of valid blocks is presented with both cases of invalid blocks considered. Invalid blocks are defined as blocks that contain one or more bad bits.
   Do not try to access these invalid blocks for program and erase.
   Refer to the attached technical notes for a appropriate management of invalid blocks.
2. The 1st block, which is placed on 00h block address, is fully guaranteed to be a valid block, does not require Error Correction.

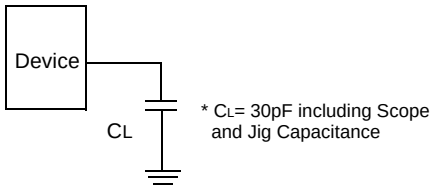
AC TEST CONDITION

Parameter	Value
Input Pulse Levels	0V to Vcc
Input Rise and Fall Times	5ns
Input and Output Timing Levels	Vcc/2 or $VccQ_U$/2
Output Load	C_L = 30pF

NOTE: AC test inputs are driven at Vcc_R, Vcc_F or Vcc_U for a logic "1" and 0V for a logic "0". Input timing begins, and output timing ends, at Vcc_R/2, Vcc_F/2 or $VccQ_U$/2. Input rise and fall times (10% - 90%)<5ns. Worst case speed condition are when Vcc_R = Vcc_Rmin, Vcc_F= Vcc_Fmin or $VccQ_U$ = $VccQ_U$min.



Input Pulse and Test Point



Output Load

NOR Flash AC CHARACTERISTICS
Write(Erase/Program)Operations
Alternate $\overline{WE}$ Controlled Write

Parameter		Symbol	70ns		Unit
			Min	Max	
Write Cycle Time (1)		t_{WC}	70	-	ns
Address Setup Time		t_{AS}	0	-	ns
		t_{ASO}	55	-	ns
Address Hold Time		t_{AH}	45	-	ns
		t_{AHT}	0	-	ns
Data Setup Time		t_{DS}	35	-	ns
Data Hold Time		t_{DH}	0	-	ns
Output Enable Setup Time (1)		t_{OES}	0	-	ns
Output Enable Hold Time	Read (1)	t_{OEH1}	0	-	ns
	Toggle and $\overline{Data}$ Polling (1)	t_{OEH2}	10	-	ns
$\overline{CE}_R$ Setup Time		t_{CS}	0	-	ns
$\overline{CE}_R$ Hold Time		t_{CH}	0	-	ns
Write Pulse Width		t_{WP}	35	-	ns
Write Pulse Width High		t_{WPH}	25	-	ns
Programming Operation	Word	t_{PGM}	14(typ.)		µs
	Byte		9(typ.)		µs
Accelerated Programming Operation	Word	t_{ACCPGM}	9(typ.)		µs
	Byte		7(typ.)		µs
Block Erase Operation (2)		t_{BERS}	0.7(typ.)		sec
V_{CC_R} Set Up Time		t_{VCS}	50	-	µs
Write Recovery Time from R/$\overline{B}_R$		t_{RB}	0	-	ns
$\overline{RESET}$ High Time Before Read		t_{RH}	50	-	ns
$\overline{RESET}$ to Power Down Time		t_{RPD}	20	-	µs
Program/Erase Valid to R/$\overline{B}_R$ Delay		t_{BUSY}	90	-	ns
V_{ID} Rising and Falling Time		t_{VID}	500	-	ns
$\overline{RESET}$ Pulse Width		t_{RP}	500	-	ns
$\overline{RESET}$ Low to R/$\overline{B}_R$ High		t_{RRB}	-	20	µs
$\overline{RESET}$ Setup Time for Temporary Unprotect		t_{RSP}	1	-	µs
$\overline{RESET}$ Low Setup Time		t_{RSTS}	500	-	ns
$\overline{RESET}$ High to Address Valid		t_{RSTW}	200	-	ns
Read Recovery Time Before Write		t_{GHWL}	0	-	ns
$\overline{CE}$ High during toggling bit polling		t_{CEPH}	20	-	ns
$\overline{OE}$ High during toggling bit polling		t_{OEPH}	20	-	ns

NOTES: 1. Not 100% tested.
2. The duration of the Program or Erase operation varies and is calculated in the internal algorithms.

NOR Flash AC CHARACTERISTICS
Write(Erase/Program)Operations
Alternate $\overline{CE}_R$ Controlled Writes

Parameter			Symbol	70ns		Unit
				Min	Max	
Write Cycle Time (1)			t_{WC}	70	-	ns
Address Setup Time			t_{AS}	0	-	ns
Address Hold Time			t_{AH}	45	-	ns
Data Setup Time			t_{DS}	35	-	ns
Data Hold Time			t_{DH}	0	-	ns
Output Enable Setup Time (1)			t_{OES}	0	-	ns
Output Enable Hold Time	Read (1)		t_{OEH1}	0	-	ns
	Toggle and $\overline{Data}$ Polling (1)		t_{OEH2}	10	-	ns
$\overline{WE}$ Setup Time			t_{WS}	0	-	ns
$\overline{WE}$ Hold Time			t_{WH}	0	-	ns
$\overline{CE}_R$ Pulse Width			t_{CP}	35	-	ns
$\overline{CE}_R$ Pulse Width High			t_{CPH}	25	-	ns
Programming Operation		Word	t_{PGM}	14(typ.)		µs
		Byte		9(typ.)		µs
Accelerated Programming Operation		Word	t_{ACCPGM}	9(typ.)		µs
		Byte		7(typ.)		µs
Block Erase Operation (2)			t_{BERS}	0.7(typ.)		sec
$\overline{BYTE}$ Switching Low to Output HIGH-Z			t_{FLQZ}	25	-	ns

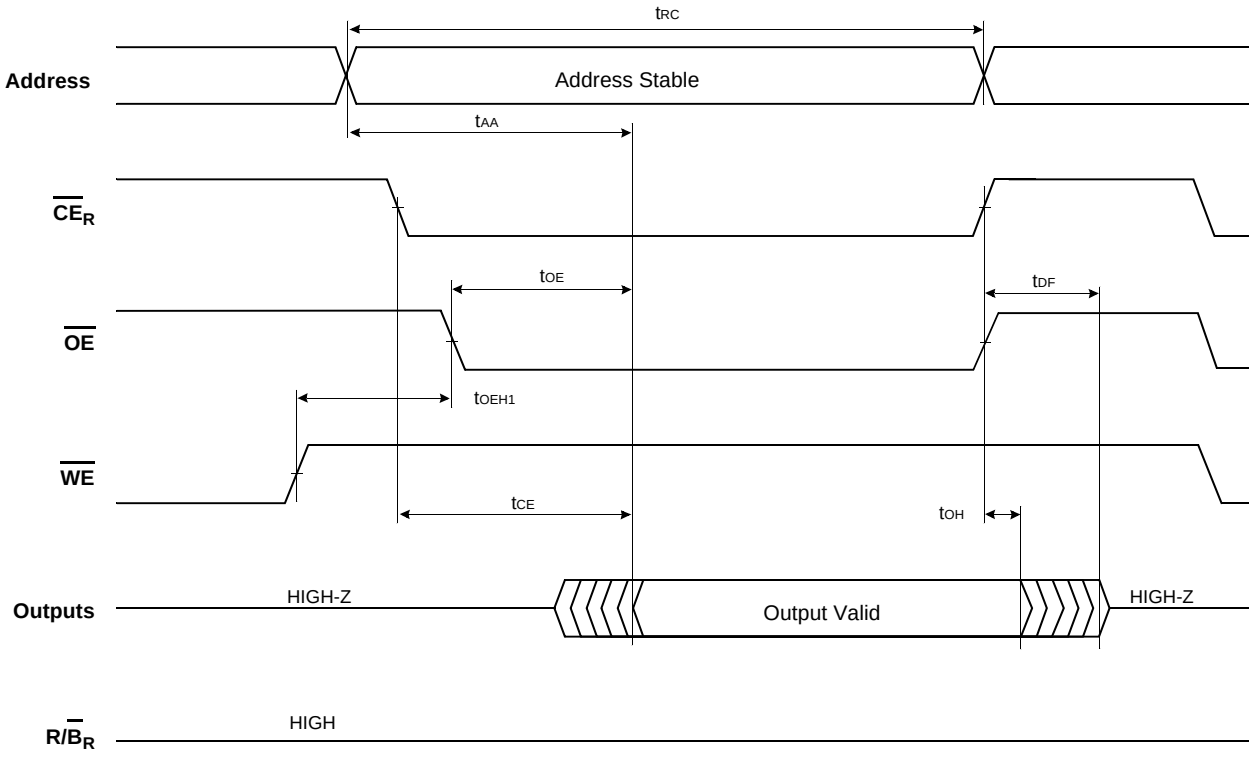
NOTES: 1. Not 100% tested.
2.This does not include the preprogramming time.

ERASE AND PROGRAM PERFORMANCE

Parameter		Limits			Unit	Comments
		Min	Typ	Max		
Block Erase Time		-	0.7	15	sec	Excludes 00H programming prior to erasure
Chip Erase Time		-	98	-	sec	
Word Programming Time		-	14	330	µs	Excludes system-level overhead
Byte Programming Time		-	9	210	µs	Excludes system-level overhead
Accelerated Byte/Word Program Time	Word Mode	-	9	210	µs	Excludes system-level overhead
	Byte Mode	-	7	150	µs	Excludes system-level overhead
Chip Programming Time	Word Mode	-	59	177	sec	Excludes system-level overhead
	Byte Mode	-	75	225	sec	
Erase/Program Endurance		100,000	-	-	cycles	Minimum 100,000 cycles guaranteed

NOTES: 1. 25 °C, Vcc_R = 2.9V 100,000 cycles, typical pattern.
2. System-level overhead is defined as the time required to execute the four bus cycle command necessary to program each byte. In the preprogramming step of the Internal Erase Routine, all bytes are programmed to 00H before erasure.

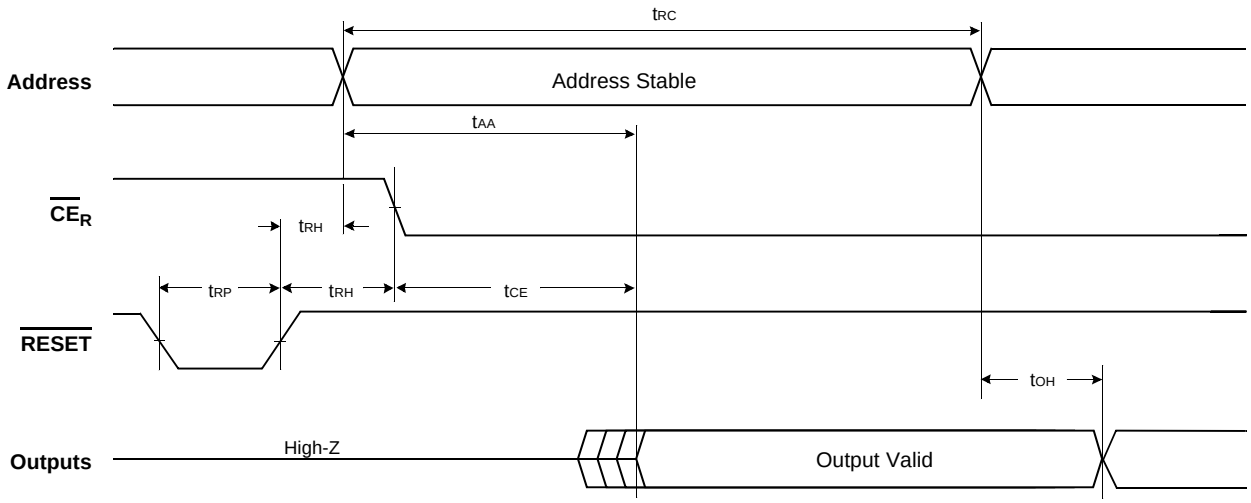
NOR Flash SWITCHING WAVEFORMS
Read Operations



Parameter	Symbol	70ns		Unit
		Min	Max	
Read Cycle Time	t_{RC}	70	-	ns
Address Access Time	t_{AA}	-	70	ns
Chip Enable Access Time	t_{CE}	-	70	ns
Output Enable Time	t_{OE}	-	25	ns
$\overline{CE}_R$ & $\overline{OE}$ Disable Time (1)	t_{DF}	-	16	ns
Output Hold Time from Address, $\overline{CE}_R$ or $\overline{OE}$	t_{OH}	0	-	ns
$\overline{OE}$ Hold Time	t_{OEH1}	0	-	ns

NOTE: 1. Not 100% tested.

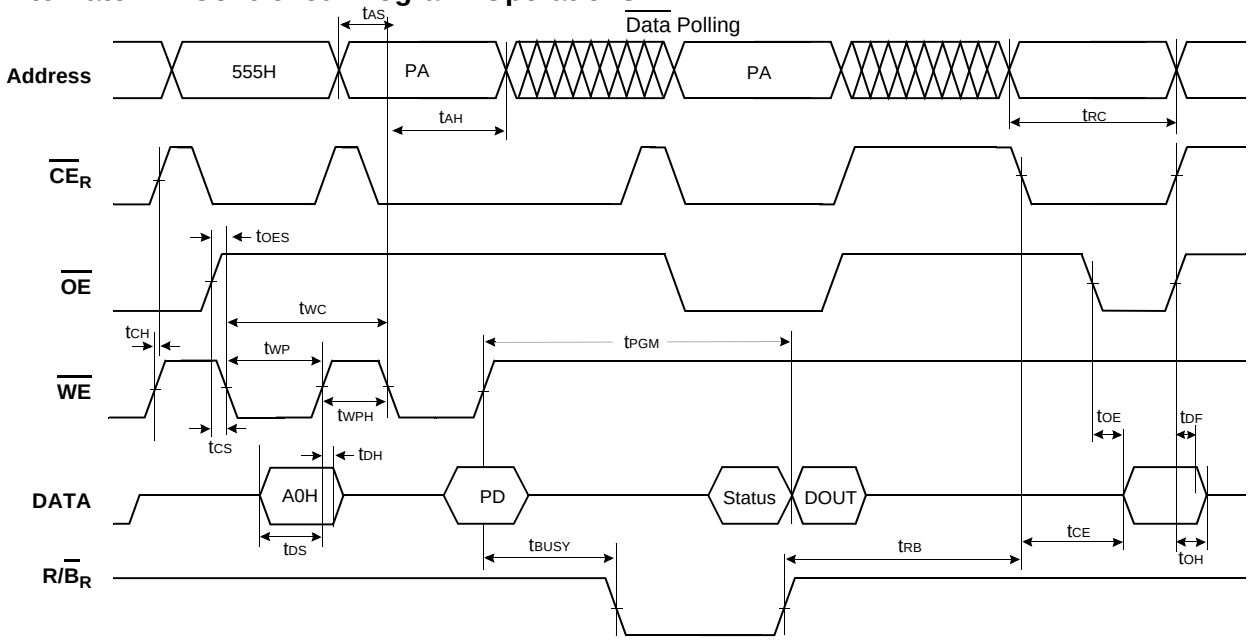
NOR Flash SWITCHING WAVEFORMS
Hardware Reset/Read Operations



Parameter	Symbol	70ns		Unit
		Min	Max	
Read Cycle Time	t_{RC}	70	-	ns
Address Access Time	t_{AA}	-	70	ns
Chip Enable Access Time	t_{CE}	-	70	ns
Output Hold Time from Address, $\overline{CE}_R$ or $\overline{OE}$	t_{OH}	0	-	ns
$\overline{RESET}$ Pulse Width	t_{RP}	500	-	ns
$\overline{RESET}$ High Time Before Read	t_{RH}	50	-	ns

NOR Flash SWITCHING WAVEFORMS

Alternate WE Controlled Program Operations

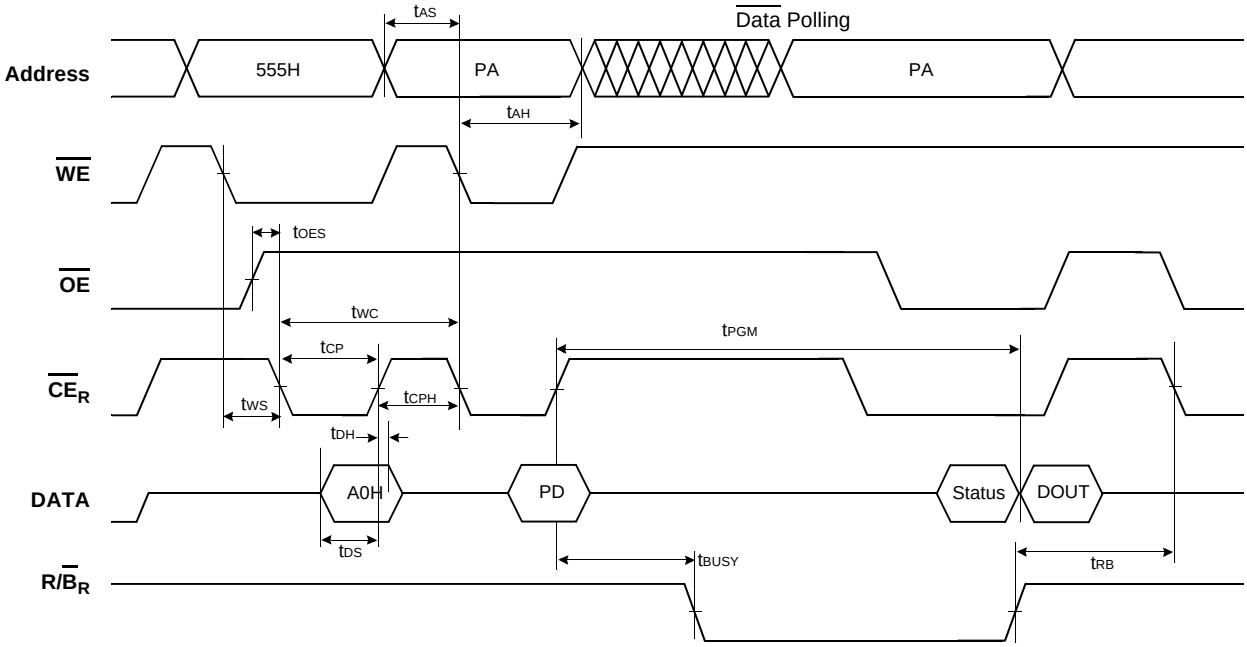


NOTES: 1. $\overline{DQ7}$ is the output of the complement of the data written to the device.
2. DOUT is the output of the data written to the device.
3. PA : Program Address, PD : Program Data
4. The illustration shows the last two cycles of the program command sequence.

Parameter		Symbol	70ns		Unit
			Min	Max	
Write Cycle Time		t_{WC}	70	-	ns
Address Setup Time		t_{AS}	0	-	ns
Address Hold Time		t_{AH}	45	-	ns
Data Setup Time		t_{DS}	35	-	ns
Data Hold Time		t_{DH}	0	-	ns
$\overline{CE}_R$ Setup Time		t_{CS}	0	-	ns
$\overline{CE}_R$ Hold Time		t_{CH}	0	-	ns
$\overline{OE}$ Setup Time		t_{OES}	0	-	ns
Write Pulse Width		t_{WP}	35	-	ns
Write Pulse Width High		t_{WPH}	25	-	ns
Programming Operation	Word	t_{PGM}	14(typ.)		us
	Byte		9(typ.)		us
Accelerated Programming Operation	Word	t_{ACCPGM}	9(typ.)		µs
	Byte		7(typ.)		µs
Read Cycle Time		t_{RC}	70	-	ns
Chip Enable Access Time		t_{CE}	-	70	ns
Output Enable Time		t_{OE}	-	25	ns
$\overline{CE}_R$ & $\overline{OE}$ Disable Time		t_{DF}	-	16	ns
Output Hold Time from Address, $\overline{CE}_R$ or $\overline{OE}$		t_{OH}	0	-	ns
Program/Erase Valide to R/$\overline{B}_R$ Delay		t_{BUSY}	90	-	ns
Recovery Time from R/$\overline{B}_R$		t_{RB}	0	-	ns

NOR Flash SWITCHING WAVEFORMS

Alternate $\overline{CE}_R$ Controlled Program Operations

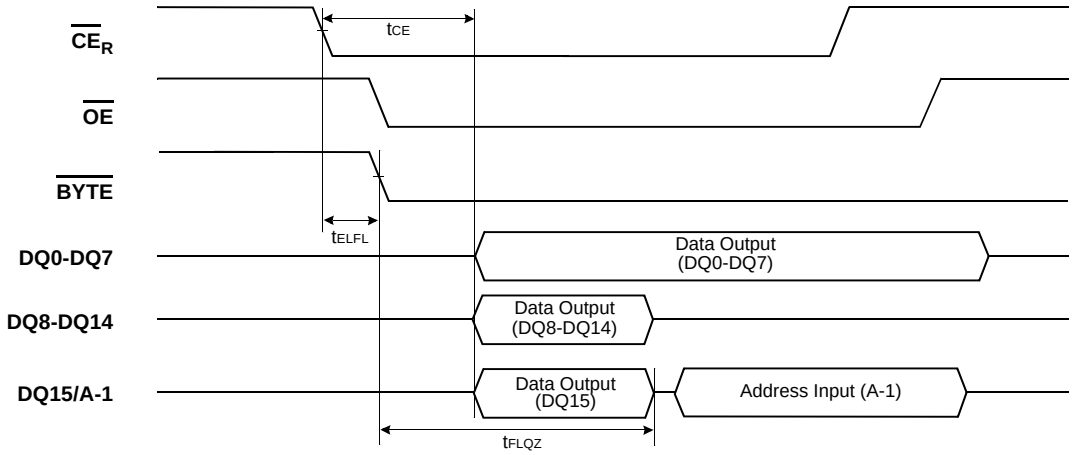


NOTES:
1. $\overline{DQ7}$ is the output of the complement of the data written to the device.
2. DOUT is the output of the data written to the device.
3. PA : Program Address, PD : Program Data
4. The illustration shows the last two cycles of the program command sequence.

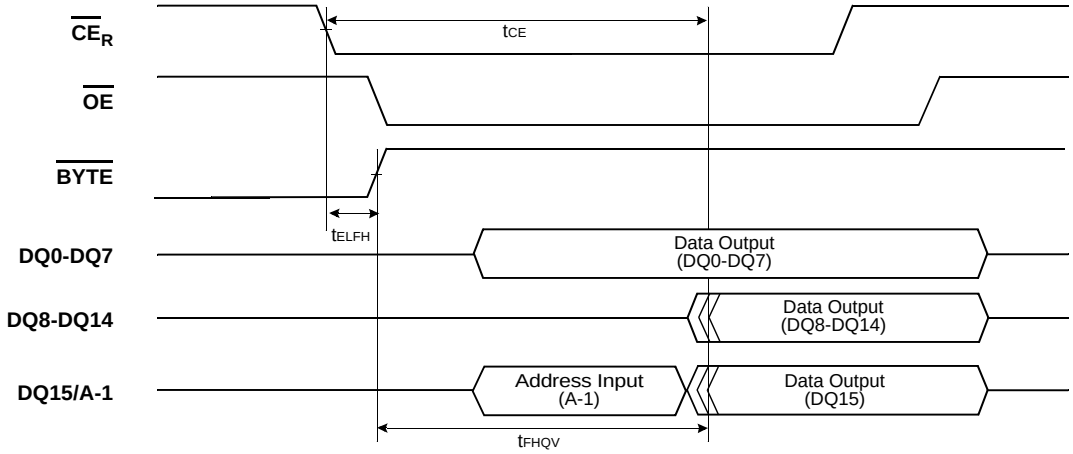
Parameter		Symbol	70ns		Unit
			Min	Max	
Write Cycle Time		tWC	70	-	ns
Address Setup Time		tAS	0	-	ns
Address Hold Time		tAH	45	-	ns
Data Setup Time		tDS	35	-	ns
Data Hold Time		tDH	0	-	ns
$\overline{OE}$ Setup Time		tOES	0	-	ns
$\overline{WE}$ Setup Time		tWS	0	-	ns
$\overline{WE}$ Hold Time		tWH	0	-	ns
$\overline{CE}_R$ Pulse Width		tCP	35	-	ns
$\overline{CE}_R$ Pulse Width High		tCPH	25	-	ns
Programming Operation	Word	tPGM	14(typ.)		µs
	Byte		9(typ.)		µs
Accelerated Programming Operation	Word	tACCPGM	9(typ.)		µs
	Byte		7(typ.)		µs
Program/Erase Valide to $R/\overline{B}_R$ Delay		tBUSY	90	-	ns
Recovery Time from $R/\overline{B}_R$		tRB	0	-	ns

NOR Flash SWITCHING WAVEFORMS

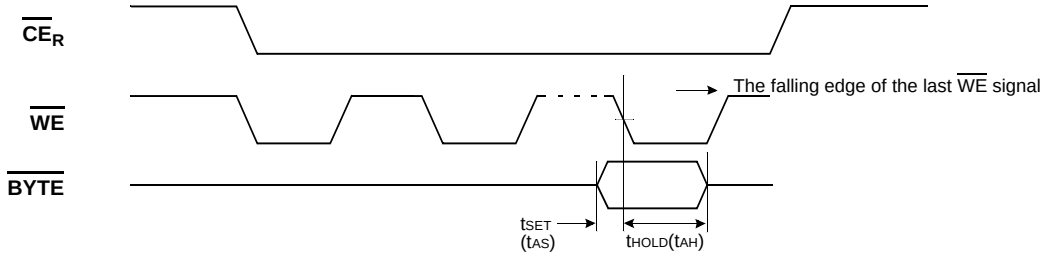
Word to Byte Timing Diagram for Read Operation



Byte to Word Timing Diagram for Read Operation



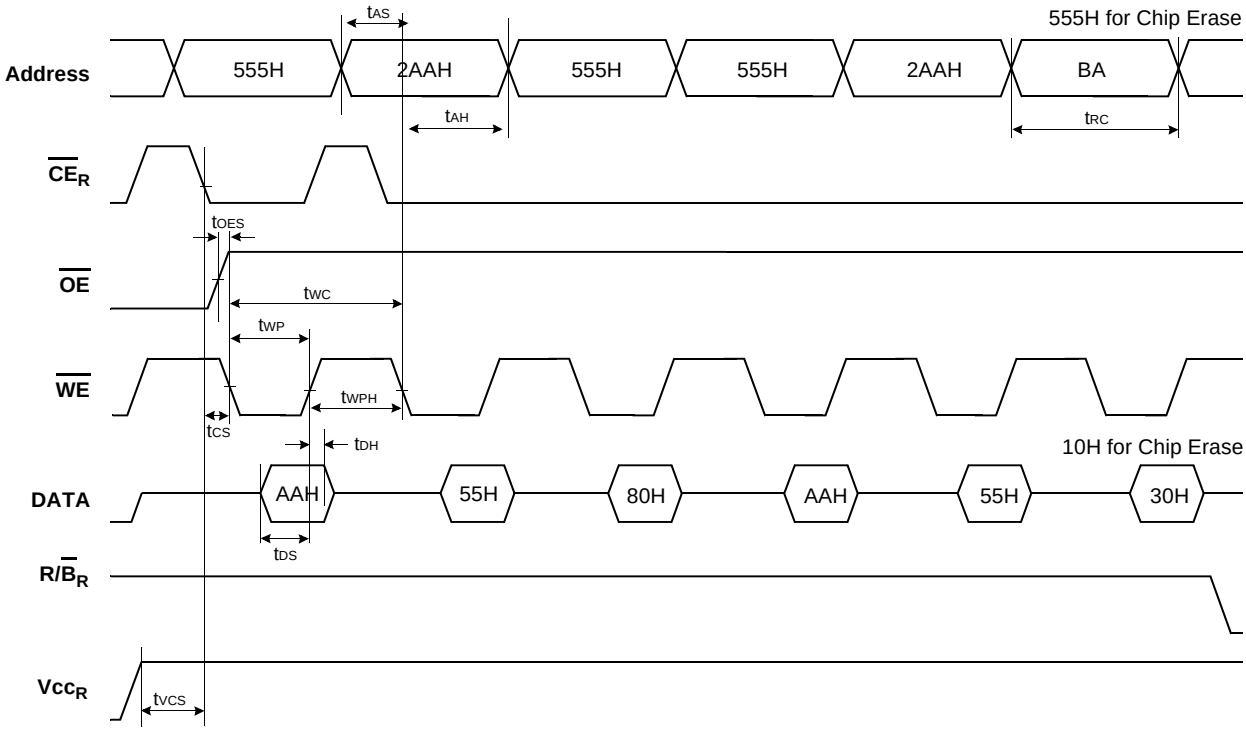
$\overline{BYTE}$ Timing Diagram for Write Operation



Parameter	Symbol	70ns		Unit
		Min	Max	
Chip Enable Access Time	tCE	-	70	ns
$\overline{CE_R}$ to $\overline{BYTE}$ Switching Low or High	tELFL/tELFH	-	5	ns
$\overline{BYTE}$ Switching Low to Output HIGH-Z	tFLQZ	-	25	ns
$\overline{BYTE}$ Switching High to Output Active	tFHQV	-	25	ns

NOR Flash SWITCHING WAVEFORMS

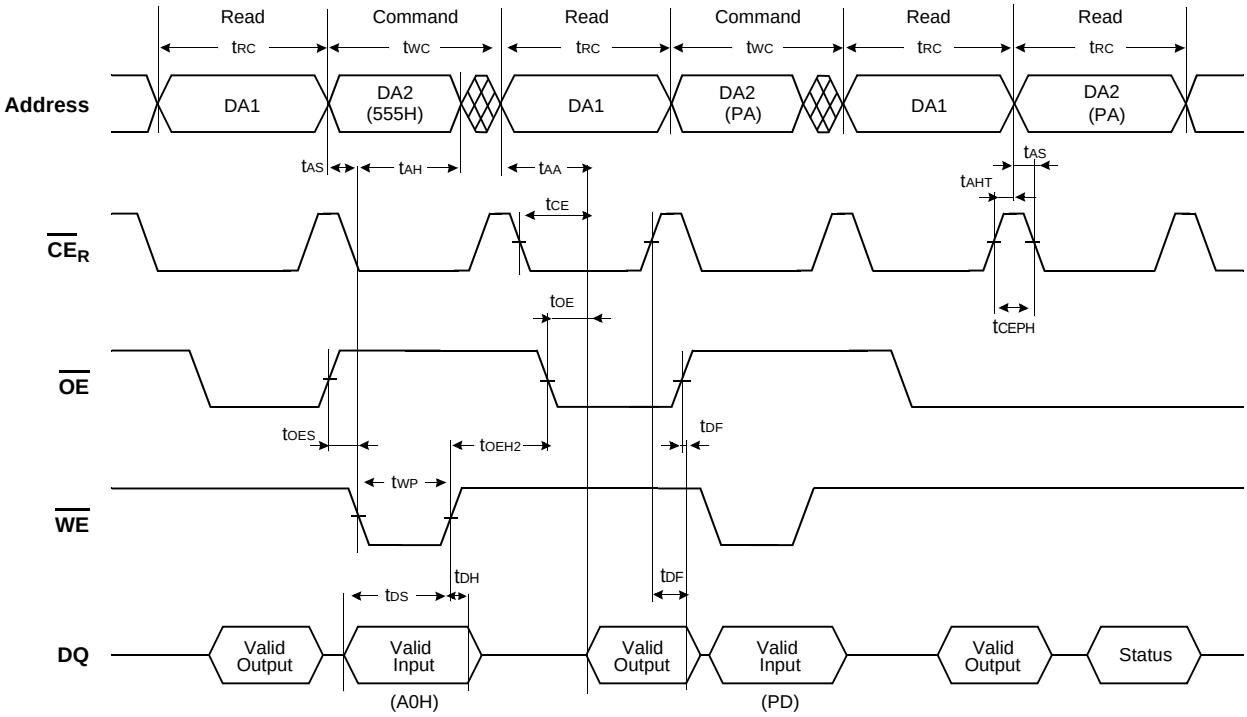
Chip/Block Erase Operations



NOTE: BA : Block Address

Parameter	Symbol	70ns		Unit
		Min	Max	
Write Cycle Time	t_{WC}	70	-	ns
Address Setup Time	t_{AS}	0	-	ns
Address Hold Time	t_{AH}	45	-	ns
Data Setup Time	t_{DS}	35	-	ns
Data Hold Time	t_{DH}	0	-	ns
$\overline{OE}$ Setup Time	t_{OES}	0	-	ns
$\overline{CE}_R$ Setup Time	t_{CS}	0	-	ns
Write Pulse Width	t_{WP}	35	-	ns
Write Pulse Width High	t_{WPH}	25	-	ns
Read Cycle Time	t_{RC}	70	-	ns
Vcc_R Set Up Time	t_{VCS}	50	-	µs

NOR Flash SWITCHING WAVEFORMS
Read While Write Operations

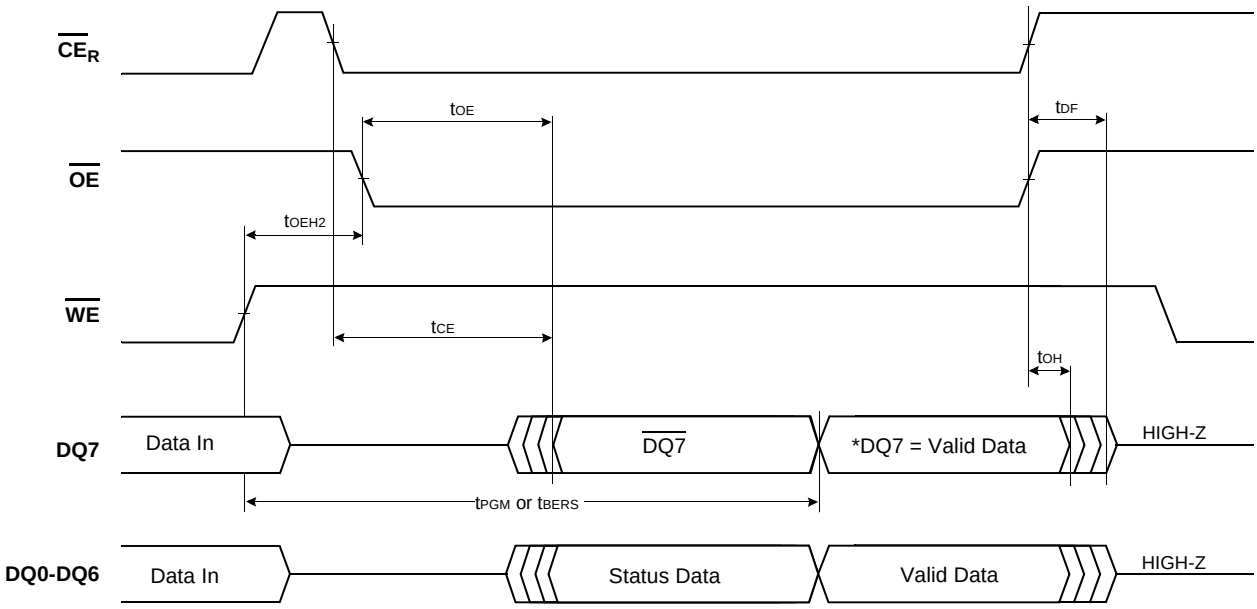


NOTE: This is an example in the program-case of the Read While Write function.
DA1 : Address of Bank1, DA2 : Address of Bank 2
PA = Program Address at one bank , RA = Read Address at the other bank, PD = Program Data In , RD = Read Data Out

Parameter	Symbol	70ns		Unit
		Min	Max	
Write Cycle Time	t_{WC}	70	-	ns
Write Pulse Width	t_{WP}	35	-	ns
Write Pulse Width High	t_{WPH}	25	-	ns
Address Setup Time	t_{AS}	0	-	ns
Address Hold Time	t_{AH}	45	-	ns
Data Setup Time	t_{DS}	35	-	ns
Data Hold Time	t_{DH}	0	-	ns
Read Cycle Time	t_{RC}	70	-	ns
Chip Enable Access Time	t_{CE}	-	70	ns
Address Access Time	t_{AA}	-	70	ns
Output Enable Access Time	t_{OE}	-	25	ns
$\overline{OE}$ Setup Time	t_{OES}	0	-	ns
$\overline{OE}$ Hold Time	t_{OEH2}	10	-	ns
$\overline{CE}_R$ & $\overline{OE}$ Disable Time	t_{DF}	-	16	ns
Address Hold Time	t_{AHT}	0	-	ns
$\overline{CE}_R$ High during toggle bit polling	t_{CEPH}	20	-	ns

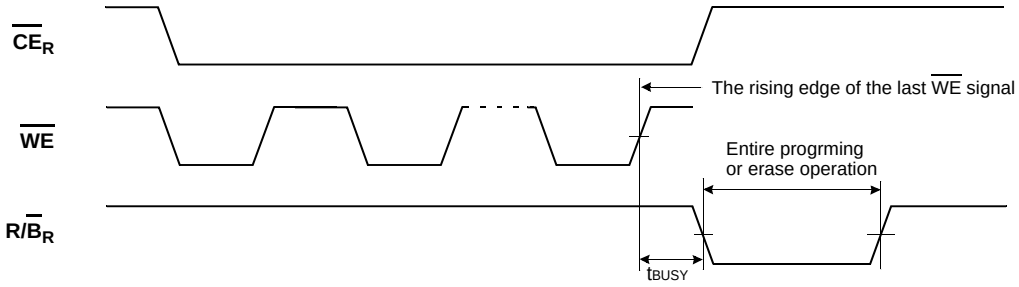
NOR Flash SWITCHING WAVEFORMS

Data Polling During Internal Routine Operation



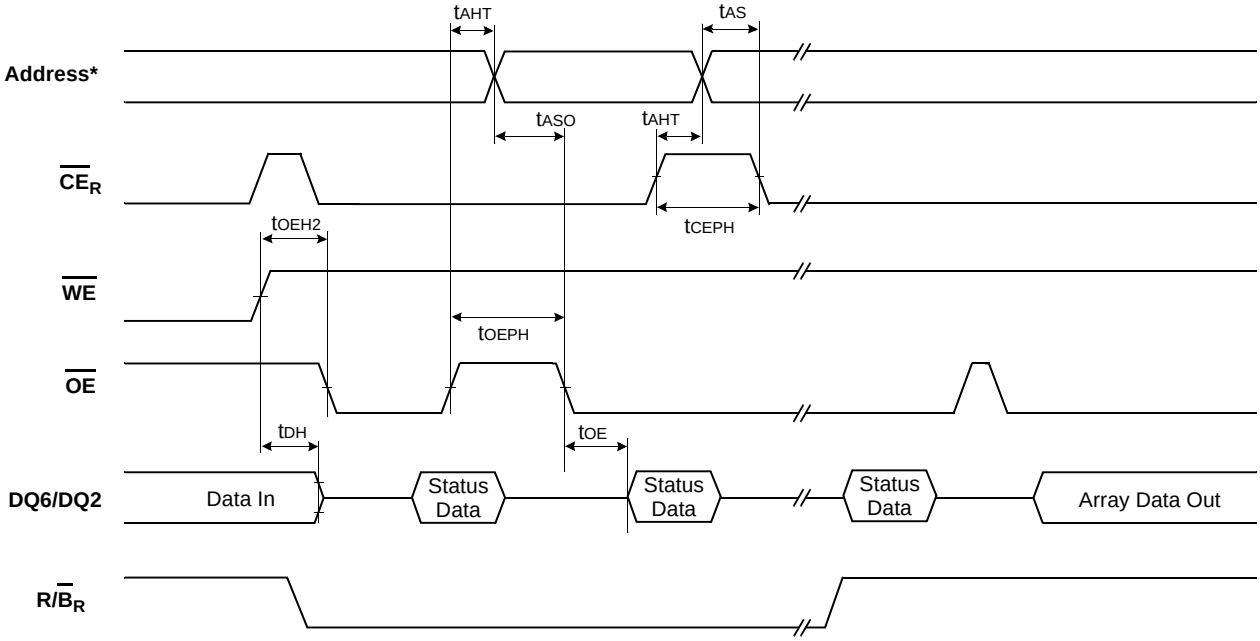
NOTE: *DQ7=Vaild Data (The device has completed the internal operation).

R/$\overline{B}_R$ Timing Diagram During Program/Erase Operation

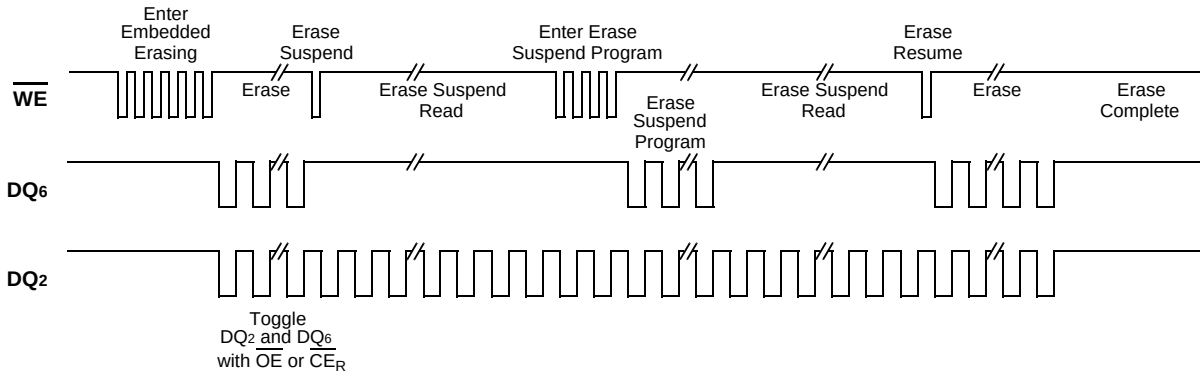


Parameter	Symbol	70ns		Unit
		Min	Max	
Program/Erase Valid to R/$\overline{B}_R$ Delay	t_{BUSY}	90	-	ns
Chip Enable Access Time	t_{CE}	-	70	ns
Output Enable Time	t_{OE}	-	25	ns
$\overline{CE}_R$ & $\overline{OE}$ Disable Time	t_{DF}	-	16	ns
Output Hold Time from Address, $\overline{CE}_R$ or $\overline{OE}$	t_{OH}	0	-	ns
$\overline{OE}$ Hold Time	t_{OEH2}	10	-	ns

NOR Flash SWITCHING WAVEFORMS
Toggle Bit During Internal Routine Operation



NOTE: Address for the write operation must include a bank address (A20~A21) where the data is written.

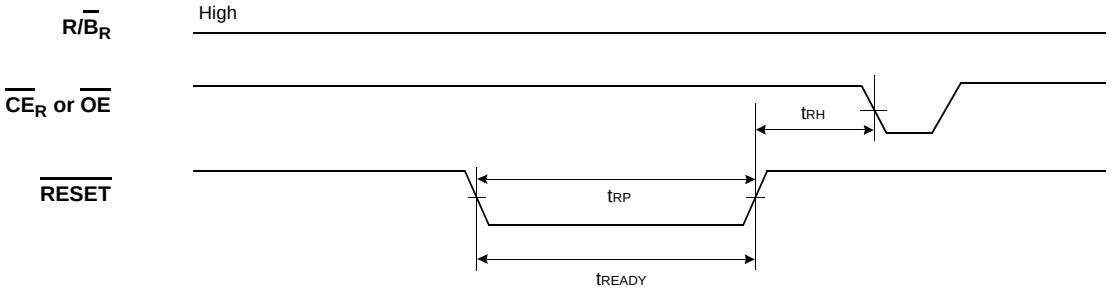


NOTE: DQ2 is read from the erase-suspended block.

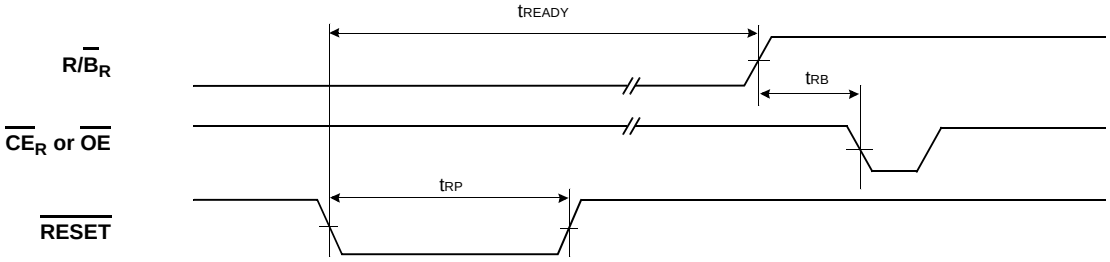
Parameter	Symbol	70ns		Unit
		Min	Max	
Output Enable Access Time	tOE	-	25	ns
OE Hold Time	tOEH2	10	-	ns
Address Hold Time	tAHT	0	-	ns
Address Setup	tASO	55	-	ns
Address Setup Time	tAS	0	-	ns
Data Hold Time	tDH	0	-	ns
CER High during toggle bit polling	tCEPH	20	-	ns
OE High during toggle bit polling	tOEPH	20	-	ns

NOR Flash SWITCHING WAVEFORMS

RESET Timing Diagram

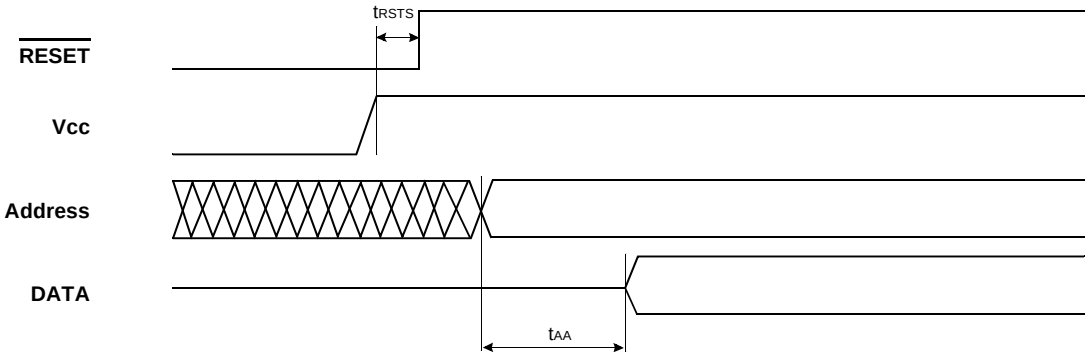


Reset Timings NOT during Internal Routine



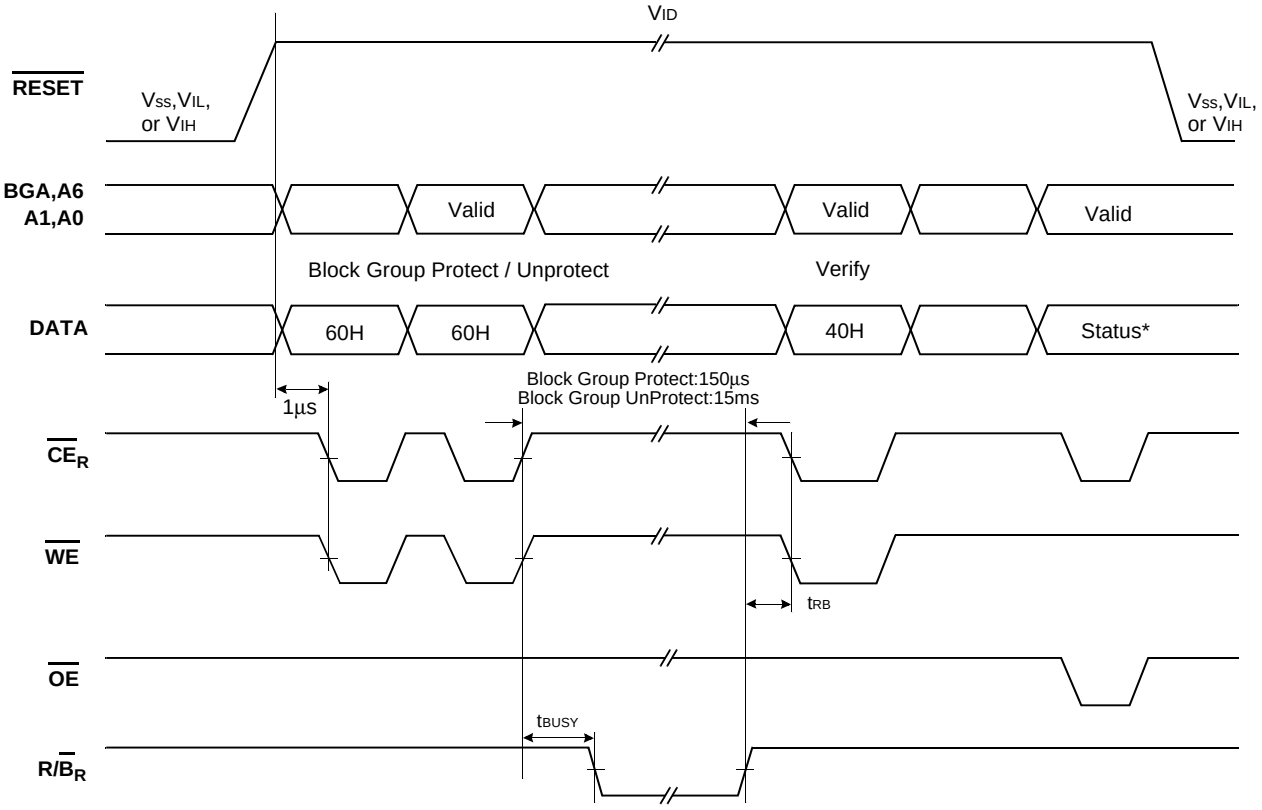
Reset Timings during Internal Routine

Power-up and RESET Timing Diagram



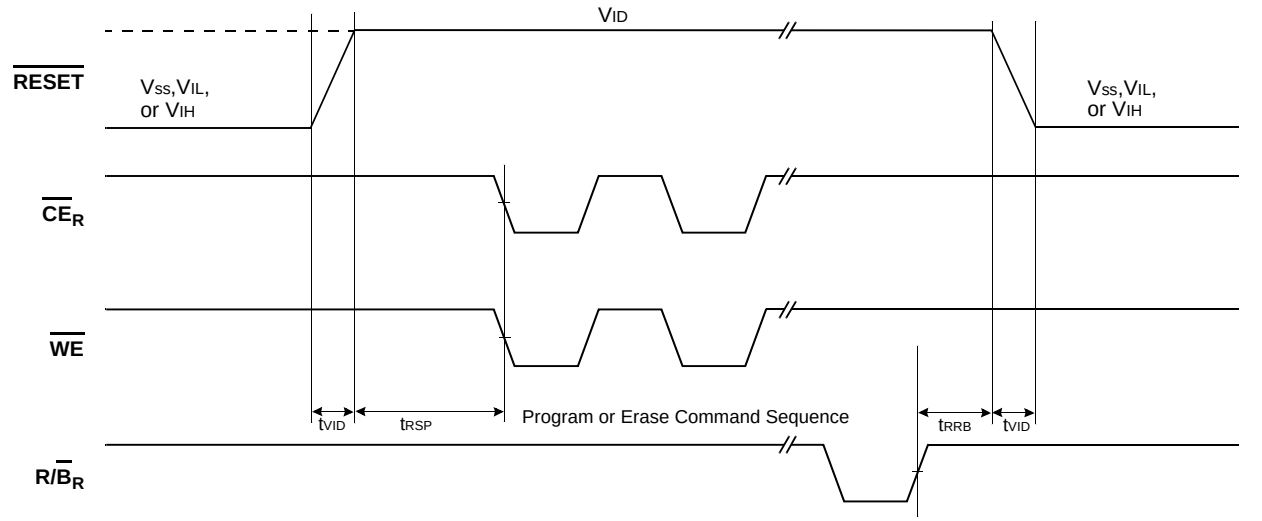
Parameter	Symbol	70ns		Unit
		Min	Max	
RESET Pulse Width	tRP	500	-	ns
RESET Low to Valid Data (During Internal Routine)	tREADY	-	20	µs
RESET Low to Valid Data (Not during Internal Routine)	tREADY	-	500	ns
RESET High Time Before Read	tRH	50	-	ns
R/B_R Recovery Time	tRB	0	-	ns
RESET High to Address Valid	tRSTW	200	-	ns
RESET Low Set-up Time	tRSTS	500	-	ns

NOR Flash SWITCHING WAVEFORMS
Block Group Protect & Unprotect Operations



NOTES: Block Group Protect (A6=V_{IL} , A1=V_{IH} , A0=V_{IL}) , Status=01H
Block Group Unprotect (A6=V_{IH} , A1=V_{IH}, A0=V_{IL}) , Status=00H
BGA = Block Group Address (A12 ~ A21)

Temporary Block Group Unprotect



NAND Flash Program/Erase Characteristics (Vcc_F=2.7~3.1V, T_A=-25 to 85°C)

Parameter		Symbol	Min	Typ	Max	Unit
Program Time		t_{PROG}	-	200	500	µs
Number of Partial Program Cycles in the Same Page	Main Array	Nop	-	-	1	cycles
	Spare Array		-	-	1	
Block Erase Time		t_{BERS}	-	2	3	ms

NAND Flash AC Timing Characteristics for Command/Address/Data Input

(Vcc_F=2.7~3.1V, T_A=-25 to 85°C)

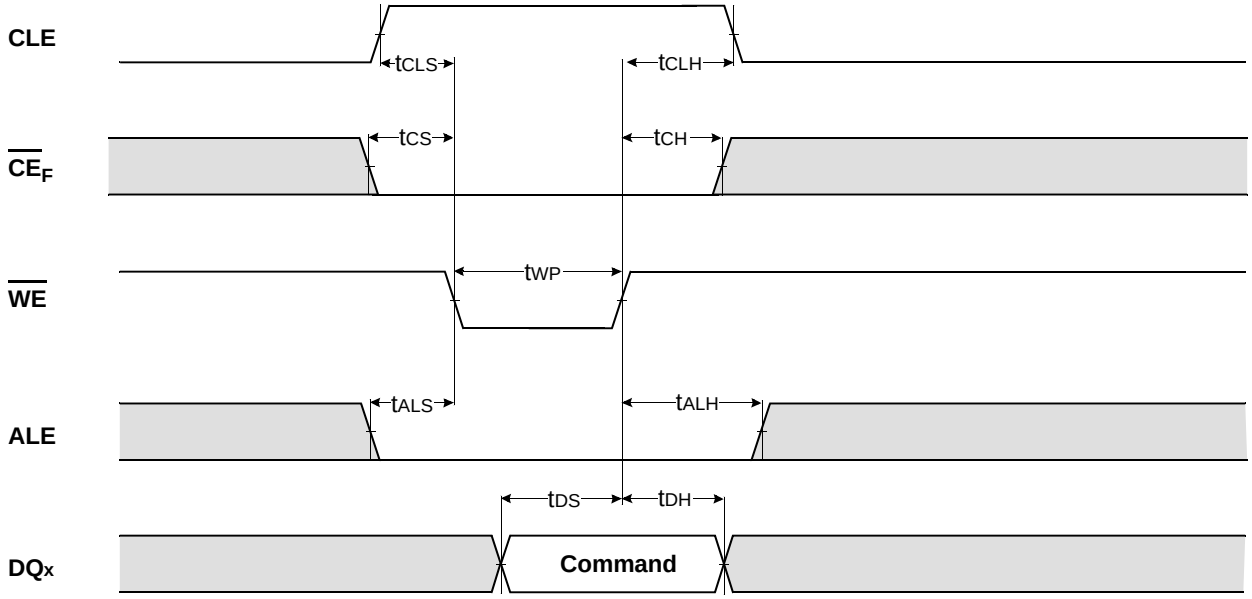
Parameter	Symbol	Min	Max	Unit
CLE Set-up Time	t_{CLS}	0	-	ns
CLE Hold Time	t_{CLH}	10	-	ns
$\overline{CE}_F$ Setup Time	t_{CS}	0	-	ns
$\overline{CE}_F$ Hold Time	t_{CH}	10	-	ns
$\overline{WE}$ Pulse Width	t_{WP}	25	-	ns
ALE Setup Time	t_{ALS}	0	-	ns
ALE Hold Time	t_{ALH}	10	-	ns
Data Setup Time	t_{DS}	20	-	ns
Data Hold Time	t_{DH}	10	-	ns
Write Cycle Time	t_{WC}	45	-	ns
$\overline{WE}$ High Hold Time	t_{WH}	15	-	ns

NAND Flash AC Characteristics for Operation (Vcc_F=2.7~3.1V, T_A=-25 to 85°C)

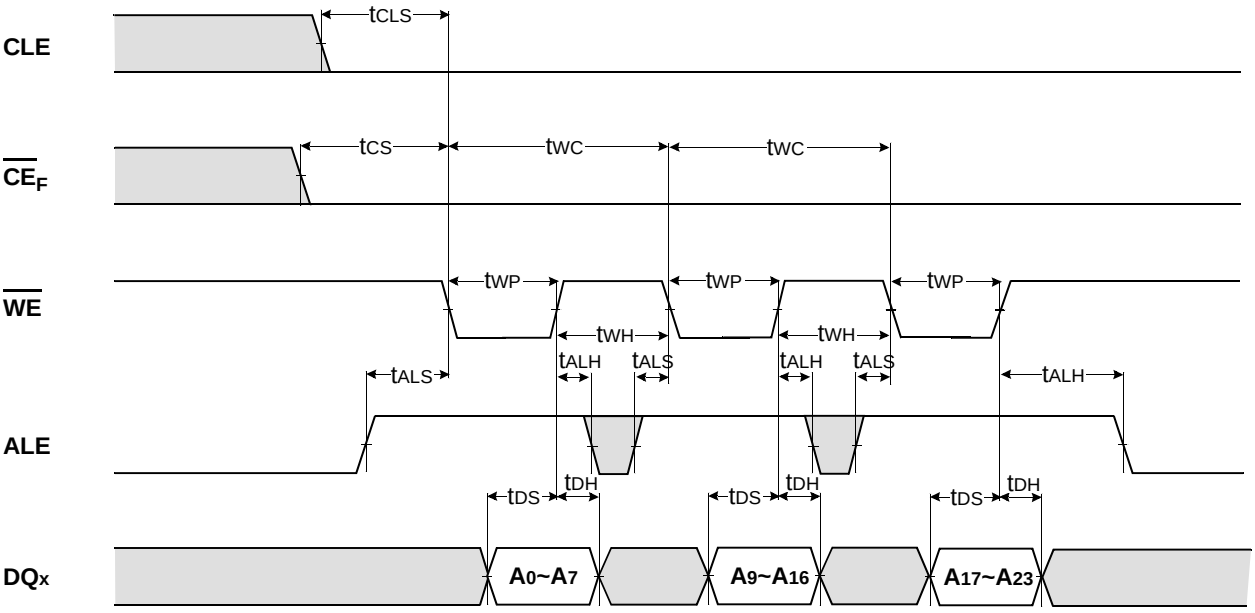
Parameter	Symbol	Min	Max	Unit
Data Transfer from Cell to Register	t_R	-	10	µs
ALE to $\overline{RE}$ Delay	t_{AR}	10	-	ns
$\overline{CE}_F$ Access Time	t_{CEA}	-	45	ns
Ready to $\overline{RE}$ Low	t_{RR}	20	-	ns
$\overline{RE}$ Pulse Width	t_{RP}	25	-	ns
$\overline{WE}$ High to Busy	t_{WB}	-	100	ns
Read Cycle Time	t_{RC}	50	-	ns
$\overline{RE}$ Access Time	t_{REA}	-	30	ns
$\overline{RE}$ High to Output Hi-Z	t_{RHZ}	-	30	ns
$\overline{CE}_F$ High to Output Hi-Z	t_{CHZ}	-	20	ns
$\overline{RE}$ or $\overline{CE}_F$ High to Output Hold	t_{OH}	15	-	ns
$\overline{RE}$ High Hold Time	t_{REH}	15	-	ns
Output Hi-Z to $\overline{RE}$ Low	t_{IR}	0	-	ns
$\overline{WE}$ High to $\overline{RE}$ Low	t_{WHR}	60	-	ns
Device Resetting Time(Read/Program/Erase)	t_{RST}	-	5/10/500(1)	µs

NOTE: 1. If reset command(FFh) is written at Ready state, the device goes into Busy for maximum 5us

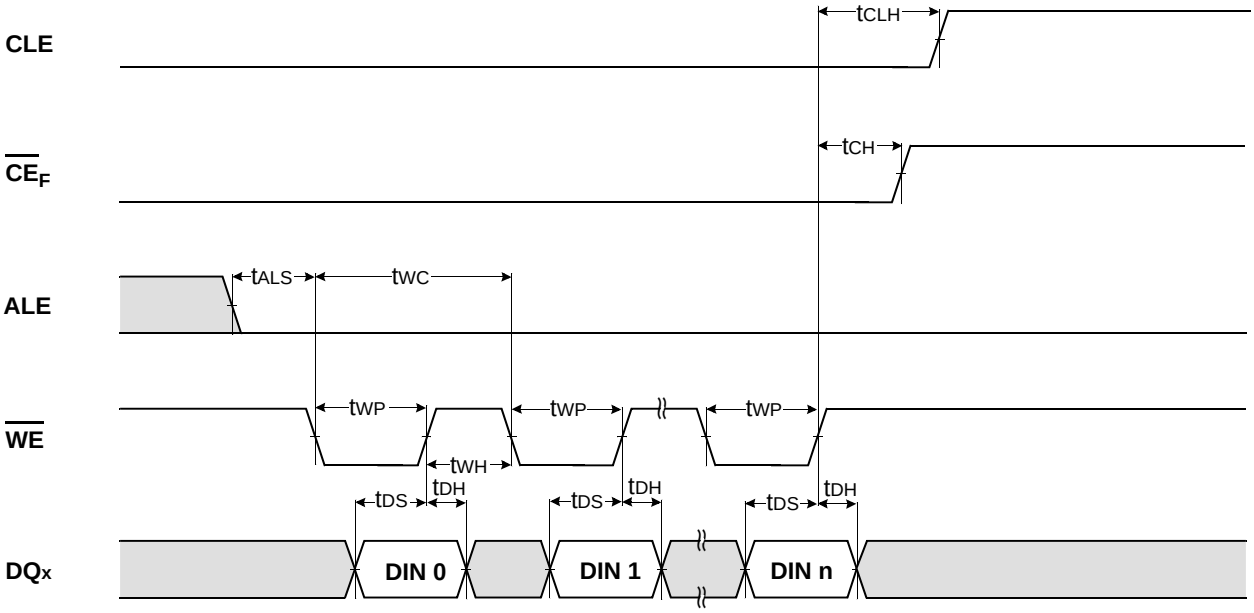
NAND Flash Command Latch Cycle



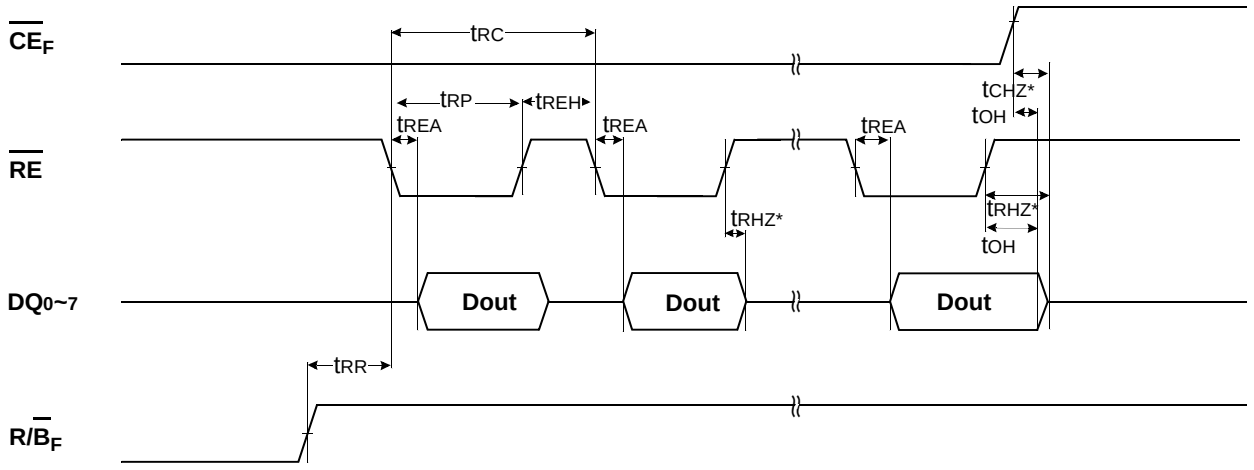
NAND Flash Address Latch Cycle



NAND Flash Input Data Latch Cycle

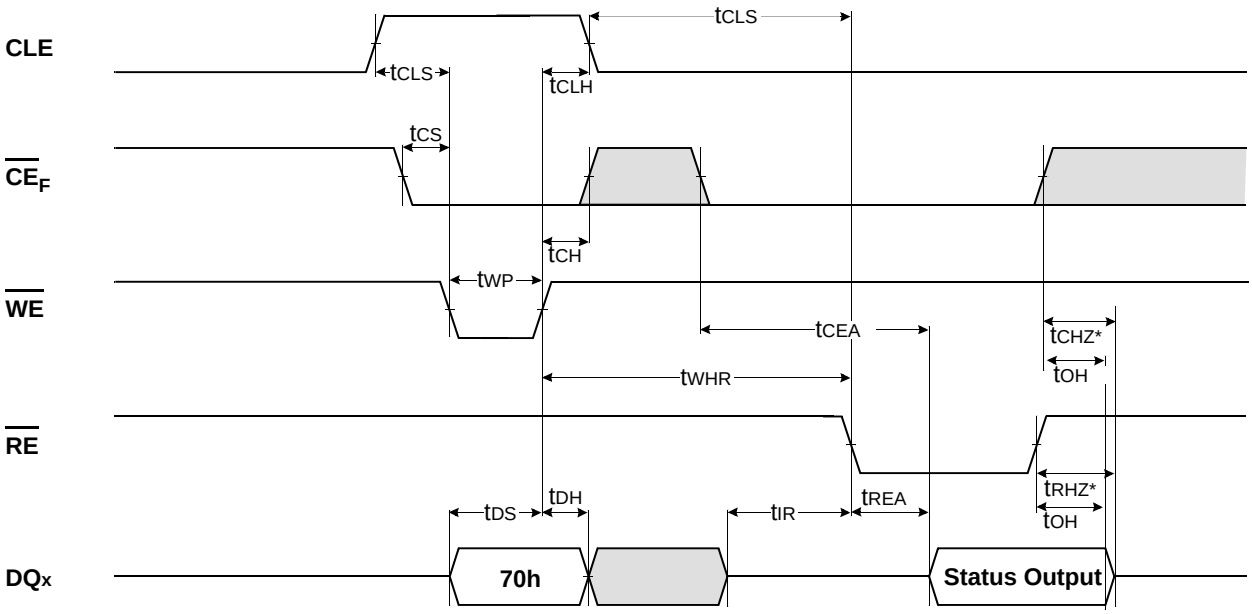


NAND Flash Sequential Out Cycle after Read(CLE=L, $\overline{WE}$=H, ALE=L)

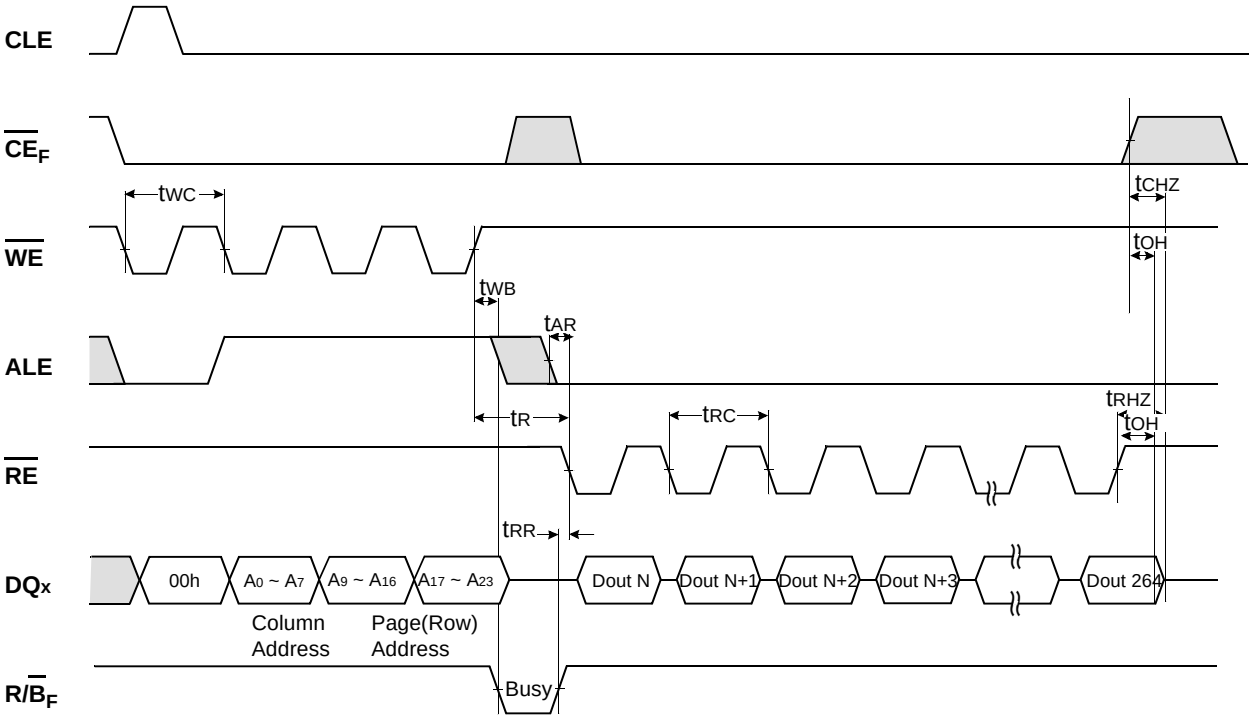


NOTES: Transition is measured ±200mV from steady state voltage with load.
This parameter is sampled and not 100% tested.

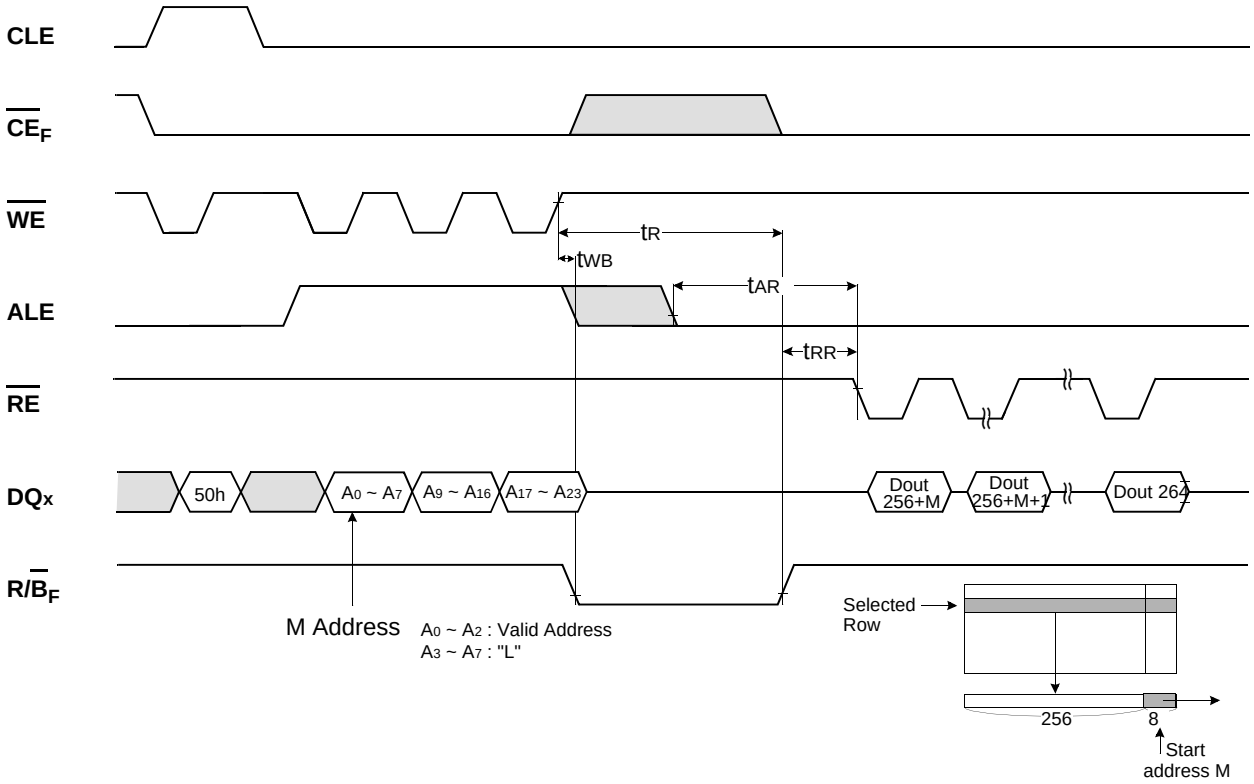
NAND Flash Status Read Cycle



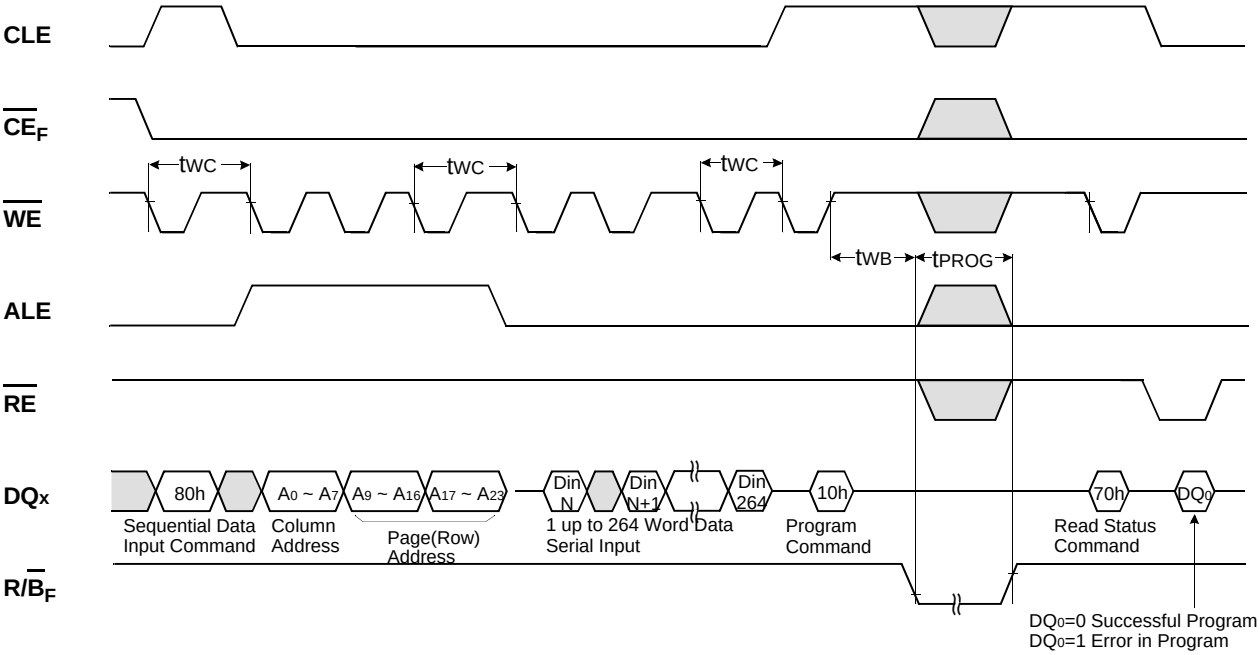
NAND FLASH READ1 OPERATION(READ ONE PAGE)



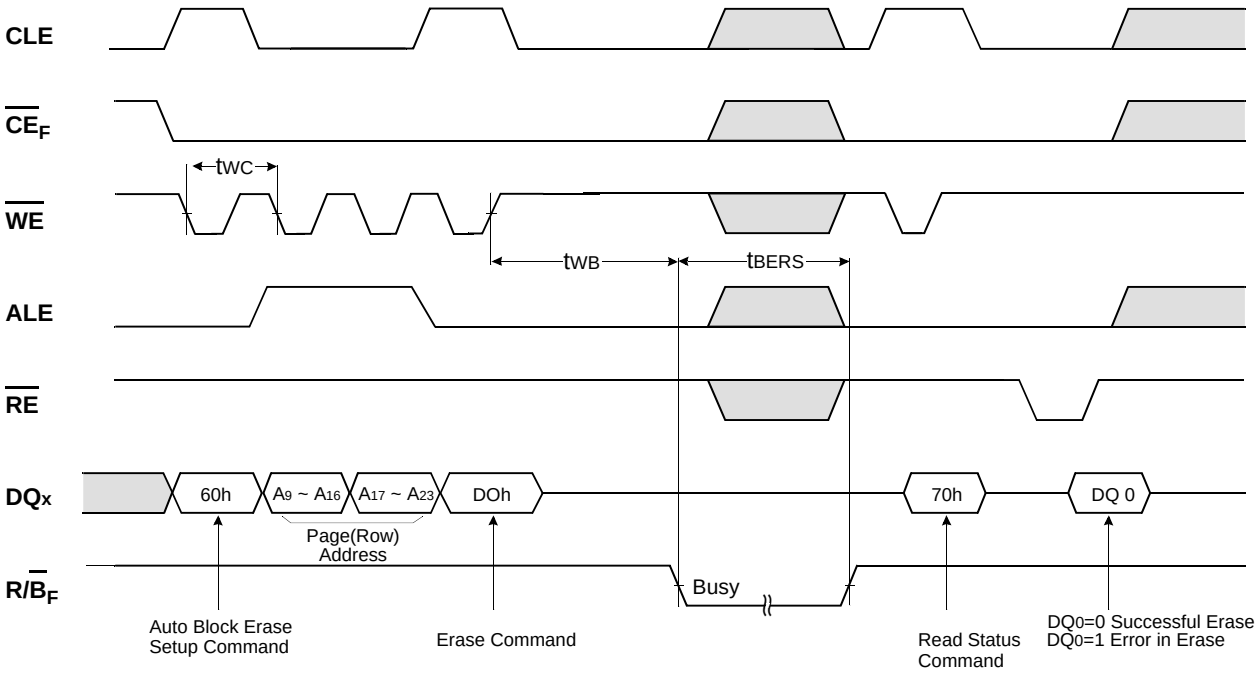
NAND FLASH READ2 OPERATION(READ ONE PAGE)



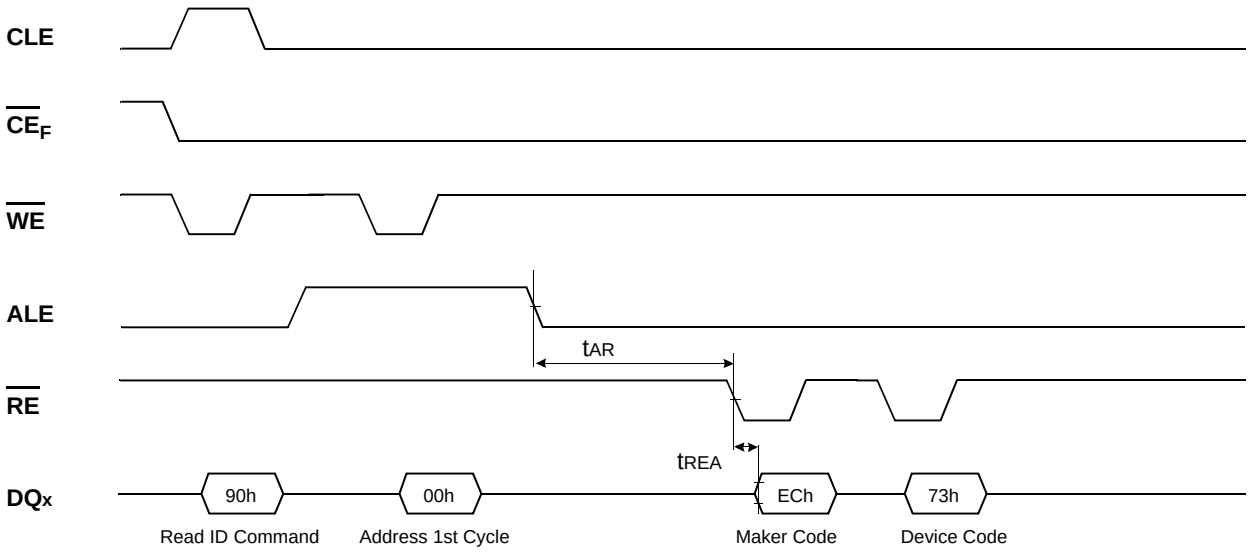
NAND FLASH PAGE PROGRAM OPERATION



NAND FLASH BLOCK ERASE OPERATION(ERASE ONE BLOCK)



NAND FLASH MANUFACTURE & DEVICE ID READ OPERATION



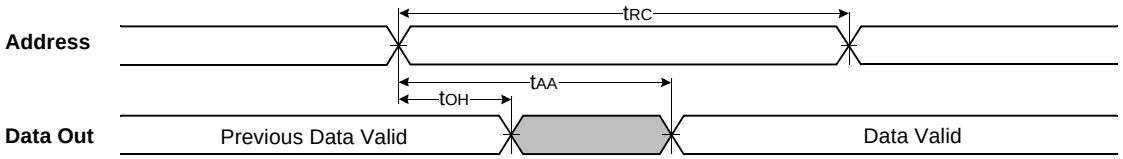
U*t*RAM AC CHARACTERISTICS(Vcc_U=2.7~3.1V, T_A=-25 to 85°C)

Parameter List		Symbol	Speed Bins		Units
			70ns		
			Min	Max	
Read	Read Cycle Time	t_{RC}	70	-	ns
	Address Access Time	t_{AA}	-	70	ns
	Chip Select to Output	t_{CO}	-	70	ns
	Output Enable to Valid Output	t_{OE}	-	35	ns
	$\overline{UB}$, $\overline{LB}$ Access Time	t_{BA}	-	70	ns
	Chip Select to Low-Z Output	t_{LZ}	10	-	ns
	$\overline{UB}$, $\overline{LB}$ Enable to Low-Z Output	t_{BLZ}	10	-	ns
	Output Enable to Low-Z Output	t_{OLZ}	5	-	ns
	Chip Disable to High-Z Output	t_{HZ}	0	25	ns
	$\overline{UB}$, $\overline{LB}$ Disable to High-Z Output	t_{BHZ}	0	25	ns
	Output Disable to High-Z Output	t_{OHZ}	0	25	ns
	Output Hold from Address Change	t_{OH}	5	-	ns
	Page Cycle	t_{PC}	-	30	ns
	Page Access Time	t_{PA}	-	25	ns
Write	Write Cycle Time	t_{WC}	70	-	ns
	Chip Select to End of Write	t_{CW}	60	-	ns
	Address Set-up Time	t_{AS}	0	-	ns
	Address Valid to End of Write	t_{AW}	60	-	ns
	$\overline{UB}$, $\overline{LB}$ Valid to End of Write	t_{BW}	60	-	ns
	Write Pulse Width	t_{WP}	55[1)]	-	ns
	Write Recovery Time	t_{WR}	0	-	ns
	Write to Output High-Z	t_{WHZ}	0	25	ns
	Data to Write Time Overlap	t_{DW}	30	-	ns
	Data Hold from Write Time	t_{DH}	0	-	ns
	End Write to Output Low-Z	t_{OW}	5	-	ns

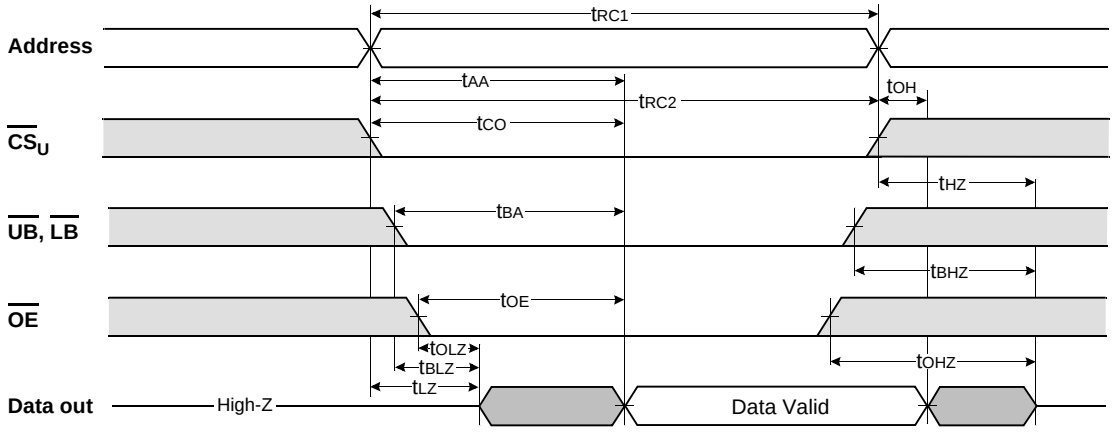
1. t_{WP}(min)=70ns for continuous write operation over 50 times.(Only in case of $\overline{WE}$ controlled write operation)

U*t*RAM TIMING DIAGRAMS

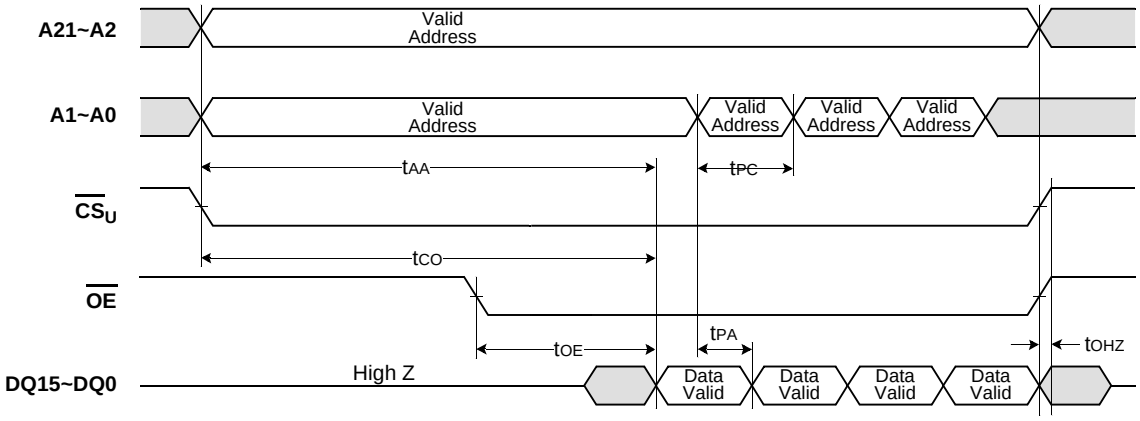
TIMING WAVEFORM OF READ CYCLE(1)(Address Controlled, $\overline{CS_U}$=$\overline{OE}$=V_{IL}, $\overline{ZZ}$=$\overline{WE}$=V_{IH}, $\overline{UB}$ or/and $\overline{LB}$=V_{IL})



TIMING WAVEFORM OF READ CYCLE(2)($\overline{ZZ}$=$\overline{WE}$=V_{IH})



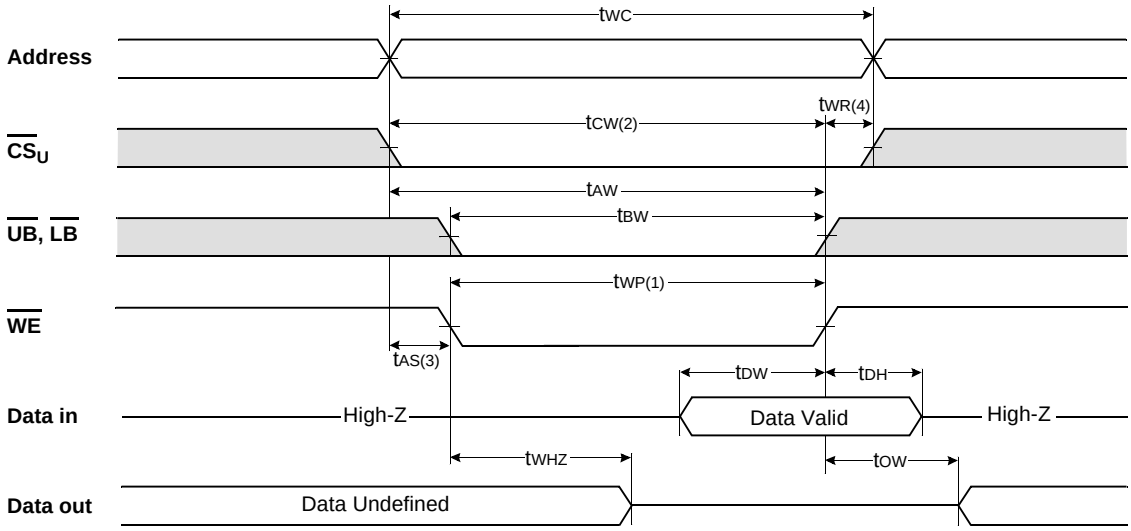
TIMING WAVEFORM OF PAGE CYCLE(READ ONLY)



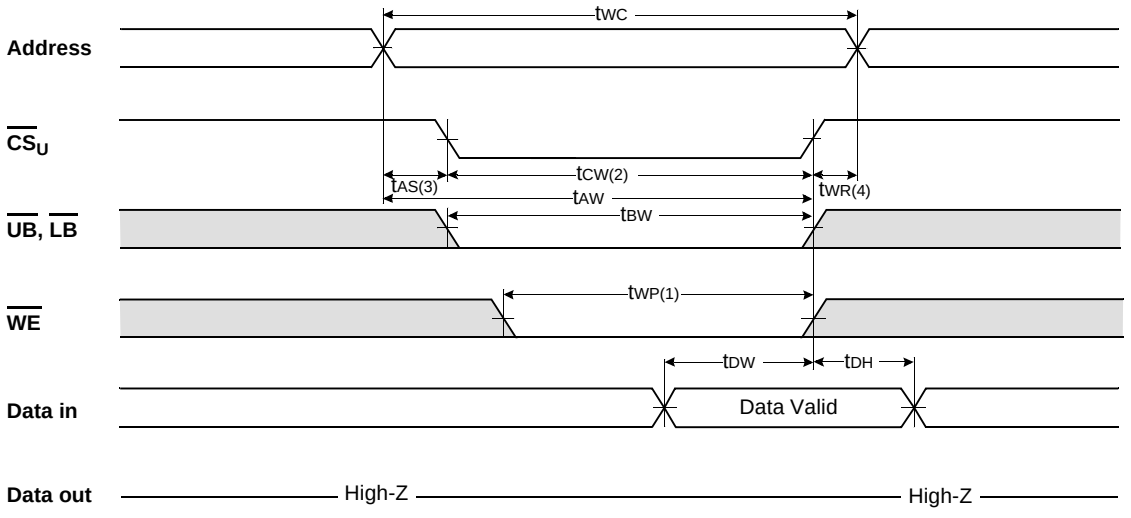
(READ CYCLE)

1. t_{HZ} and t_{OHZ} are defined as the time at which the outputs achieve the open circuit conditions and are not referenced to output voltage levels.
2. At any given temperature and voltage condition, t_{HZ}(Max.) is less than t_{LZ}(Min.) both for a given device and from device to device interconnection.
3. The minimum read cycle(t_{RC}) is determined by longer one of the t_{RC1} and t_{RC2}.
4. t_{OE}(max) is met only when $\overline{OE}$ becomes enabled after t_{AA}(max).
5. If invalid address signals shorter than min. t_{RC} are continuously repeated for over 4us, the device needs a normal read timing(t_{RC}) or needs to sustain standby state for min. t_{RC} at least once in every 4us.

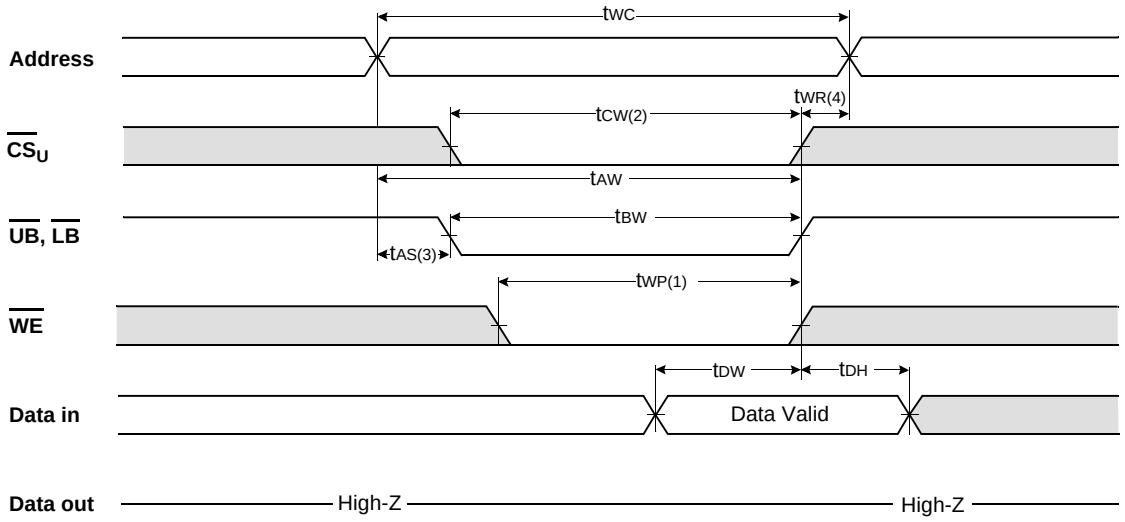
TIMING WAVEFORM OF WRITE CYCLE(1)($\overline{WE}$ Controlled, $\overline{ZZ}$=V_{IH})



TIMING WAVEFORM OF WRITE CYCLE(2)($\overline{CS_U}$ Controlled, $\overline{ZZ}$=V_{IH})



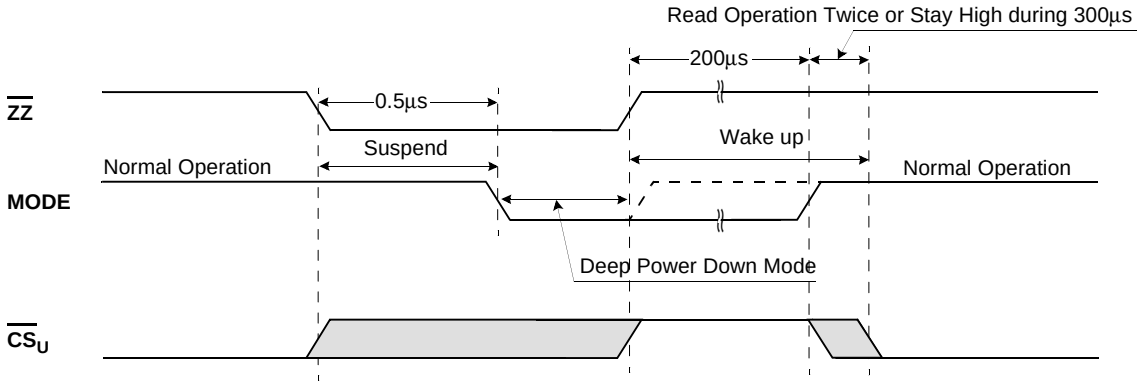
TIMING WAVEFORM OF WRITE CYCLE(3)($\overline{UB}$, $\overline{LB}$ Controlled, $\overline{ZZ}$=V_{IH})



(WRITE CYCLE)

1. A write occurs during the overlap(t_{WP}) of low $\overline{CS}_U$ and low $\overline{WE}$. A write begins when $\overline{CS}_U$ goes low and $\overline{WE}$ goes low with asserting $\overline{UB}$ or $\overline{LB}$ for single byte operation or simultaneously asserting $\overline{UB}$ and $\overline{LB}$ for double byte operation. A write ends at the earliest transition when $\overline{CS}_U$ goes high and $\overline{WE}$ goes high. The t_{WP} is measured from the beginning of write to the end of write.
2. t_{CW} is measured from the $\overline{CS}_U$ going low to the end of write.
3. t_{AS} is measured from the address valid to the beginning of write.
4. t_{WR} is measured from the end of write to the address change. t_{WR} applied in case a write ends as $\overline{CS}_U$ or $\overline{WE}$ going high.

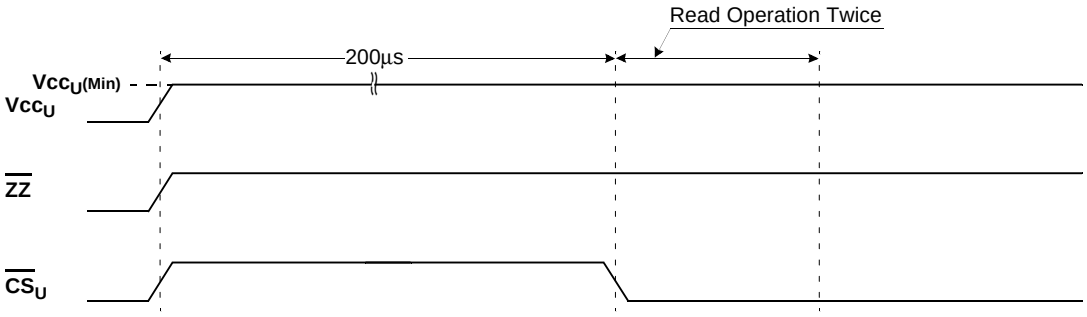
TIMING WAVEFORM OF DEEP POWER DOWN MODE



(DEEP POWER DOWN MODE)

1. When you toggle $\overline{ZZ}$ pin low, the device gets into the Deep Power Down mode after 0.5µs suspend period.
2. To return to normal operation, the device needs Wake Up period.
3. Wake Up sequence is just the same as Power up sequences.

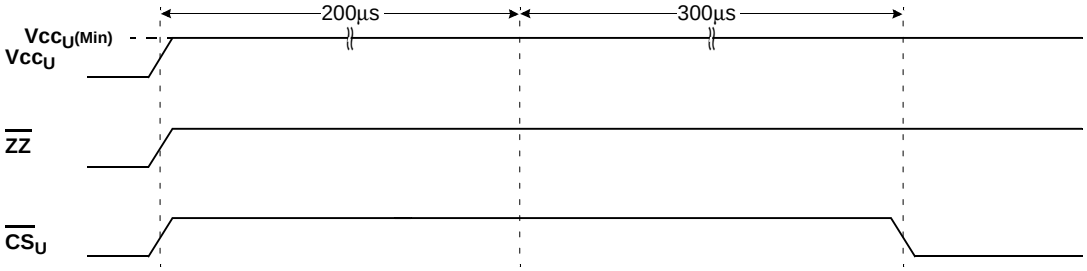
TIMING WAVEFORM OF POWER UP(1)



(POWER UP(1))

1. After Vcc_U reaches Vcc_U(Min.) following power application, wait 200µs with $\overline{CS}_U$ high and then toggle $\overline{CS}_U$ low and commit Read Operation at least twice. Then you get into the normal operation.
2. Read operation should be executed by toggling $\overline{CS}_U$ pin low.
3. The read operation must satisfy the specified tRC.
4. $\overline{ZZ}$ pin should be kept high during whole power up sequence.

TIMING WAVEFORM OF POWER UP(2)(No Dummy Cycle)



(POWER UP(2))

1. After Vcc_U reaches Vcc_U(Min.) following power application, wait 200µs and wait another 300µs with $\overline{CS}_U$ high if you don't want to commit dummy read cycle. After total 500µs wait, toggle $\overline{CS}_U$ low, then you get into the normal mode.
2. $\overline{ZZ}$ pin should be kept high during whole power up sequence.

PACKAGE DIMENSION

80-Ball Tape Ball Grid Array Package (measured in millimeters)