

2N5529 2N5530 2N5533 2N5534

NPN SILICON POWER TRANSISTORS

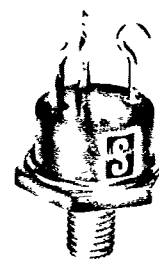
RADIATION RESISTANT

10 AMPERES**FEATURES**

HIGH POWER
 RADIATION EXPOSURE LEVEL TO 5×10^{14} nvt
 TOTAL NEUTRON FLUX GREATER THAN 10 KEV

APPLICATIONS

POWER AMPLIFIER
 RADIATION ENVIRONMENTS
 ULTRA HIGH FREQUENCY

**TO-61**

*All leads isolated from case

ABSOLUTE MAXIMUM RATINGS

		2N5529 2N5530*	2N5533 2N5534*
V_{CB0}	COLLECTOR-BASE VOLTAGE	60 V	90 V
V_{CE0}	COLLECTOR-EMITTER VOLTAGE	40 V	75 V
V_{EB0}	EMITTER-BASE VOLTAGE	3 V	3 V
I_C	CONTINUOUS COLLECTOR CURRENT	10 A	10 A
I_B	CONTINUOUS BASE CURRENT	4 A	4 A
T_J	OPERATING JUNCTION TEMPERATURE	— -65°C to $+200^{\circ}\text{C}$ —	
T_{stg}	STORAGE TEMPERATURE	— -65°C to $+200^{\circ}\text{C}$ —	
$R_{\theta JC}$	THERMAL RESISTANCE, JUNCTION TO CASE	5°C/W	
P_D	POWER DISSIPATION (25°C)	35 W	

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T-33.11

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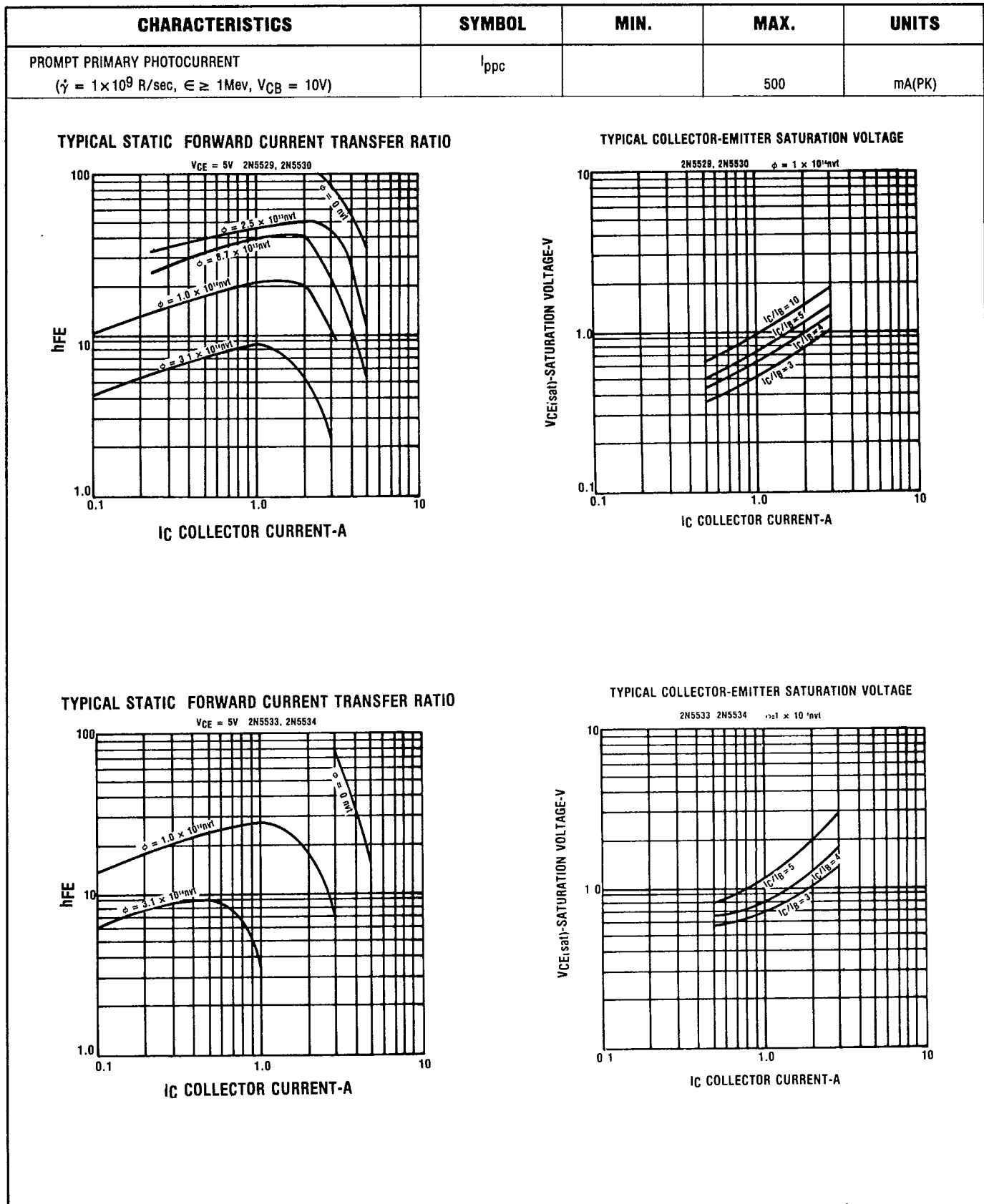
SOLITRON DEVICES INC

ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ UNLESS OTHERWISE NOTED)

CHARACTERISTICS	SYMBOL	MIN.	MAX.	UNITS
COLLECTOR-EMITTER SUSTAINING VOLTAGE ⁽¹⁾ ($I_C = 50\text{ mA}$) 2N5529, 2N5530 2N5533, 2N5534 ($I_C = 50\text{ mA}$, NOTE 2) 2N5529, 2N5530 2N5533, 2N5534	$V_{CE(sus)}$	40 75 40 75		V V V V
COLLECTOR-CUTOFF CURRENT ($V_{CE} = 30\text{V}$, $V_{BE} = 0$, $T_C = 100^\circ\text{C}$)	I_{CEX}		1.0	mA
COLLECTOR-CUTOFF CURRENT ($V_{CB} = \text{RATED}$) ($V_{CB} = \text{RATED}$, NOTE 2)	I_{CBO}		1.0 1.0	mA mA
COLLECTOR-CUTOFF CURRENT ($V_{CB} = 30\text{V}$) ($V_{CB} = 30\text{V}$, NOTE 2)	I_{CBO}		0.1 1.0	mA mA
COLLECTOR-CUTOFF CURRENT ($V_{CE} = \text{RATED}$)	I_{CEO}		50	mA
EMITTER CUTOFF CURRENT ($V_{EB} = 3.0\text{V}$) ($V_{EB} = 3.0\text{V}$, NOTE 2)	I_{EBO}		1.0 1.0	mA mA
EMITTER FLOATING POTENTIAL ($V_{CB} = \text{RATED}$, $I_E = 0$)	V_{EBF}		1.0	V
DC CURRENT GAIN ⁽¹⁾ ($V_{CE} 5.0\text{V}$, $I_C = 0.5\text{A}$) 2N5529, 2N5530 ($V_{CE} 5.0\text{V}$, $I_C = 0.5\text{A}$) 2N5533, 2N5534 ($V_{CE} 5.0\text{V}$, $I_C = 3.0\text{A}$) 2N5529, 2N5530 ($V_{CE} 5.0\text{V}$, $I_C = 3.0\text{A}$) 2N5533, 2N5534 ($V_{CE} 5.0\text{V}$, $I_C = 5.0\text{A}$) 2N5529, 2N5530 ($V_{CE} 5.0\text{V}$, $I_C = 5.0\text{A}$) 2N5533, 2N5534 ($V_{CE} 2.0\text{V}$, $I_C = 10\text{A}$) ($V_{CE} 5.0\text{V}$, $I_C = 3.0\text{A}$ NOTE 2) 2N5529, 2N5530 ($V_{CE} 5.0\text{V}$, $I_C = 3.0\text{A}$ NOTE 2) 2N5533, 2N5534	h_{FE}	40 25 40 30 25 20 2.5 15 7.0	300 300 200 150	
COLLECTOR-EMITTER SATURATION VOLTAGE ⁽¹⁾ ($I_C = 3.0\text{A}$, $I_B = 0.3\text{A}$) 2N5529, 2N5530 ($I_C = 0.5\text{A}$, $I_B = 4.0\text{A}$) 2N5533, 2N5534 ($I_C = 10\text{A}$, $I_B = 4.0\text{A}$) ($I_C = 3.0\text{A}$, $I_B = 0.3\text{A}$, NOTE 2) 2N5529, 2N5530 ($I_C = 3.0\text{A}$, $I_B = 0.5\text{A}$, NOTE 2) 2N5533, 2N5534	$V_{CE(sat)}$		1.25 1.25 2.0 2.0 3.0	V V V V V
BASE-EMITTER SATURATION VOLTAGE ⁽¹⁾ ($I_C = 3.0\text{A}$, $I_B = 0.3\text{A}$) 2N5529, 2N5530 ($I_C = 3.0\text{A}$, $I_B = 0.5\text{A}$) 2N5533, 2N5534	$V_{BE(sat)}$		1.5 1.5	V V
BASE-EMITTER VOLTAGE ($V_{CE} = 5.0\text{V}$, $I_C = 3.0\text{A}$) ($V_{CE} = 5.0\text{V}$, $I_C = 5.0\text{A}$)	V_{BE}		1.5 3.0	V V
MAGNITUDE OF SMALL SIGNAL GAIN ($V_{CE} = 28\text{V}$, $I_C = 0.5\text{A}$, $f = 25\text{ MHz}$)	$[h_{fe}]$	8.0		
SMALL SIGNAL GAIN ($V_{CE} = 5.0\text{V}$, $I_C = 3.0\text{A}$, $f = 1.0\text{ KHz}$) 2N5529, 2N5530 2N5533, 2N5534	h_{fe}	20 15		
OUTPUT CAPACITANCE ($V_{CB} = 30\text{V}$, $f = 1.0\text{ MHz}$)	C_{obo}		75	pF

Note 1: Pulsed 300 μsec , 1.8% Duty CycleNote 2: After exposure 1×10^{14} nvt, FLUX $\geq 10\text{ KEV}$

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RADIATION RESISTANT NPN SILICON POWER TRANSISTORS**2N5529 2N5530 2N5533 2N5534****ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ UNLESS OTHERWISE NOTED)**

RADIATION RESISTANT NPN SILICON POWER TRANSISTORS

SOLITRON DEVICES INC

T 33-11

2N5529 2N5530 2N5533 2N5534**SAFE OPERATING AREA (SOAR)
INFORMATION**

The Safe Operating Area (SOAR) principle is a method of specifying the exact transistor to use in an amplifier, switching or DC application. SOAR defines the region which encloses all of the points representing simultaneous values of the collector current and the collector-to-emitter voltage which a transistor can safely handle under specified conditions for base current, time, junction temperature and average power dissipation. With transistors specified under the Solitron SOAR technique, secondary breakdown is virtually eliminated.

The suggested test circuits are shown for each type of SOAR operation. Any other thermally stable circuit may also be used as long as the SOAR conditions and maximum ratings are observed.

CONTINUOUS DC OPERATION**SOAR VALUES**

TYPE NUMBER	V1 V	V2 V
2N5530	30	60
2N5534	65	90

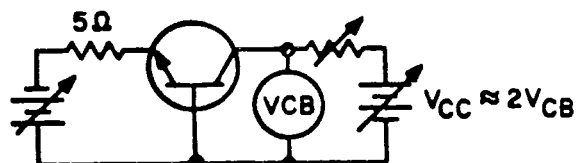
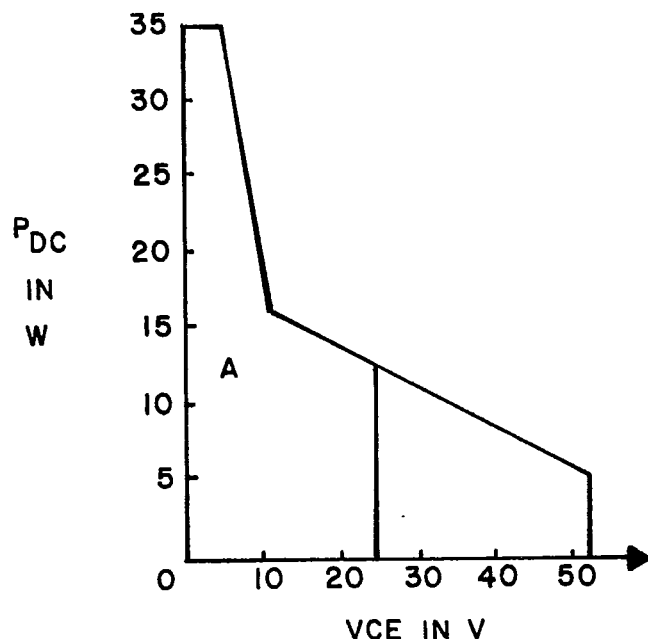
Conditions: 1. $T_J = T_{CASE} + \Theta_{J-C} P_{DC} \leq 200^\circ\text{C}$

2. $P_{DC} \leq P_{DC \text{ max rating for specified transistor type}}$

3. $P_{DC} \leq P_{DC} = f(V_{CE}) \text{ Area A}$

4. $V_{CE} \leq 24\text{V (2N5529, 2N5530)}$

52V (2N5533, 2N5534)



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PULSED OPERATION

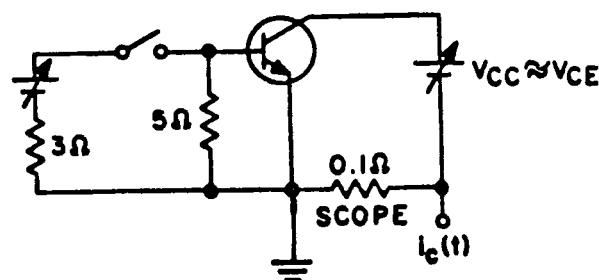
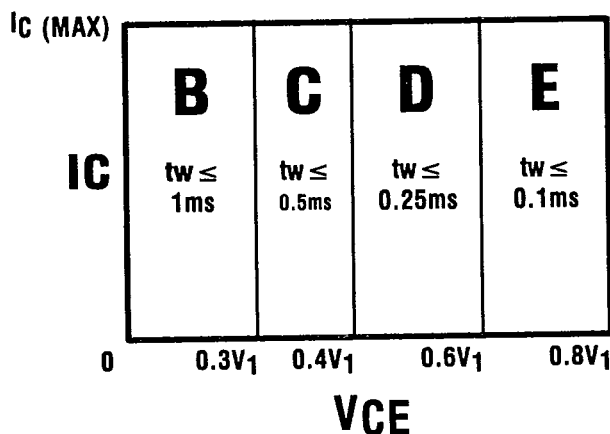
Conditions:

$$1. T_J = T_{CASE} + \Theta_{J-C} P_{avg} \leq 200^\circ\text{C}$$

$$2. P_{avg} = \frac{1}{2\text{ms}} \int_0^{2\text{ms}} i_C v_{CE} dt \leq \text{the allowed DC}$$

power dissipation for a V_{CE} equal to the highest v_{CE} applied to the transistor

3. Operation in the active region should be limited to a maximum pulse width of $t_w = 1\text{ ms}$ for Area B, $t_w = 0.5\text{ ms}$ for Area C, $t_w = 0.25\text{ ms}$ for Area D, and $t_w = 0.10\text{ ms}$ for Area E. $t_r \leq 20\text{ }\mu\text{s}$ and $t_f \leq 20\text{ }\mu\text{s}$ for Areas B-E.



RESISTIVE AND CLAMPED INDUCTIVE SWITCHING

(Switching from saturation to cutoff)

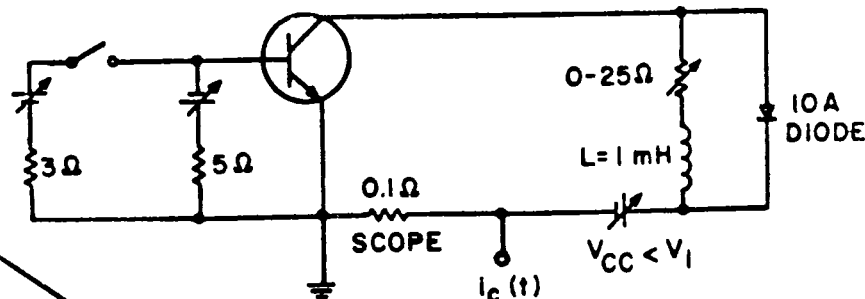
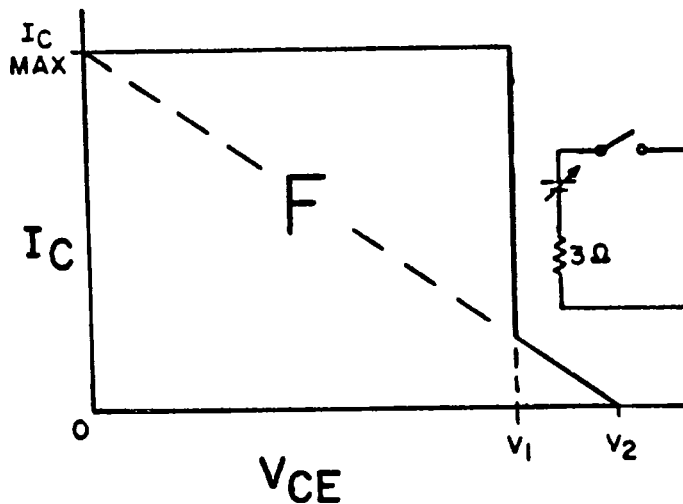
Conditions:

$$1. T_J = T_C + \Theta_{J-C} P_{avg} \leq 200^\circ\text{C}$$

$$2. P_{avg} = \frac{1}{2\text{ms}} \int_0^{2\text{ms}} i_C v_{CE} dt \leq \text{PDC max.}$$

3. For the resistive loadline, $L = 0$ and $V_{CC} = V_2$

4. $t_r \leq 2\text{ }\mu\text{s}$, $t_f \leq 2\text{ }\mu\text{s}$ in Area F



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UNCLAMPED SWITCHING

(Switching from saturation to cutoff)

Conditions:

1. $T_J = T_C + \Theta_{J-C} P_{avg} \leq 200^\circ\text{C}$

2. $P_{avg} = \frac{1}{2\text{ms}} \int_0^{2\text{ms}} i_C v_{CE} dt \leq P_{DC \text{ max.}}$

3. $I_C \text{ peak} \leq I_C \text{ max rating for specified transistor type}$

4. $\frac{1}{2} I_C^2 \leq 80 \mu\text{Ws}$

