CY8C20142

CapSense*LITE* - 4 Configurable IOs

Features

- Four configurable IOs supporting
  - CapSense buttons
  - LED drive
  - Interrupt outputs
  - WAKE on interrupt input
  - User defined Input/output
- 2.4V to 5.25V operating voltage
- Industrial temperature range: –40°C to +85°C
- I^2C slave interface for configuration
- Reduce BOM cost
  - Internal oscillator - no external oscillators or crystal
  - Free development tool - no external tuning components
- Low Operating Current
  - Active current: continuous sensor scan - 1mA
  - Active current: no sensor scan - 30uA
  - Sleep current: no scan, continuous sleep - 2.6uA
- Available in 8-pin SOIC package

Overview

The CapSense Lite controller allows the control of four configurable IOs that are configurable as capacitive sensing buttons or as GPIOs for driving LEDs or interrupt signals based on various button conditions. The GPIOs also configurable for waking up the device from sleep based on an interrupt input.

The user has the ability to configure buttons, outputs, and parameters, through specific commands sent to the I^2C port. The IOs have the flexibility to be mapped to capacitive buttons and/or as standard GPIO functions such as interrupt output or input, LED drive and digital mapping of input to output using simple logical operations. This enables easy PCB trace routing and reduces the PCB size and stack up. Capsense Lite products are designed for easy integration into complex products.

Architecture

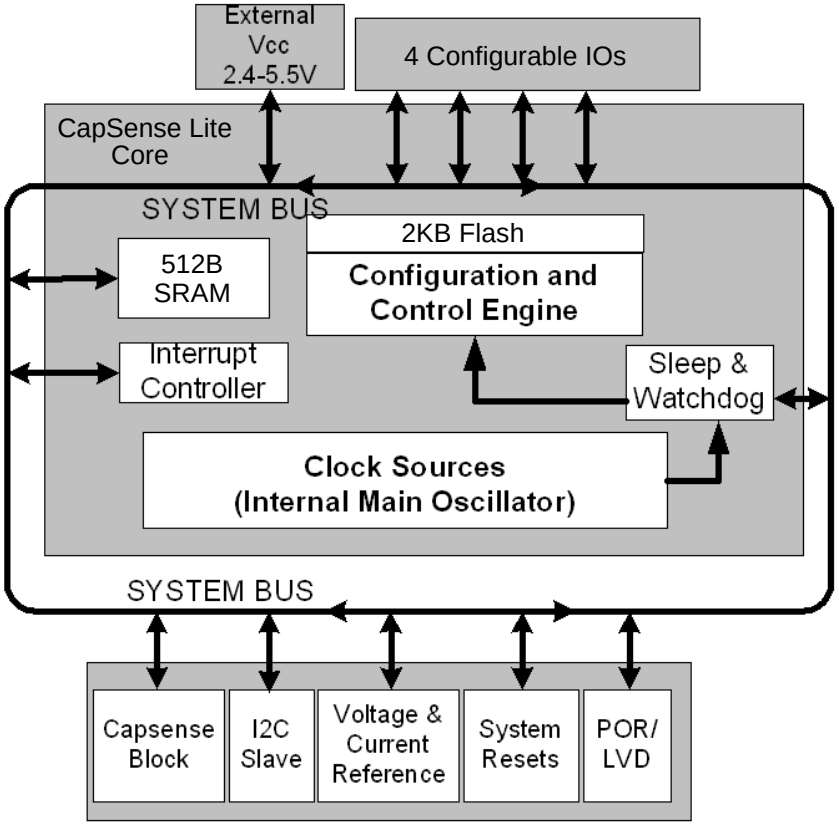
The logic block diagram shows the internal architecture of CY8C20140.

The user can configure registers with parameters needed to adjust the operation and sensitivity of the CapSense system. CY8C20140 supports a standard I²C serial communications interface that allows the host to configure the device and to read sensor information in real time through easy register access.

The CapSense Lite Core

The CapSense Lite Core has a powerful configuration and control block. It encompasses SRAM for data storage, an interrupt controller, sleep and watchdog timers. System resources provide additional capability, such as a configurable I^2C slave communication interface and various system resets. The Analog System is composed of the CapSense PSoC block and an internal 1.8V analog reference, which together support capacitive sensing of up to 4 inputs.

Logic Block Diagram



Pinouts

Figure 1. Pin Diagram - 8 SOIC

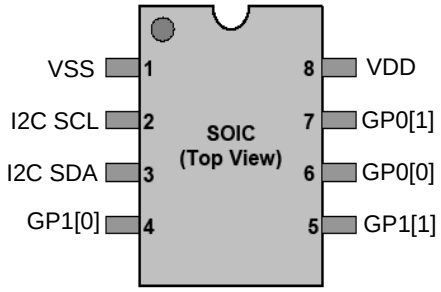


Table 1. Pin Definitions - 8 SOIC

Pin No	Name	Description
1	VSS	Ground connection
2	I^2C SCL	I^2C clock
3	I^2C SDA	I^2C data
4	GP1[0]	Configurable as CapSense or GPIO
5	GP1[1]	Configurable as CapSense or GPIO
6	GP0[0]	Configurable as CapSense or GPIO
7	GP0[1]	Configurable as CapSense or GPIO
8	VDD	Supply Voltage

The CapSense Analog System

The analog system contains the capacitive sensing hardware. Several hardware algorithms are supported. This hardware performs capacitive sensing and scanning without requiring external components. Capacitive sensing is configurable on each GPIO pin. Scanning of enabled CapSense pins is completed quickly and easily across multiple pins.

Additional System Resources

System resources provide additional capability useful to complete systems. Additional resources are low voltage detection and power on reset.

- The I^2C slave provides 50, 100, or 400 kHz communication over two wires.
- Low Voltage Detection (LVD) interrupts can signal the application of falling voltage levels and the advanced POR (Power On Reset) circuit eliminates the need for a system supervisor.

An internal 1.8V reference provides an absolute reference for capacitive sensing.

I^2C Interface

The two modes of operation for the I^2C interface are:

- Device register configuration and status read/write for controller
- Command execution

The I^2C address is programmable during configuration. It can be locked to prevent accidental change by setting a flag in a configuration register.

Electrical Specifications

Absolute Maximum Ratings

Parameter	Description	Min	Typ	Max	Unit	Notes
T_{STG}	Storage temperature	–55	25	+100	°C	Higher storage temperatures reduce data retention time. Recommended storage temperature is +25°C ± 25°C. Extended duration storage temperatures above 65°C degrade reliability.
T_A	Ambient temperature with power applied	–40	–	+85	°C	
V_{DD}	Supply voltage on V_{DD} relative to V_{SS}	–0.5	–	+6.0	V	
V_{IO}	DC input voltage	V_{SS} – 0.5	–	V_{DD} + 0.5	V	
V_{IOZ}	DC voltage applied to tri-state	V_{SS} – 0.5	–	V_{DD} + 0.5	V	
I_{MIO}	Maximum current into any GPIO pin	–25	–	+50	mA	
ESD	Electro static discharge voltage	2000	–	–	V	Human body model ESD
LU	Latch up current	–	–	200	mA	

Operating Temperature

Parameter	Description	Min	Typ	Max	Unit	Notes
T_A	Ambient temperature	–40	–	+85	°C	
T_J	Junction temperature	–40	–	+100	°C	

DC Electrical Characteristics

DC Chip Level Specifications

Parameter	Description	Min	Typ	Max	Unit	Notes
V_{DD}	Supply voltage	2.40	–	5.25	V	
I_{DD}	Supply current	–	1.5	2.5	mA	Conditions are V_{DD} = 3.0V, T_A = 25°C
I_{SB27}	Sleep mode current with POR and LVD active. Mid temperature range	–	2.6	4	µA	V_{DD} = 2.55V, 0°C ≤ T_A ≤ 40°C
I_{SB}	Sleep mode current with POR and LVD active.	–	2.6	5	µA	V_{DD} = 3.3V, –40°C ≤ T_A ≤ 85°C

5V and 3.3V DC General Purpose IO Specifications

Parameter	Description	Min	Typ	Max	Unit	Notes
R_{PU}	Pull up resistor	4	5.6	8	kΩ	
V_{OH1}	High output voltage Port 0 Pins	V_{DD} – 0.2	–	–	V	IOH ≤ 10 µA, Vdd ≥ 3.0V, maximum of 10 mA source current in all IOs.
V_{OH2}	High output voltage Port 0 Pins	V_{DD} – 0.9	–	–	V	IOH = 1 mA, Vdd > 3.0V, maximum of 20 mA source current in all IOs.
V_{OH3}	High output voltage Port 1 Pins	V_{DD} – 0.2	–	–	V	IOH < 10 µA, Vdd> 3.0V, maximum of 10 mA source current in all IOs.
V_{OH4}	High output voltage Port 1 Pins	V_{DD} – 0.9	–	–	V	IOH = 5 mA, Vdd > 3.0V, maximum of 20 mA source current in all IOs.
V_{OH4}	High output voltage Port 1 pins	V_{DD} – 0.9	–	–	V	IOH = 5 mA, Vdd > 3.0V, maximum of 20 mA source current in all IOs.
V_{OH5}	High output voltage Port 1 pins with LDO regulator enabled	2.75	3.0	3.2	V	IOH < 10 µA, Vdd> 3.1V, maximum of 4 IOs all sourcing 5mA.
V_{OH6}	High Output Voltage Port 1 pins with LDO regulator Enabled	2.2	–	–	V	IOH = 5 mA, Vdd > 3.1V, maximum of 20 mA source current in all IOs.
V_{OH7}	High Output Voltage Port 1 pins with LDO regulator enabled	2.1	2.4	2.5	V	IOH < 10 µA, Vdd > 3.0V
V_{OH8}	High Output Voltage Port 1 pins with LDO regulator enabled	2	–	–	V	IOH < 200 µA, Vdd > 3.0V
V_{OL}	Low output voltage	–	–	0.75	V	IOL = 20 mA, Vdd > 3V, maximum of 60 mA sink current on even port pins (for example, P0[2] and P1[4]) and 60 mA sink current on odd port pins (for example, P0[3] and P1[3]).
V_{IL}	Input low voltage	–	–	0.8	V	Vdd = 3.0 to 5.25V.
V_{IH}	Input high voltage	2.0	–	–	V	Vdd = 3.0 to 5.25V.
V_H	Input hysteresis voltage	-	140	-	mV	
I_{IL}	Input leakage	–	1	–	nA	Gross tested to 1 µA.
C_{IN}	Capacitive load on pins as input	0.5	1.7	5	pF	Package and pin dependent. Temp = 25°C.
C_{OUT}	Capacitive load on pins as output	0.5	1.7	5	pF	Package and pin dependent. Temp = 25°C.

2.7V DC General Purpose IO Specifications

Parameter	Description	Min	Typ	Max	Unit	Notes
R_{PU}	Pull up resistor	4	5.6	8	kΩ	
V_{OH1}	High output voltage Port 0 pins	V_{DD} – 0.2	–	–	V	IOH ≤ 10 µA, maximum of 10 mA source current in all IOs.
V_{OH2}	High output voltage Port 0 pins	V_{DD} – 0.5	–	–	V	IOH = 0.2 mA, maximum of 10 mA source current in all IOs.
V_{OH3}	High output voltage Port 1 pins	V_{DD} – 0.2	–	–	V	IOH < 10 µA, maximum of 10 mA source current in all IOs.
V_{OH4}	High output voltage Port 1 pins	V_{DD} – 0.5	–	–	V	IOH = 2 mA, maximum of 10 mA source current in all IOs.
V_{OL}	Low output voltage	–	–	0.75	V	IOL = 10 mA, maximum of 30 mA sink current on even port pins (for example, P0[2] and P1[4]) and 30 mA sink current on odd port pins (for example, P0[3] and P1[3]).
V_{OLP1}	Low output voltage port 1 pins	–	–	0.4	V	IOL=5mA Maximum of 50mA sink current on even port pins (for example, P0[2] and P1[4]) and 50mA sink current on odd port pins (for example, P0[1] and P1[3]). 2.4<=Vdd<=3.6
V_{IL}	Input low voltage	–	–	0.8	V	Vdd = 2.4 to 3.0V.
V_{IH}	Input high voltage	2.0	–	–	V	Vdd = 2.4 to 3.0V.
V_H	Input hysteresis voltage	-	60	-	mV	
I_{IL}	Input leakage	–	1	–	nA	Gross tested to 1 µA.
C_{IN}	Capacitive load on pins as input	0.5	1.7	5	pF	Package and pin dependent. Temp = 25°C.
C_{OUT}	Capacitive load on pins as output	0.5	1.7	5	pF	Package and pin dependent. Temp = 25°C.

3.0V GPIO Specifications

Parameter	Description	Min	Typ	Max	Unit	Notes
V_{IH}	Input High Voltage	1.6	–	–	V	3.0V<=Vdd<=3.6V
V_{OH1}	High Output Voltage Port 1 Pins with 1.8V LDO Regulator Enabled	1.6	1.8	1.95	V	IOH<10uA 3.0V<=Vdd<=3.6V 0C<=TA<=85C
V_{OH2}	High Output Voltage Port 1 Pins with 1.8V LDO Regulator Enabled	1.5	–	–	V	IOH<100uA 3.0V<=Vdd<=3.6V 0C<=TA<=85C

DC POR and LVD Specifications

Parameter	Description	Min	Typ	Max	Unit	Notes
	V_{DD} Value PPOR Trip					Vdd must be greater than or equal to 2.5V during startup, reset from the XRES pin, or reset from Watchdog.
V_{PPOR0}	PORLEV[1:0] = 00b	–	2.36	2.40	V	
V_{PPOR1}	PORLEV[1:0] = 01b	–	2.60	2.65	V	
V_{PPOR2}	PORLEV[1:0] = 10b	–	2.82	2.95	V	
	V_{DD} Value for LVD trip					
VLVD0	VM[2:0] = 000b	2.39	2.45	2.51	V	
VLVD1	VM[2:0] = 001b	2.54	2.71	2.78	V	
VLVD2	VM[2:0] = 010b	2.75	2.92	2.99	V	
VLVD3	VM[2:0] = 011b	2.85	3.02	3.09	V	
VLVD4	VM[2:0] = 100b	2.96	3.13	3.20	V	
VLVD5	VM[2:0] = 101b	–	–	–	V	
VLVD6	VM[2:0] = 110b	–	–	–	V	
VLVD7	VM[2:0] = 111b	4.52	4.73	4.83	V	

AC Electrical Characteristics

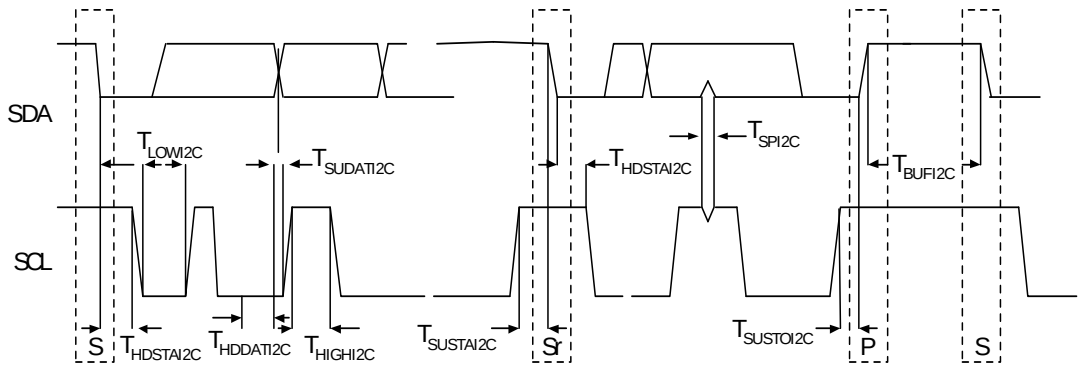
AC General Purpose IO Specifications

Parameter	Description	5.0V/3.3V		2.7V		Unit	Notes
		Min	Max	Min	Max		
TRise0	Rise time, strong mode, Cload = 50pF, Port 0	15	80	15	100	ns	Vdd = 2.4V to 3.0V, 10% - 90%
TRise1	Rise time, strong mode, Cload = 50pF, Port 1	10	50	10	70	ns	Vdd = 2.4V to 3.0V, 10% - 90%
TFall	Fall time, strong mode, Cload = 50pF, All Ports	10	50	10	70	ns	Vdd = 2.4V to 3.0V, 10% - 90%

AC I²C Specifications

Parameter	Description	Standard Mode		Fast Mode		Unit	Notes
		Min	Max	Min	Max		
F_{SCLI2C}	SCL clock frequency	0	100	0	400	KHz	Fast mode not supported for Vdd < 3.0V
$T_{HDSTAI2C}$	Hold time (repeated) START condition. After this period, the first clock pulse is generated.	4.0	-	0.6	-	µs	
T_{LOWI2C}	LOW period of the SCL clock	4.7	-	1.3	-	µs	
$T_{HIGHI2C}$	HIGH period of the SCL clock	4.0	-	0.6	-	µs	
$T_{SUSTAI2C}$	Setup time for a repeated START condition	4.7	-	0.6	-	µs	
$T_{HDDATI2C}$	Data hold time	0	-	0	-	µs	
$T_{SUDATI2C}$	Data setup time	250	-	100	-	ns	
$T_{SUSTOI2C}$	Setup time for STOP condition	4.0	-	0.6	-	µs	
T_{BUFI2C}	BUS free time between a STOP and START condition	4.7	-	1.3	-	µs	
T_{SPI2C}	Pulse width of spikes suppressed by the input filter	-	-	0	50	ns	

Figure 2. Definition for Timing for Fast/Standard Mode on the I²C Bus



Ordering Information

Ordering Code	Package Diagram	Package Type	Operating Temperature
CY8C20140-SX1I	51-85066	8 SOIC	Industrial

Thermal Impedances by Package

Package	Typical θ_{JA}[1]
8 SOIC	127.22 °C/W

Note
1. $T_J = T_A + \text{Power} \times \theta_{JA}$

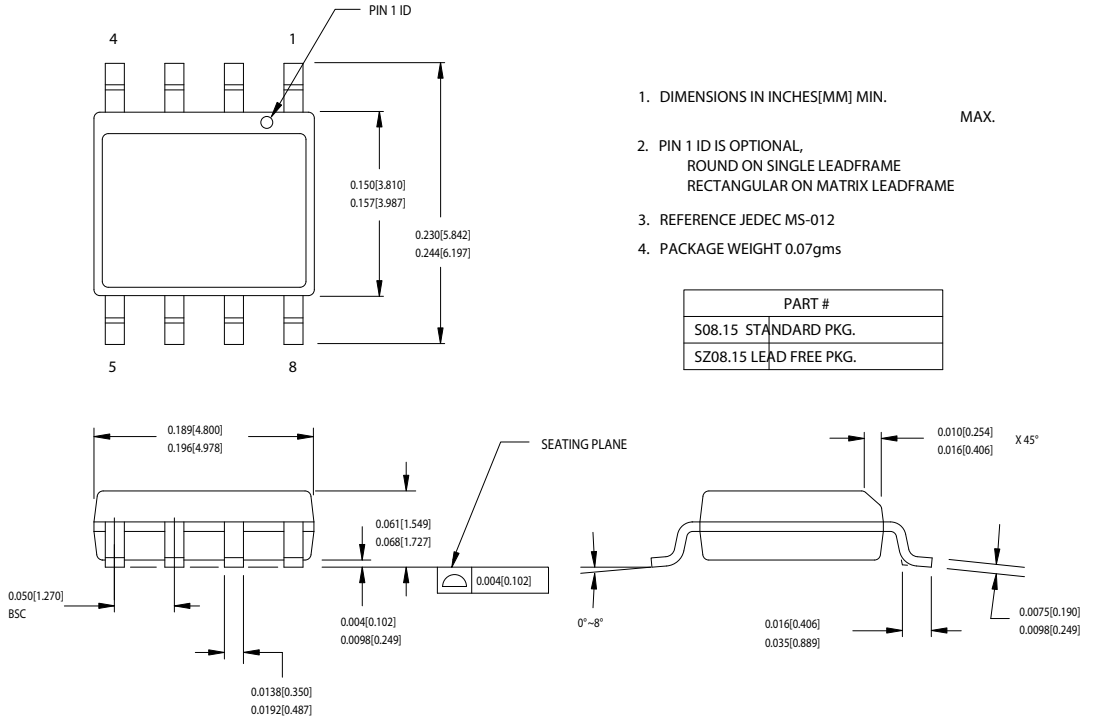
Solder Reflow Peak Temperature

Package	Minimum Peak Temperature[2]	Maximum Peak Temperature
8 SOIC	240 °C	260 °C

Note
2. Higher temperatures may be required based on the solder melting point. Typical temperatures for solder are 220 ± 5°C with Sn-Pb or 245 ± 5°C with Sn-Ag-Cu paste. Refer to the solder manufacturer specifications.

Package Diagram

Figure 3. 8 - Pin (150-Mil) SOIC



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Document History Page

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REV.	**ECN.**	**Issue Date**	**Orig. of Change**	**Description of Change**
**	1494145	See ECN	TUP/AESA	New Datasheet