HARRIS

HS-65142RH

ADVANCE INFORMATION

Radiation Hardened 1024 x 4 CMOS RAM

Features

- Radiation Hardened EPI-CMOS
- Total Dose ..... $> 5 \times 10^5$ Rad (Si)
- Transient Upset
  - ▸ Short Pulse ..... $> 5 \times 10^9$ Rad (Si)/s
  - ▸ Long Pulse ..... $> 1 \times 10^9$ Rad (Si)/s
- Latch-Up Free ..... $> 1 \times 10^{12}$ Rad (Si)/s
- CMOS Compatible
- Common Data I/O
- Standard JEDEC Pinout
- Asynchronous Operation
- Fast Access Time ..... 75ns Max
- Column Address Access Time (Nibble Mode) ..... 25ns 8 Nibbles Available
- Low Standby Current ..... 50μA Maximum
- Low Standby Power ..... 250μW Maximum
- Completely Static Operation
- Three-State Outputs
- Full Military Temperature Range

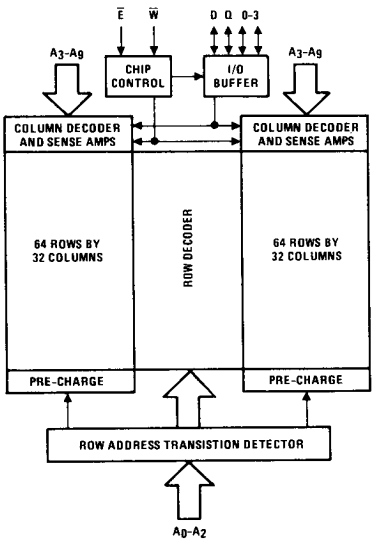
Description

The HS-65142RH is an asynchronous 1024 x 4 static CMOS RAM fabricated using the Harris Custom Integrated Circuit Division's radiation hardened, self-aligned junction isolated silicon gate technology. The device utilizes asynchronous circuitry to achieve high performance and high speed.

Latch-up free operation is achieved by the use of epitaxial starting material to eliminate the parasitic SCR effect seen in conventional bulk CMOS devices. The data outputs can be forced to a high impedance state for use in expanded memory systems.

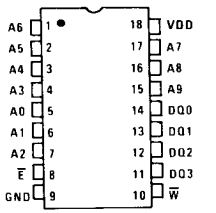
The HS-65142RH is a fully static RAM and may be maintained in any state for an indefinite period of time.

Functional Diagram

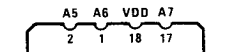


Pinouts

TOP VIEW



TOP VIEW



A — Address Input
$\overline{E}$ — Chip Enable
$\overline{W}$ — Write Enable
DQ — Data In/Out

CAUTION: These devices are sensitive to electrostatic discharge. Proper IC handling procedures should be followed.

Absolute Maximum Ratings*

Supply Voltage (VDD-GND) .....-0.3V to 7.0V
Input or Output Voltage Applied.....GND -0.3 to VDD +0.3V
Storage Temperature.....-65°C to +150°C

Operating Range

Operating Supply Voltage.....4.5V to 5.5V
Operating Temperature.....-55°C to +125°C

CAUTION: As with all semiconductors, stresses listed under "Absolute Maximum Ratings" may be applied to devices (one at a time) without resulting in permanent damage. This is a stress rating only. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. The conditions listed under "Electrical Specifications" are the only conditions recommended for satisfactory operation.

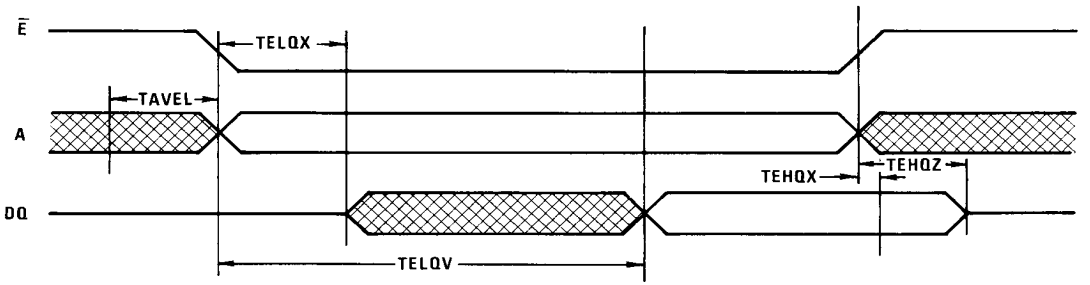
Electrical Specifications ①

	SYMBOL	PARAMETER	MIN	MAX	UNITS	TEST CONDITIONS
D.C.	IDDSB1	Standby Supply Current (CMOS)	—	50	µs	IO = 0, E = VDD -0.3V
	IDD	Enabled Supply Current	—	200	µs	IO = 0, E = VIL
	IDDOP	Operating Supply Current ②	—	7	mA	IO = 0, E = VIL, f = 1MHz
	II	Input Leakage Current	-1.0	+1.0	µA	VI = GND or VDD
	IIOZ	Input/Output Leakage Current	-10.0	+10.0	µA	VIO = GND or VDD
	VDDDR	Data Retention Supply Voltage	3.0	—	V	
	VOL	Output Low Voltage	—	0.4	V	IO = 5.0mA
	VOH	Output High Voltage	4.0	—	V	IO = -5.0mA
	VIL	Input Low Voltage	-0.3	0.8	V	
	VIH	Input High Voltage	VDD -1.5	VDD +0.3	V	
	CI	Input Capacitance ③	—	8	pF	VI = VDD or GND, f = 1MHz
	CO	Output Capacitance ③	—	10	pF	VIO = VDD or GND, f = 1MHz
READ CYCLE A.C.	TAVAV	Read Cycle Time	75	—	ns	④
	TAVQV	Address Access Time	—	75	ns	④
	TELQV	Chip Enable Access Time	—	75	ns	④
	TELQX	Chip Enable Output Enable Time	20	—	ns	③
	TEHQX	Chip Disable Output Hold Time	20	—	ns	④
	TAXQX	Address Invalid Output Hold Time	20	—	ns	④
	TEHQZ	Chip Disable Output Disable Time	—	20	ns	③
WRITE CYCLE A.C.	TAVAV	Write Cycle Time	75	—	ns	④
	TELWH	Chip Enable to End or Write	65	—	ns	↓
	TWLWH	Write Enable Pulse Width	75	—	ns	↓
	TAVWL	Address Setup Time	0	—	ns	↓
	TWHAX	Address Hold Time	0	—	ns	↓
	TDVWH	Data Setup Time	75	—	ns	↓
	TWHDX	Data Hold Time	0	—	ns	↓
	TWLQZ	Write Enable Output Disable Time	—	20	ns	③
	TWHQX	Write Disable Output Enable Time	0	—	ns	③
	TAVWH	Address Valid to End of Write	65	—	ns	④
	TAVEL	Address Setup Time	0	—	ns	↓
	TEHAX	Address Hold Time	0	—	ns	↓
	TAVEH	Address Valid to End of Write	65	—	ns	↓
	TELEH	Enable Pulse Width	65	—	ns	↓
	TWLEH	Write to End of Write	65	—	ns	↓
	TDVEH	Data Setup Time	75	—	ns	↓
	TEHDX	Data Hold Time	0	—	ns	↓

NOTES: ① All devices tested at worst case temperature and supply voltage limits.
② Typical derating = 7mA/MHz increase in IDDOP, VI = VDD or GND.
③ Guaranteed — not tested.
④ Input pulse levels: 0V to 3.0V
Input rise and fall times: 5ns maximum
Input and output timing reference levels: 1.5V.
Output load: 1TTL gate equivalent and 50pF (including scope and jig).
Output load for output enable and disable times: 1TTL gate equivalent and 5pF (including scope and jig).

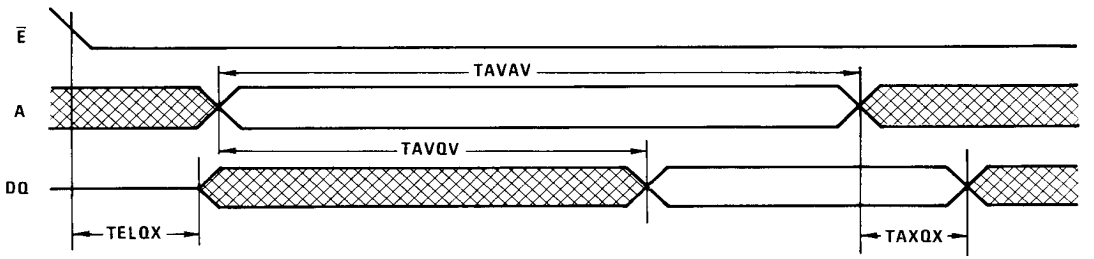
Read Cycle

SYNCHRONOUS OPERATION



NOTES: $\overline{W}$ is held high for entire cycle and D is ignored. Address is stable by the time E goes low and remains valid until $\overline{E}$ goes high.

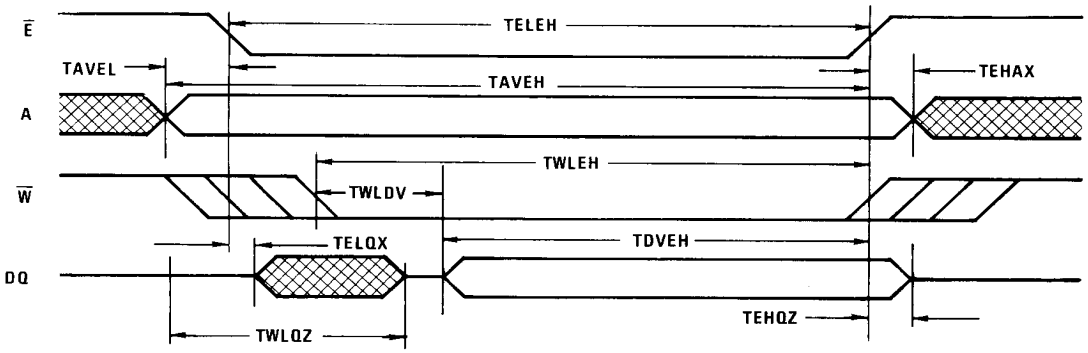
ASYNCHRONOUS OPERATION



NOTE: $\overline{W}$ is high for the entire cycle and D is ignored. $\overline{E}$ is stable prior to A becoming valid and after A becomes invalid.

Write Cycle

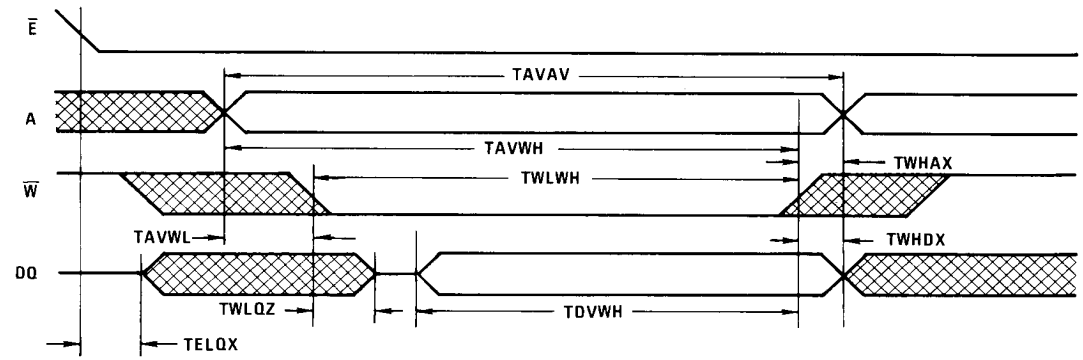
SYNCHRONOUS OPERATION



NOTES: In this mode, $\overline{W}$ rises after $\overline{E}$. If TWLEL ≥ 0 ($\overline{W}$ low before $\overline{E}$), then Q will remain in the high impedance state throughout the cycle.

The Address must remain stable whenever $\overline{E}$ and $\overline{W}$ are both low.

ASYNCHRONOUS OPERATION



NOTES: In this mode, $\overline{E}$ rises after $\overline{W}$. The address must remain stable whenever both $\overline{E}$ and $\overline{W}$ are low.

Radiation Screening Procedure

1. At least 20% of the yielding wafers contribute equally to a population of dice. From that population, a radiation test sample is selected. The sample has a size equivalent to 2 dice taken from 20% of the yielding wafers in a diffusion run.
2. The sample die shall be assembled and tested to the customer's specification for proper operation.
3. The sample devices shall be subjected to a Total Dose Radiation level of 5×10^5 Rad-Si (±10%) from a Gammacell 220 Cobalt 60 source or equivalent. The samples shall be biased at 5 volts with all inputs high. The dose rate shall be between 100 rads/sec and 300 rads/sec.
4. The samples will be tested to the data sheet limits within one hour after irradiation. The lot will be accepted only if all units, exclusive of nonradiation failures, meet the specified limits.
5. Radiation screening to a higher total dose is available. Customers should contact the factory for details.

Radiation Effects

The HS-65142RH has been designed to survive in a radiation environment and to meet the electrical characteristcs. Latch-up free operation is achieved by the use of epitaxial starting material. Improved total dose hardness is obtained with special low temperature processing cycles. On a production basis, Harris performs screens for total dose hardness to a level of 5×10^5 Rad-Si. Transient radiation tests have shown the following results:

- Latch-up free to doses $\geq 1 \times 10^{12}$ rads/sec.
- Upset (short pulse) $\geq 5 \times 10^9$ rads/sec.
- Upset (long pulse) $\geq 1 \times 10^9$ rads/sec.