

January 1998

### Features

- 1.5A, 500V
- $r_{DS(ON)} = 7.0\Omega$
- Single Pulse Avalanche Energy Rated
- SOA is Power Dissipation Limited
- Nanosecond Switching Speeds
- High Input Impedance
- 150°C Operating Temperature
- Related Literature
  - TB334 "Guidelines for Soldering Surface Mount Components to PC Boards"

### Ordering Information

PART NUMBER	PACKAGE	BRAND
IRFU410	TO-251AA	IFU410
IRFR410	TO-252AA	IFR410

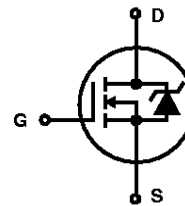
NOTE: When ordering, use the entire part number.

### Description

These are N-Channel enhancement mode silicon gate power field effect transistors. They are advanced power MOSFETs designed, tested, and guaranteed to withstand a specified level of energy in the breakdown avalanche mode of operation. All of these power MOSFETs are designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high power bipolar switching transistors requiring high speed and low gate drive power. These types can be operated directly from integrated circuits.

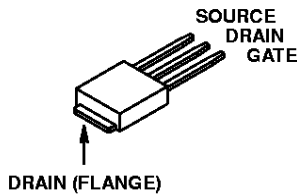
Formerly developmental type TA17445.

### Symbol

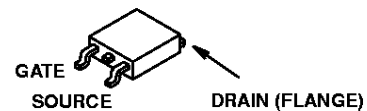


### Packaging

JEDEC TO-251AA



JEDEC TO-252AA



## IRFR410, IRFU410

### Absolute Maximum Ratings $T_C = 25^\circ\text{C}$ , Unless Otherwise Specified

	IRFR410, IRFU410	UNITS
Drain to Source Voltage (Note 1) . . . . .	500	V
Drain to Gate Voltage ( $R_{GS} = 20\text{k}\Omega$ ) (Note 1) . . . . .	500	V
Continuous Drain Current . . . . .	1.5	A
$T_C = 100^\circ\text{C}$ . . . . .	1.2	A
Pulsed Drain Current (Note 2) . . . . .	3.0	A
Gate to Source Voltage . . . . .	$\pm 20$	V
Maximum Power Dissipation . . . . .	42	W
Linear Derating Factor . . . . .	0.33	W/ $^\circ\text{C}$
Single Pulse Avalanche Rating (See Figure 5). . . . .	Refer to UIS Curve	mj
Operating and Storage Temperature . . . . .	-55 to 150	$^\circ\text{C}$
Maximum Temperature for Soldering		
Leads at 0.063in (1.6mm) from Case for 10s . . . . .	300	$^\circ\text{C}$
Package Body for 10s, See Techbrief 334 . . . . .	260	$^\circ\text{C}$

**CAUTION:** Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

**NOTE:**

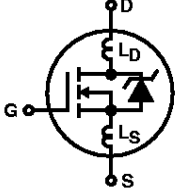
1.  $T_J = 25^\circ\text{C}$  to  $125^\circ\text{C}$ .

### Electrical Specifications $T_C = 25^\circ\text{C}$ , Unless Otherwise Specified

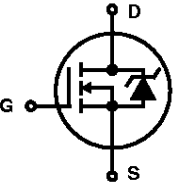
PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Drain to Source Breakdown Voltage	$BV_{DSS}$	$I_D = 250\mu\text{A}$ , $V_{GS} = 0\text{V}$	500	-	-	V
Temperature Coefficient of Breakdown Voltage	$\Delta B-V_{DSS}/\Delta T_J$	Reference to $25^\circ\text{C}$ , $I_D = 250\mu\text{A}$	-	0.61	-	$V/^\circ\text{C}$
Gate to Source Threshold Voltage	$V_{GS(TH)}$	$V_{GS} = V_{DS}$ , $I_D = 250\mu\text{A}$	2	-	4	V
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS} = 500\text{V}$ , $V_{GS} = 0\text{V}$	-	-	25	$\mu\text{A}$
		$V_{DS} = 500\text{V}$ , $V_{GS} = 0\text{V}$ , $T_J = 125^\circ\text{C}$	-	-	250	$\mu\text{A}$
Gate to Source Leakage Current	$I_{GSS}$	$V_{GS} = \pm 20\text{V}$	-	-	$\pm 100$	nA
Drain to Source On Resistance (Note 3)	$r_{DS(ON)}$	$I_D = 1.5\text{A}$ , $V_{GS} = 10\text{V}$ , (Figure 9)	-	-	7.0	$\Omega$
Forward Transconductance (Note 3)	$g_{fs}$	$V_{DS} = 50\text{V}$ , $I_{DS} = 0.75\text{A}$ , (Figure 8)	0.5	-	-	S
Turn-On Delay Time	$t_{d(ON)}$	$V_{DD} = 250\text{V}$ , $I_D \approx 1.5\text{A}$ , $R_G = 24\Omega$ , $R_L = 167\Omega$ , (Figures 15, 16) MOSFET Switching Times are Essentially Independent of Operating Temperature	-	7	-	ns
Rise Time	$t_r$		-	10	-	ns
Turn-Off Delay Time	$t_{d(OFF)}$		-	24	-	ns
Fall Time	$t_f$		-	15	-	ns
Total Gate Charge	$Q_{g(TOT)}$	$V_{GS} = 10\text{V}$ , $I_{D^*} = 1.5\text{A}$ , $V_{DS} = 0.8 \times \text{Rated } BV_{DSS}$ , (Figures 12, 17, 18) Gate Charge is Essentially Independent of Operating Temperature	-	9	12	nC
Gate to Source Charge	$Q_{gs}$		-	1.1	1.4	nC
Gate to Drain "Miller" Charge	$Q_{gd}$		-	5	7	nC
Input Capacitance	$C_{ISS}$	$V_{GS} = 0\text{V}$ , $V_{DS} = 25\text{V}$ , $f = 1.0\text{MHz}$ , (Figure 10)	-	210	-	pF
Output Capacitance	$C_{OSS}$		-	30	-	pF
Reverse Transfer Capacitance	$C_{RSS}$		-	7	-	pF

# IRFR410, IRFU410

## Electrical Specifications $T_C = 25^\circ\text{C}$ , Unless Otherwise Specified (Continued)

PARAMETER	SYMBOL	TEST CONDITIONS		MIN	TYP	MAX	UNITS
Internal Drain Inductance	$L_D$	Measured From the Drain Lead, 6mm (0.25in) From Package to Center of Die	Modified MOSFET Symbol Showing the Internal Devices Inductances 	-	4.5	-	nH
Internal Source Inductance	$L_S$	Measured From The Source Lead, 6mm (0.25in) From Header to Source Bonding Pad		-	7.5	-	nH
Thermal Resistance Junction to Case	$R_{\theta JC}$			-	-	3.0	$^\circ\text{C/W}$
Thermal Resistance Junction to Ambient	$R_{\theta JA}$	Free Air Operation		-	-	110	$^\circ\text{C/W}$

## Source to Drain Diode Specifications

PARAMETER	SYMBOL	TEST CONDITIONS		MIN	TYP	MAX	UNITS
Continuous Source to Drain Current	$I_{SD}$	Modified MOSFET Symbol Showing the Integral Reverse P-N Junction Diode 	-	-	1.5	A	
Pulse Source to Drain Current (Note 2)	$I_{SDM}$		-	-	3.0	A	
Source to Drain Diode Voltage (Note 3)	$V_{SD}$	$T_J = 25^\circ\text{C}$ , $I_{SD} = 1.5\text{A}$ , $V_{GS} = 0\text{V}$ , (Figure 11)		-	-	2.0	V
Reverse Recovery Time (Note 3)	$t_{rr}$	$T_J = 25^\circ\text{C}$ , $I_{SD} = 1.5\text{A}$ , $dI_{SD}/dt = 100\text{A}/\mu\text{s}$		130	-	520	ns

### NOTES:

2. Pulse test: pulse width  $\leq 300\mu\text{s}$ , duty cycle  $\leq 2\%$ .
3. Repetitive rating: pulse width limited by maximum junction temperature. See Transient Thermal Impedance curve. (Figure 3)
4.  $V_{DD} = 50\text{V}$ , starting  $T_J = 25^\circ\text{C}$ ,  $L = 40\mu\text{H}$ ,  $R_G = 25\Omega$ , peak  $I_{AS} = 1.5\text{A}$ .

## Typical Performance Curves Unless Otherwise Specified

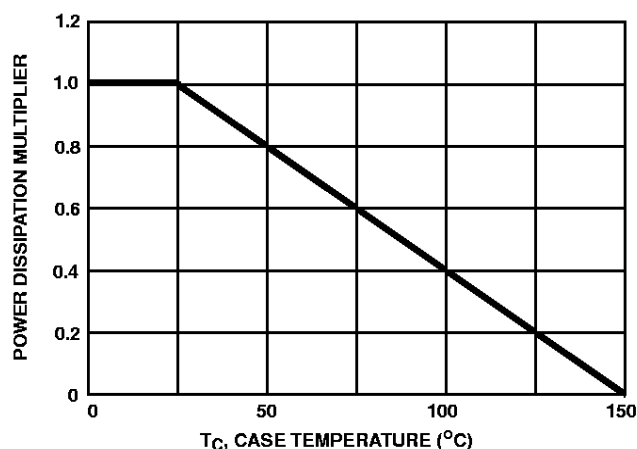


FIGURE 1. NORMALIZED POWER DISSIPATION vs CASE TEMPERATURE

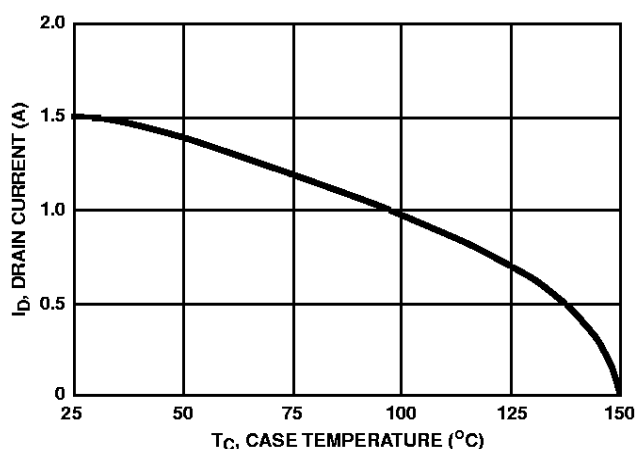


FIGURE 2. MAXIMUM CONTINUOUS DRAIN CURRENT vs CASE TEMPERATURE

Typical Performance Curves Unless Otherwise Specified (Continued)

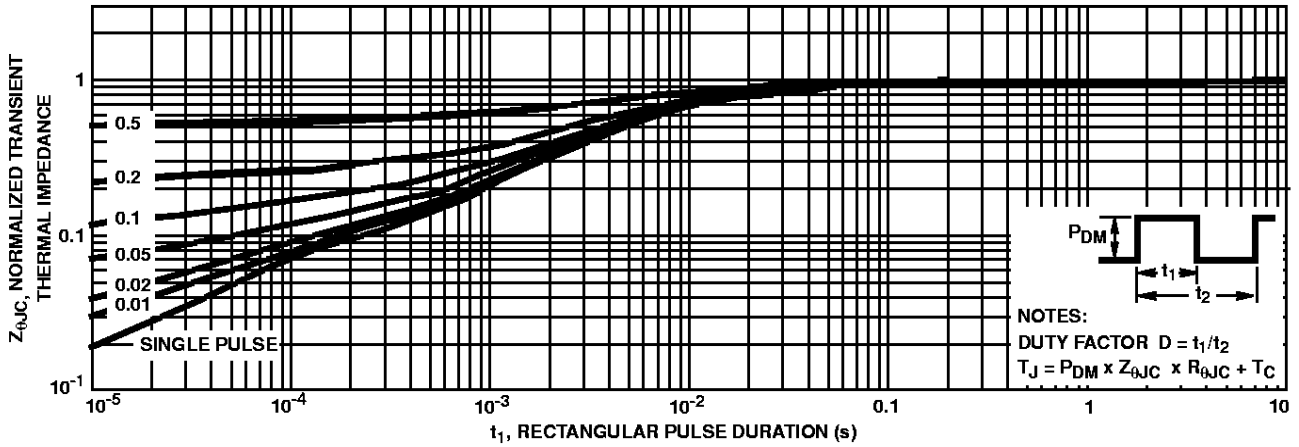


FIGURE 3. NORMALIZED MAXIMUM TRANSIENT THERMAL IMPEDANCE

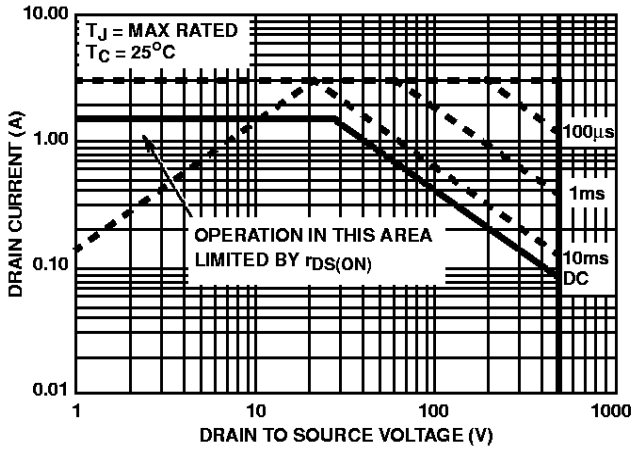


FIGURE 4. FORWARD BIAS SAFE OPERATING AREA

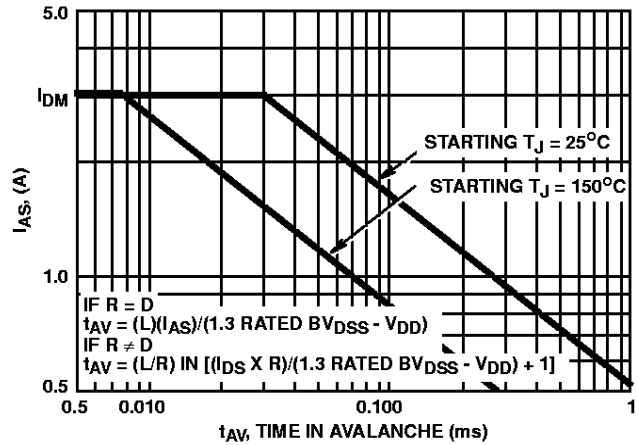


FIGURE 5. UNCLAMPED INDUCTIVE SWITCHING

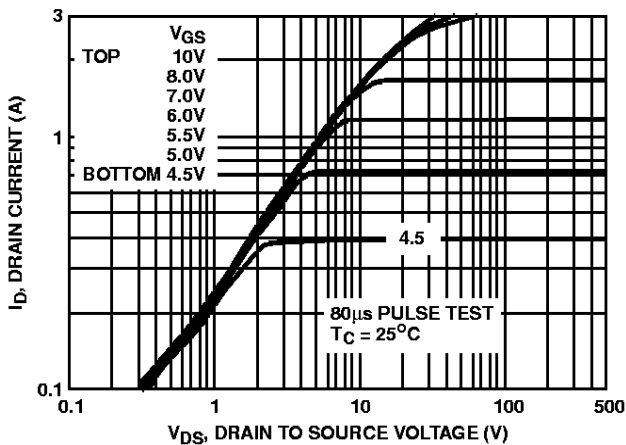


FIGURE 6. OUTPUT CHARACTERISTICS,  $T_C = 25^\circ\text{C}$

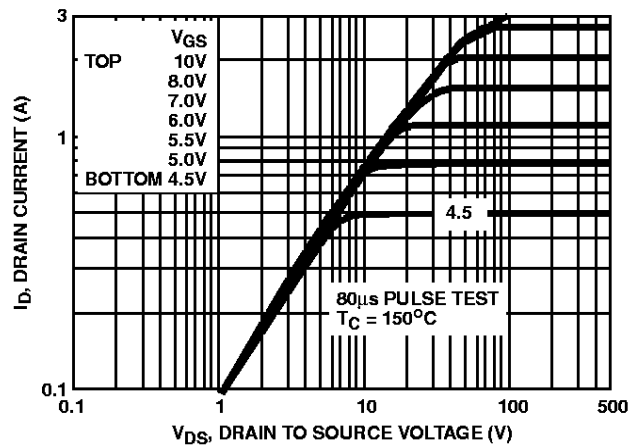


FIGURE 7. OUTPUT CHARACTERISTICS,  $T_C = 150^\circ\text{C}$

Typical Performance Curves Unless Otherwise Specified (Continued)

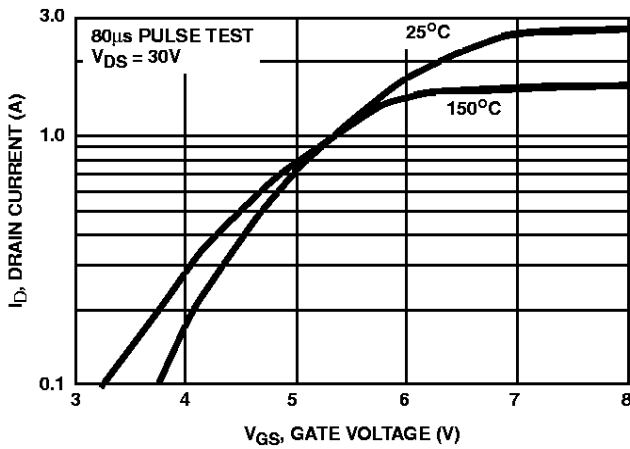


FIGURE 8. TRANSFER CHARACTERISTICS

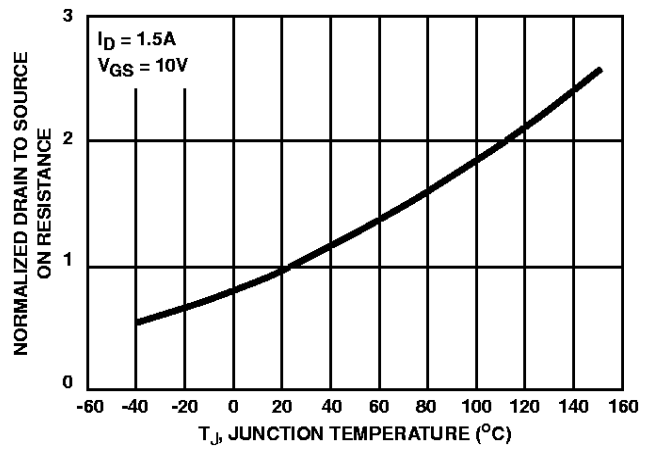


FIGURE 9. NORMALIZED DRAIN TO SOURCE ON RESISTANCE vs. JUNCTION TEMPERATURE

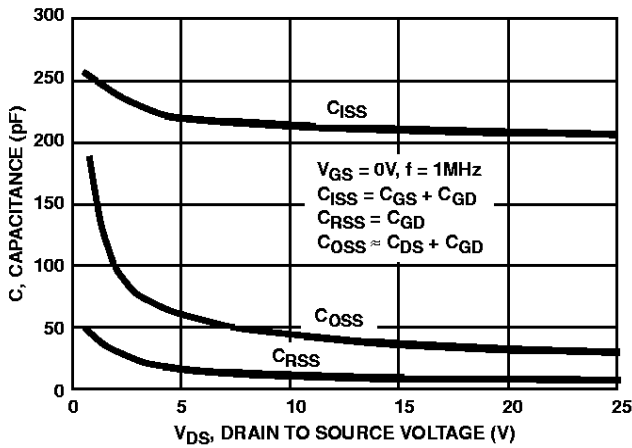


FIGURE 10. CAPACITANCE vs. DRAIN TO SOURCE VOLTAGE

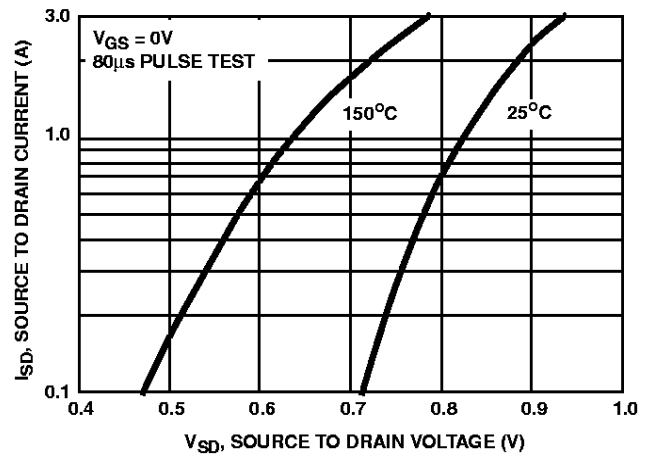


FIGURE 11. SOURCE TO DRAIN DIODE VOLTAGE

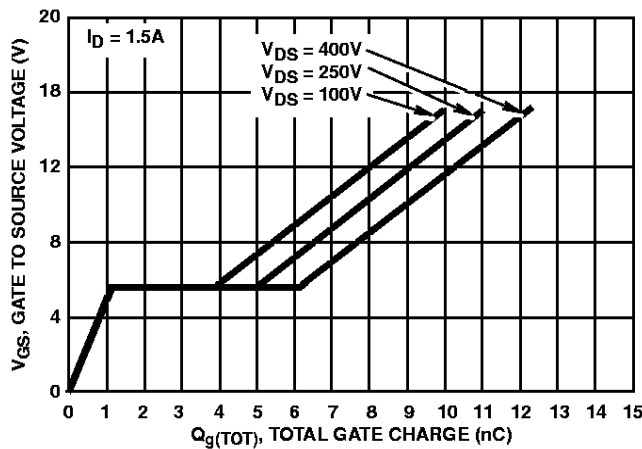


FIGURE 12. GATE TO SOURCE VOLTAGE vs. GATE CHARGE

Test Circuits and Waveforms

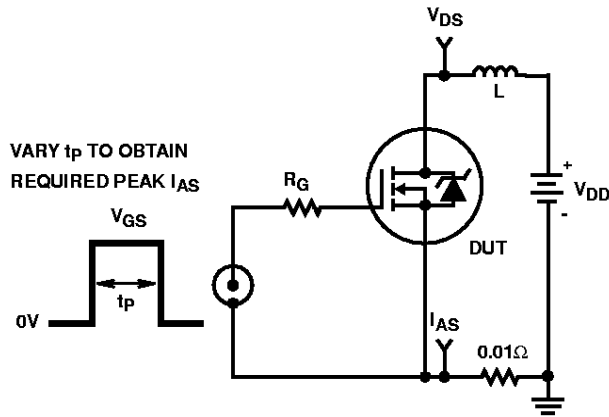


FIGURE 13. UNCLAMPED ENERGY TEST CIRCUIT

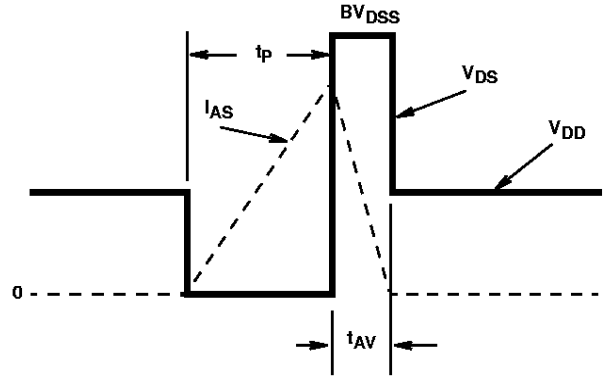


FIGURE 14. UNCLAMPED ENERGY WAVEFORMS

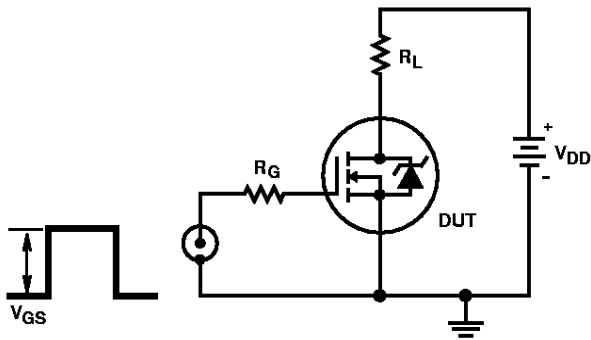


FIGURE 15. SWITCHING TIME TEST CIRCUIT

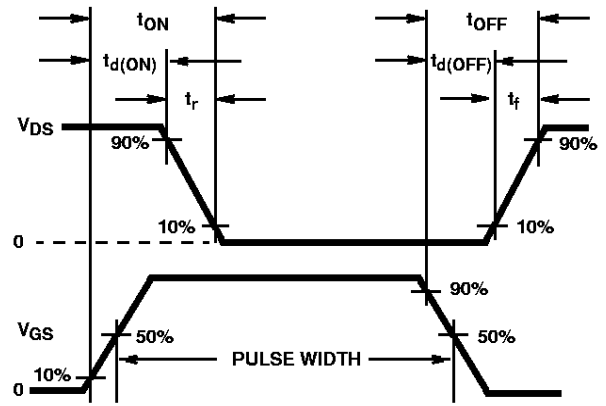


FIGURE 16. RESISTIVE SWITCHING WAVEFORMS

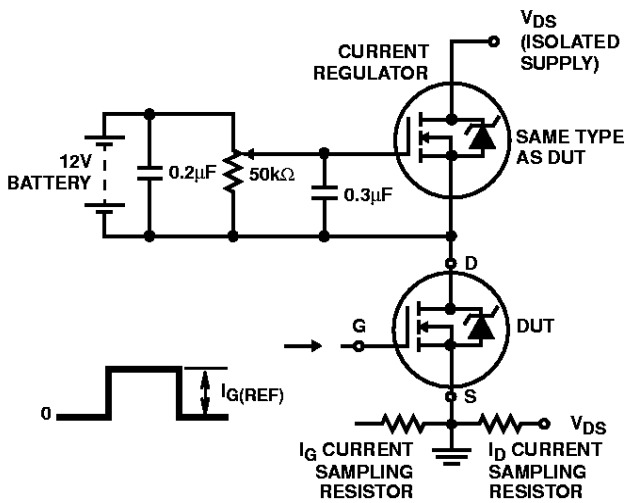


FIGURE 17. GATE CHARGE TEST CIRCUIT

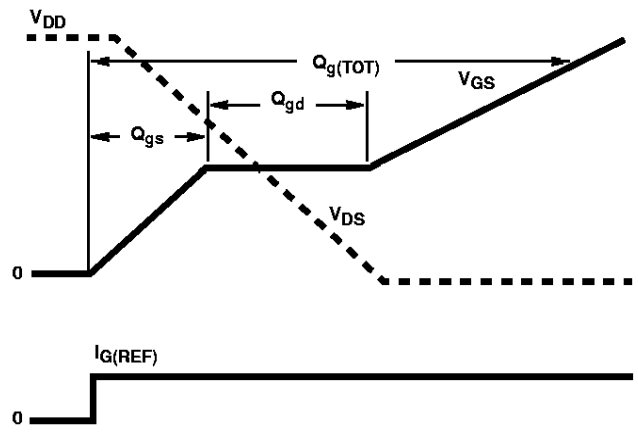


FIGURE 18. GATE CHARGE WAVEFORMS