DESCRIPTION

The M5M5V1132FP is a family of 1M bit synchronous SRAMs organized as 32768-words of 32-bit. The M5M5V1132FP provides a high speed secondary cache solution for microprocessors. The design integrates a 2-bit burst counter, input and output registers with the ultra fast 1M bit SRAM on a single monolithic circuit. This design reduces component count of cache data RAM solutions. Mitsubishi's SRAMs are fabricated with high-performance, low power CMOS technology, providing greater reliability. This device operates on a single 3.3V power supply and are directly LVTTL compatible.

FEATURES

- Access times /Cycle times
  - M5M5V1132FP-6 ..... 5.5ns/10.0ns (100MHz)
  - M5M5V1132FP-7, -7L 7.0ns/13.3ns (75MHz)
  - M5M5V1132FP-8, -8L 8.0ns/15.0ns (66MHz)
  - M5M5V1132FP-10, -10L 10.0ns/16.7ns (60MHz)
- Low power dissipation
  - Active (66MHz) ..... 415mW (typ)
  - Stand-by (-6, -7, -8, -10) ..... 0.7mW (typ)
  - Stand-by (-7L, -8L, -10L) ..... 20μW (typ)
- Package
  - 100pin QFP, Body Size (14.0×20.0 mm^2)
  - Pin Pitch (0.65 mm)
- Single 3.3V power supply (3.13 ~ 3.60V)
- Fully registered inputs and outputs (Pipeline operation)
- Global write control or individual byte write control
- MODE pin allows either liner or interleaved burst
- Snooze mode pin (ZZ) for power down
- CLK stopped stand by mode.
- 32-bit wide data I/O

APPLICATION

486/Pentium™/PowerPC™ processor second level caches

FUNCTION

Synchronous circuitry allows for precise cycle control triggered by a positive edge clock transition. Synchronous signals include : all addresses, all data inputs, all chip selects ($\overline{S}_1$, $\overline{S}_2$, S_2), burst control inputs ($\overline{ADSC}$, $\overline{ADSP}$, $\overline{ADV}$) and write enables ($\overline{MBW}$, $\overline{GW}$, $\overline{BW}_1$, $\overline{BW}_2$, $\overline{BW}_3$, $\overline{BW}_4$). $\overline{S}_2$ and S_2 provide easy depth expansion.

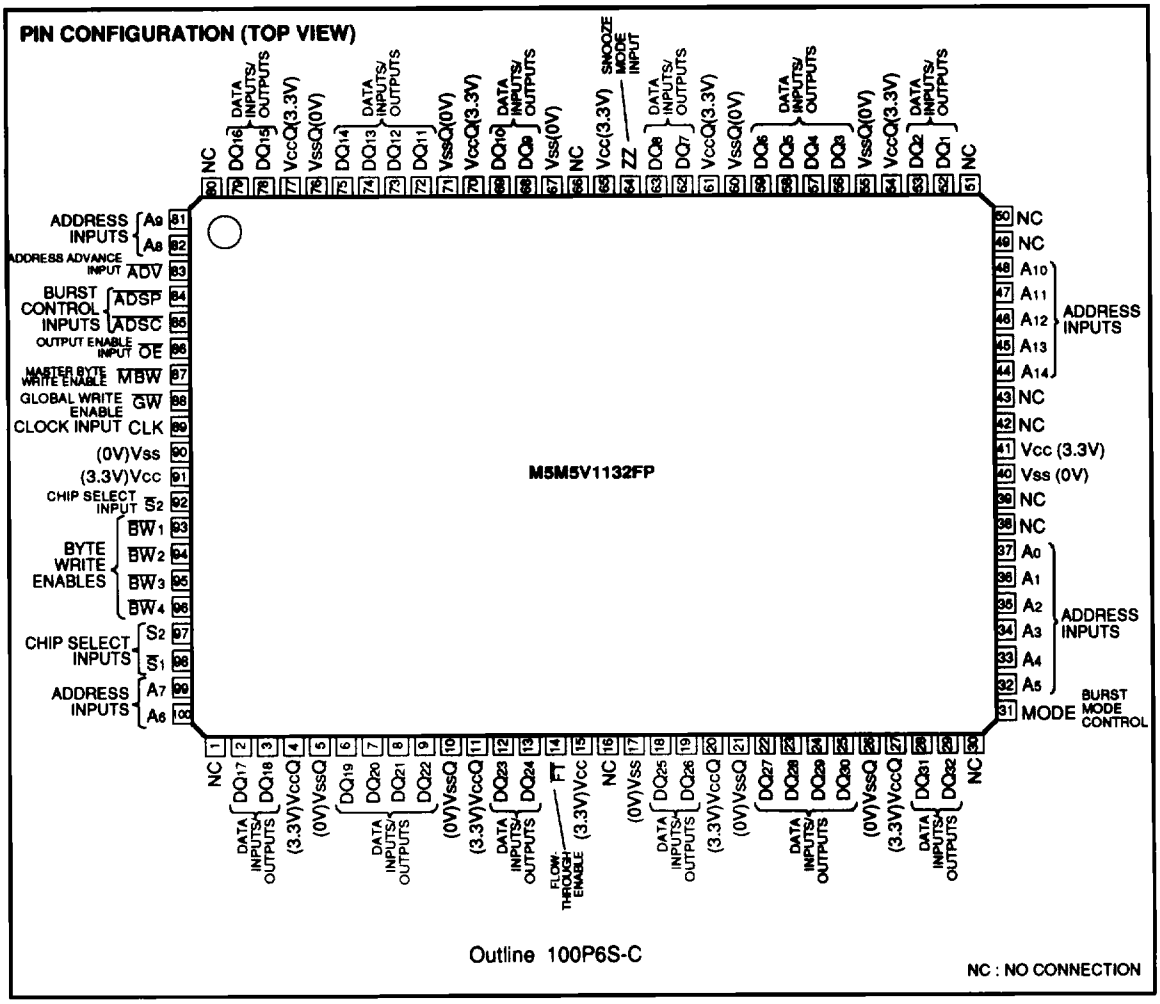
The write operation can be performed by two methods. The global write enable ($\overline{GW}$) will perform a write to all 32 bits. Byte wide writes are controlled by the master byte write enable ($\overline{MWB}$) and the 4 individual byte write enables ($\overline{BW}_1$~$\overline{BW}_4$). The byte write cycle will write from one to four bytes. The write cycle is internally self-timed, eliminating the complex signal generation of an off chip write.

Asynchronous signals are output enable ($\overline{OE}$), snooze mode pin (ZZ) and clock (CLK). The HIGH input of ZZ pin puts the SRAM in the power-down state. When ZZ is pulled to LOW, the SRAM normally operates after 30ns of the wake up period.

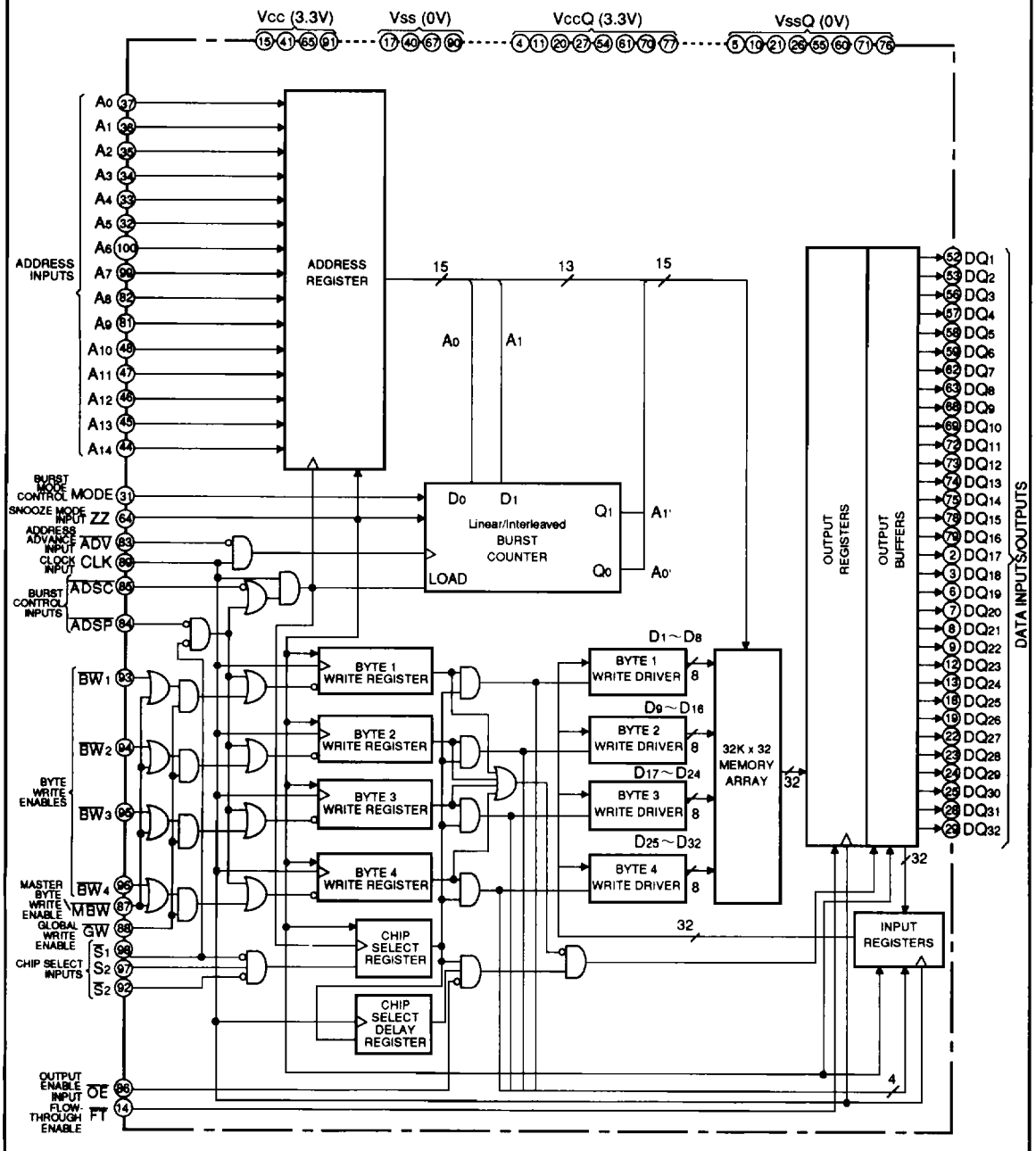
When CLK is stopped and all inputs (Address, Burst control, CLK etc.) are fixed in CMOS level, the SRAM becomes in the power-down state that is called "CLK stopped stand-by mode". During CLK stopped stand-by mode, power supply current is almost same as snooze mode even if the SRAM is selected. When CLK is active again, the SRAM immediately recovers from CLK stopped stand-by mode to normal operation mode.

The burst mode control (MODE), and the flow-through enable ($\overline{FT}$) are DC operated pins. MODE pin will allow the choice of either an interleaved burst, or a linear burst. $\overline{FT}$ pin normally is pulled HIGH. When $\overline{FT}$ is pulled LOW, the SRAM changes non-pipelined type with flow-through output. $\overline{FT}$ LOW input is only used for a test mode.

The burst operation is initiated by either address status processor ($\overline{ADSP}$) or address status controller ($\overline{ADSC}$). The burst advance pin ($\overline{ADV}$) controls subsequent burst addresses.


PIN CONFIGURATION (TOP VIEW)
M5M5V1132FP
Outline 100P6S-C
NC : NO CONNECTION

BLOCK DIAGRAM



Note: The Block Diagram illustrates simplified device operation. See Truth Table, pin descriptions and timing diagrams for detailed information.

PIN FUNCTIONS

Pin	Name	Function
A_0~A_{14}	Synchronous Address Inputs	These inputs are registered and must meet the setup and hold times around the rising edge of CLK.
$\overline{MBW}$	Synchronous Master Byte Write Enables	This active LOW input is used to enable the individual byte write operation. The individual byte write operation is performed when $\overline{MBW}$ is LOW and $\overline{GW}$ is HIGH. The global write operation (a write to all 32 bits) is performed when $\overline{GW}$ is LOW.
$\overline{GW}$	Synchronous Global Write Enables	This active LOW input is used to enable the global write operation (a write to all 32 bits) and must meet the setup and hold times around the rising edge of CLK.
$\overline{BW}_1$, $\overline{BW}_2$, $\overline{BW}_3$, $\overline{BW}_4$	Synchronous Byte Write Enables	These active LOW inputs allow individual bytes to be written and must meet the setup and hold times around the rising edge of CLK. A byte write enables is LOW for a WRITE cycle and HIGH for a READ cycle. $\overline{BW}_1$ controls DQ_1~DQ_8. $\overline{BW}_2$ controls DQ_9 ~DQ_{16}. $\overline{BW}_3$ controls DQ_{17}~DQ_{24}. $\overline{BW}_4$ controls DQ_{25}~DQ_{32}. Data I/O are tristated if any of these four inputs are LOW.
CLK	Clock Input	This signal latches the address, data, chip enables, byte write enables and burst control inputs on its rising edge. All synchronous inputs must meet setup and hold times around the clock's rising edge.
$\overline{S}_1$	Synchronous Chip Select Input	This active LOW input is used to enable the device and conditions internal use of $\overline{ADSP}$. This input is sampled only when a new external address is loaded.
$\overline{S}_2$	Synchronous Chip Select Input	This active LOW input is used to enable the device. This input is sampled only when a new external address is loaded. This input can be used for memory depth expansion.
S_2	Synchronous Chip Select Input	This active HIGH input is used to enable the device. This input is sampled only when a new external address is loaded. This input can be used for memory depth expansion.
$\overline{OE}$	Output Enable Input	This active LOW asynchronous input enables the data I/O output drivers.
DQ_1~DQ_{32}	Data I/O	Byte 1 is DQ_1~DQ_8; Byte 2 is DQ_9~DQ_{16}; Byte 3 is DQ_{17}~DQ_{24}; Byte 4 is DQ_{25}~DQ_{32}. Input data must meet setup and hold times around the rising edge of CLK.
ZZ	Snooze Mode Input	This asynchronous input allows the selection either normal operation mode or snooze mode that the SRAM is in the powerdown state even if CLK is operated. This active HIGH asynchronous input puts the SRAM in the snooze mode. When ZZ=HIGH, Input leak current flows to this pin. When this pin is pulled to LOW or NC, the SRAM normally operates.
MODE	Burst Mode Control	This DC operated pin allows the choice of either a interleaved burst or a linear burst. If this pin is HIGH or NC, an interleaved burst occurs. When this pin is tied LOW, a linear burst occurs, and input leak current flows .
$\overline{FT}$	Flow-through Enable	This DC operated pin is used as a test mode pin. Normally, this pin is pulled HIGH or NC. When this pin is tied LOW, the SRAM changes non-pipelined type with flow-through output, and input leak current flows.
$\overline{ADSP}$	Synchronous Address Status Processor	This active LOW input interrupts any ongoing burst, causing a new external address to be latched. A READ is performed using the new address, independent of the byte write enables and $\overline{ADSC}$ but dependent upon S_2 and $\overline{S}_2$. $\overline{ADSP}$ is ignored if $\overline{S}_1$ is HIGH. Power-down state is entered if S_2 is LOW or $\overline{S}_2$ is HIGH.
$\overline{ADSC}$	Synchronous Address Status Controller	This active LOW input interrupts any ongoing burst and causes a new external address to be latched. A READ or WRITE is performed using the new address if all chip enables are active. Power-down state is entered if one or more chip enables are inactive.
$\overline{ADV}$	Synchronous Address Advance	This active LOW input is used to advance the internal burst counter, controlling burst access after the external address is loaded. A HIGH on this pin effectively causes wait states to be generated (no address advance). This pin must be HIGH at the rising edge of the first clock after an $\overline{ADSP}$ cycle is initiated if a WRITE cycle is desired (to ensure use of correct address)
Vcc	Vcc	Power Supply (3.3V)
Vss	Vss	Ground (0V)
VccQ	VccQ	I/O Buffer Supply (3.3V)
VssQ	VssQ	I/O Buffer Ground (0V)

DC OPERATED TRUTH TABLE

Name	Input status	Operation
MODE	H or NC	Interleaved Burst Sequence
	L	Linear Burst Sequence
$\overline{FT}$	H or NC	Pipelined SRAM
	L	Non-pipelined SRAM (Test mode)

Note 1. MODE and $\overline{FT}$ are DC operated pins.
2. H means logic HIGH or NC. L means logic LOW. NC meons No-Connection
3. Normally, $\overline{FT}$ is pulled to HIGH or NC. $\overline{FT}$ LOW input is only used for a test mode.
4. See BURST SEQUENCE TABLE about Interleaved and Linear Burst Sequence.

BURST SEQUENCE TABLE

Interleaved Burst Sequence (when MODE = HIGH or NC)

Operation	A_{14} -A_2	A_1	A_0
First access, latch external address	A_{14} -A_2	A_1	A_0
Second access (first burst address)	latched A_{14} -A_2	latched A_1	latched $\overline{A_0}$
Third access (second burst address)	latched A_{14} -A_2	latched $\overline{A_1}$	latched A_0
Fourth access (third burst address)	latched A_{14} -A_2	latched $\overline{A_1}$	latched $\overline{A_0}$

Linear Burst Sequence (when MODE = LOW)

Operation	A_{14} -A_2	A_1, A_0			
First access, latch external address	A_{14} -A_2	0, 0	0, 1	1, 0	1, 1
Second access (first burst address)	latched A_{14} -A_2	0, 1	1, 0	1, 1	0, 0
Third access (second burst address)	latched A_{14} -A_2	1, 0	1, 1	0, 0	0, 1
Fourth access (third burst address)	latched A_{14} -A_2	1, 1	0, 0	0, 1	1, 0

Note 5. The burst sequence wraps around to its initial state upon completion.

SYNCHRONOUS TRUTH TABLE

$\overline{S_1}$	$\overline{S_2}$	S_2	$\overline{ADSP}$	$\overline{ADSC}$	$\overline{ADV}$	$\overline{Write}$	CLK	Address used	Operation
H	X	X	X	L	X	X	L-H	None	Deselected Cycle, Power-down
L	X	L	L	X	X	X	L-H	None	Deselected Cycle, Power-down
L	H	X	L	X	X	X	L-H	None	Deselected Cycle, Power-down
L	X	L	X	L	X	X	L-H	None	Deselected Cycle, Power-down
L	H	X	X	L	X	X	L-H	None	Deselected Cycle, Power-down
L	L	H	L	X	X	X	L-H	External	READ Cycle, Begin Burst
L	L	H	H	L	X	L	L-H	External	WRITE Cycle, Begin Burst
L	L	H	H	L	X	H	L-H	External	READ Cycle, Begin Burst
X	X	X	H	H	L	H	L-H	Next	READ Cycle, Continue Burst
H	X	X	X	H	L	H	L-H	Next	READ Cycle, Continue Burst
X	X	X	H	H	L	L	L-H	Next	WRITE Cycle, Continue Burst
H	X	X	X	H	L	L	L-H	Next	WRITE Cycle, Continue Burst
X	X	X	H	H	H	H	L-H	Current	READ Cycle, Suspend Burst
H	X	X	X	H	H	H	L-H	Current	READ Cycle, Suspend Burst
X	X	X	H	H	H	L	L-H	Current	WRITE Cycle, Suspend Burst
H	X	X	X	H	H	L	L-H	Current	WRITE Cycle, Suspend Burst

Note 6. X means "don't care". H means logic HIGH. L means logic LOW.
7. $\overline{Write}$ =L means "WRITE" operation in WRITE TRUTH TABLE.
$\overline{Write}$ =H means "READ" operation in WRITE TRUTH TABLE.
8. All inputs in this table must meet setup and hold times around the rising edge (LOW to HIGH) of CLK.
9. $\overline{ADSP}$ LOW always initiates an internal READ at the L-H edge of CLK.
10. Operation finally depends on status of asynchronous input pins (ZZ and $\overline{OE}$).
See ASYNCHRONOUS TRUTH TABLE.

WRITE TRUTH TABLE

$\overline{GW}$	$\overline{MBW}$	$\overline{BW_1}$	$\overline{BW_2}$	$\overline{BW_3}$	$\overline{BW_4}$	Operation
H	H	X	X	X	X	READ
H	L	H	H	H	H	READ
H	L	L	H	H	H	WRITE BYTE 1
H	L	H	L	H	H	WRITE BYTE 2
H	L	H	H	L	H	WRITE BYTE 3
H	L	H	H	H	L	WRITE BYTE 4
H	L	L	L	H	H	WRITE BYTE1 and 2
H	L	H	H	L	L	WRITE BYTE3 and 4
H	L	L	L	L	L	WRITE ALL BYTE
L	X	X	X	X	X	WRITE ALL BYTE

Note 11. X means "don't care". H means logic HIGH. L means logic LOW.
12. All inputs in this table must meet setup and hold ties around the rising edge (LOW to HIGH) of CLK.

ASYNCHRONOUS TRUTH TABLE

ZZ	$\overline{OE}$	Operation of synchronous truth table	Operation	I/O Status
H	X	X	Snooze mode	High-Z
L or NC	L	READ	READ	Q
L or NC	H	READ	READ	High-Z
L or NC	X	WRITE	WRITE	High-Z - D
L or NC	X	Deselected	Deselected	High-Z

Note 13. For a write operation following a read operation, $\overline{OE}$ must be HIGH before the input data required setup time and held HIGH through the input data hold time.
14. In I/O STATUS, Q means output data during a read cycle, and D means input data during a write cycle.
15. "Snooze mode" means power down state of which stand-by current does not depend on cycle time.
16. "Deselected" means power down state of which stand-by current depends on cycle time.
17. When ZZ is pulled to LOW, the SRAM normally operates after 30ns of the wake up period.

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Power supply voltage	With respect to GND	−2.0* ~4.6	V
V_{CCQ}	I/O buffer supply voltage		−2.0* ~Vcc+0.5 (max 4.6)	V
V_I	Input voltage		−2.0* ~Vcc+0.5 (max 4.6)	V
V_O	Output voltage		−2.0* ~4.6	V
P_d	Maximum power dissipation		1.2	W
T_{opr}	Operating temperature		0~70	℃
$T_{stg(bias)}$	Storage temperature (bias)		−10~85	℃
T_{stg}	Storage temperature		−65~150	℃

* This is −2.0V when pulse width ≤ 10ns, and −0.5V in case of DC.

DC ELECTRICAL CHARACTERISTICS (Ta = 0~70℃; Vcc = 3.13 ~ 3.60V, unless otherwise noted)

Symbol	Parameter	Test conditions		Limits Min	Limits Typ	Limits Max	Unit
V_{CC}	Power supply voltage			3.13		3.60	V
V_{CCQ}	I/O buffer supply voltage			Vcc − 0.3		Vcc+0.3	V
V_{IH}	High-level input voltage			2.0		Vcc+0.3	V
V_{IL}	Low-level input voltage			−0.3*		0.8	V
V_{OH}	High-level output voltage	I_{OH} = −4mA		2.4			V
V_{OL}	Low-level output Voltage	I_{OL} = 8mA				0.4	V
I_I	Input current except ZZ, MODE and $\overline{FT}$	V_I = 0V~Vcc				2	μA
	Input current of MODE and $\overline{FT}$	V_I = Vcc				2	
		V_I = 0V				100	
	Input current of ZZ	V_I = Vcc				200	
		V_I = 0V				2	
I_{OZ}	Off - State output current	V_I ($\overline{OE}$) ≧V_{IH}, V_O = 0~Vcc				10	μA
I_{CC1}	Active power supply current	Output open Device selected V_I ≦V_{IL} or V_I ≧V_{IH} ZZ≦V_{IL}	AC (10.0ns cycle,100MHz)		250	300	mA
			AC (13.3ns cycle,75MHz)		140	200	
			AC (15.0ns cycle,66MHz)		125	170	
			AC (16.7ns cycle,60MHz)		110	160	
I_{CC2}	TTL Stand-by current	Device deselected V_I ≦V_{IL} or V_I ≧V_{IH} ZZ≦V_{IL}	AC (10.0ns cycle,100MHz)		75	95	mA
			AC (13.3ns cycle,75MHz)		55	70	
			AC (15.0ns cycle,66MHz)		50	65	
			AC (16.7ns cycle,60MHz)		45	60	
			CLK frequency=0MHz All inputs statics		15	20	
I_{CC3}	CMOS Stand-by current (CLK stopped stand-by mode)	Output open VI ≦0.2V or VI ≧Vcc− 0.2V ZZ≦0.2V, $\overline{FT}$≧Vcc− 0.2V MODE≧Vcc− 0.2V CLK frequency=0MHz All inputs static	-6, -7, -8, -10		0.2	2	mA
			-7L, -8L, -10L		5	200	μA
I_{CC4}	Snooze mode Stand-by current	Snooze mode ZZ≧Vcc −0.2V $\overline{FT}$≧Vcc− 0.2V MODE≧Vcc− 0.2V	-6, -7, -8, -10		0.2	2	mA
			-7L, -8L, -10L		5	200	μA

Note 18. V_{IL}min* is −2.0V in case of AC (Pulse width ≦10ns).
19. "Device Deselected" means device is in POWER-DOWN mode as defined in the truth table.
20. Spec of I_{CC3} canbe supported by stopping CLK evenif device selected state.
21. I_{CC4} does not depend on CLK frequency and input level.

CAPACITANCE

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
C_I	Input capacitance	V_I = GND, V_I = 25mVrms, f = 1MHz			6	pF
C_O	Output capacitance	V_O = GND, V_O = 25mVrms, f = 1MHz			8	pF

This parameter is sampled.

THERMAL RESISTANCE

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
θ_{JA}	Thermal resistance - Junction to Ambient	Suspended in still air		89		°C/W
		Mounted on 70×70×1.6t Mitsubishi standard PC board, Air velocity = 0 m/s		72		
		Mounted on 70×70×1.6t Mitsubishi standard PC board, Air velocity = 1.0 m/s		57		
θ_{JC}	Thermal resistance - Junction to Case	Immersed in fluorinert		19		°C/W

This parameter is sampled.

AC ELECTRICAL CHARACTERISTICS (Ta = 0~70°C; Vcc = 3.13 ~ 3.60V, unless otherwise noted)

(1) MEASUREMENT CONDITIONS

Input pulse levels ..... V_{IH} = 3.0V, V_{IL} = 0V
Input rise and fall times 1.5ns
Input timing reference levels ..... V_{IH} = 1.5V, V_{IL} = 1.5V
Output reference levels ..... V_{OH} = 1.5V, V_{OL} = 1.5V
Output load ..... Fig. 1, 2

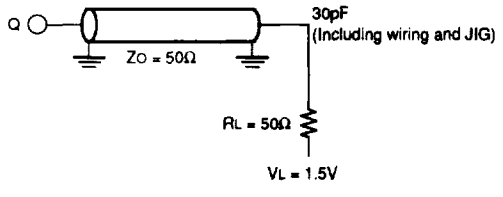


Fig. 1 Output load

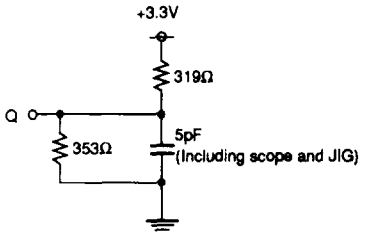


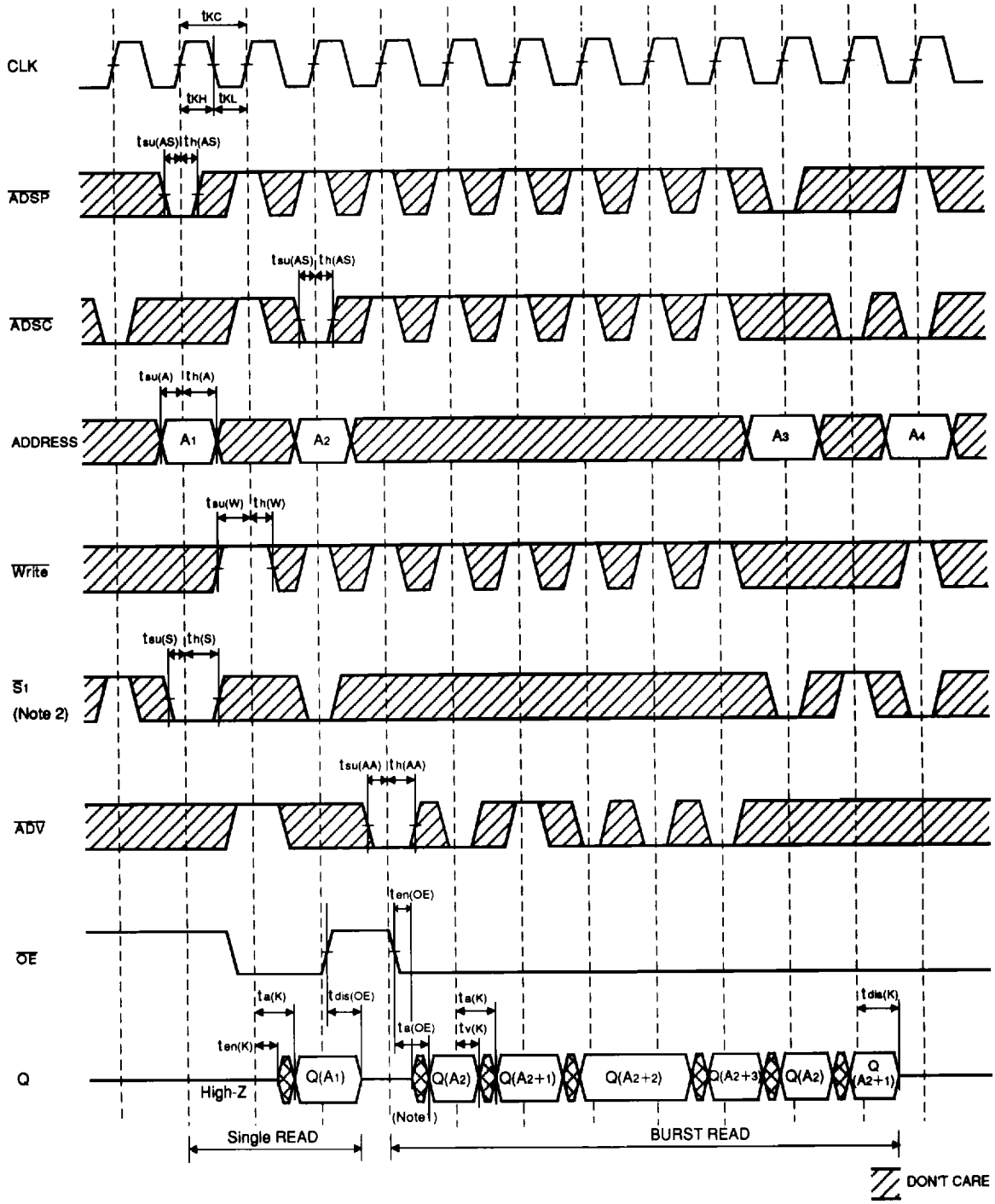
Fig. 2 Output load for ten, tdis

(2) TIMING CHARACTERISTICS

Symbol	Parameter	Limits								Unit
		100MHz -6		75MHz -7, -7L		66MHz -8, -8L		60MHz -10, -10L		
		Min	Max	Min	Max	Min	Max	Min	Max	
Clock										
t_{KC}	Clock cycle time	10		13.3		15		16.7		ns
t_{KH}	Clock HIGH time	3.5		5		6		6		ns
t_{KL}	Clock LOW time	3.5		5		6		6		ns
Output Times										
$t_{a(K)}$	Clock access time		5.5		7		8.0		10	ns
$t_{v(K)}$	Data valid time from Clock	2		2		3		3		ns
$t_{en(K)}$	Output enable time from Clock	0		0		0		0		ns
$t_{dis(K)}$	Output disable time from Clock	1	5.5	2	6	2	6	2	6	ns
$t_{a(OE)}$	OE access time		5.5		6		6		6	ns
$t_{en(OE)}$	Output enable time from OE	0		0		0		0		ns
$t_{dis(OE)}$	Output disable time from OE	1	5	2	6	2	6	2	6	ns
Setup Times										
$t_{su(A)}$	Address	2		2.5		2.5		2.5		ns
$t_{su(AS)}$	Address Status ($\overline{ADSC}$, $\overline{ADSP}$)	2		2.5		2.5		2.5		ns
$t_{su(AA)}$	Address Advance ($\overline{ADV}$)	2		2.5		2.5		2.5		ns
$t_{su(W)}$	Byte Write Enables ($\overline{MBW}$, $\overline{GW}$, $\overline{BWs}$)	2		2.5		2.5		2.5		ns
$t_{su(D)}$	Data-In	2		2.5		2.5		2.5		ns
$t_{su(S)}$	Chip Select enables ($\overline{S}_1$, $\overline{S}_2$, S_2)	2		2.5		2.5		2.5		ns
Hold Times										
$t_{h(A)}$	Address	0.5		0.5		0.5		0.5		ns
$t_{h(AS)}$	Address Status ($\overline{ADSC}$, $\overline{ADSP}$)	0.5		0.5		0.5		0.5		ns
$t_{h(AA)}$	Address Advance ($\overline{ADV}$)	0.5		0.5		0.5		0.5		ns
$t_{h(W)}$	Byte Write Enables ($\overline{MBW}$, $\overline{GW}$, $\overline{BWs}$)	0.5		0.5		0.5		0.5		ns
$t_{h(D)}$	Data-In	0.5		0.5		0.5		0.5		ns
$t_{h(S)}$	Chip Select ($\overline{S}_1$, $\overline{S}_2$, S_2)	0.5		0.5		0.5		0.5		ns
ZZ, MODE $\overline{FT}$										
t_{ZZS}	ZZ Stand-by		30		30		30		30	ns
t_{ZZREC}	ZZ Recovery	30		30		30		30		ns
t_{CFG}	Config setup (MODE, $\overline{FT}$)	40		53.3		60		66.7		ns

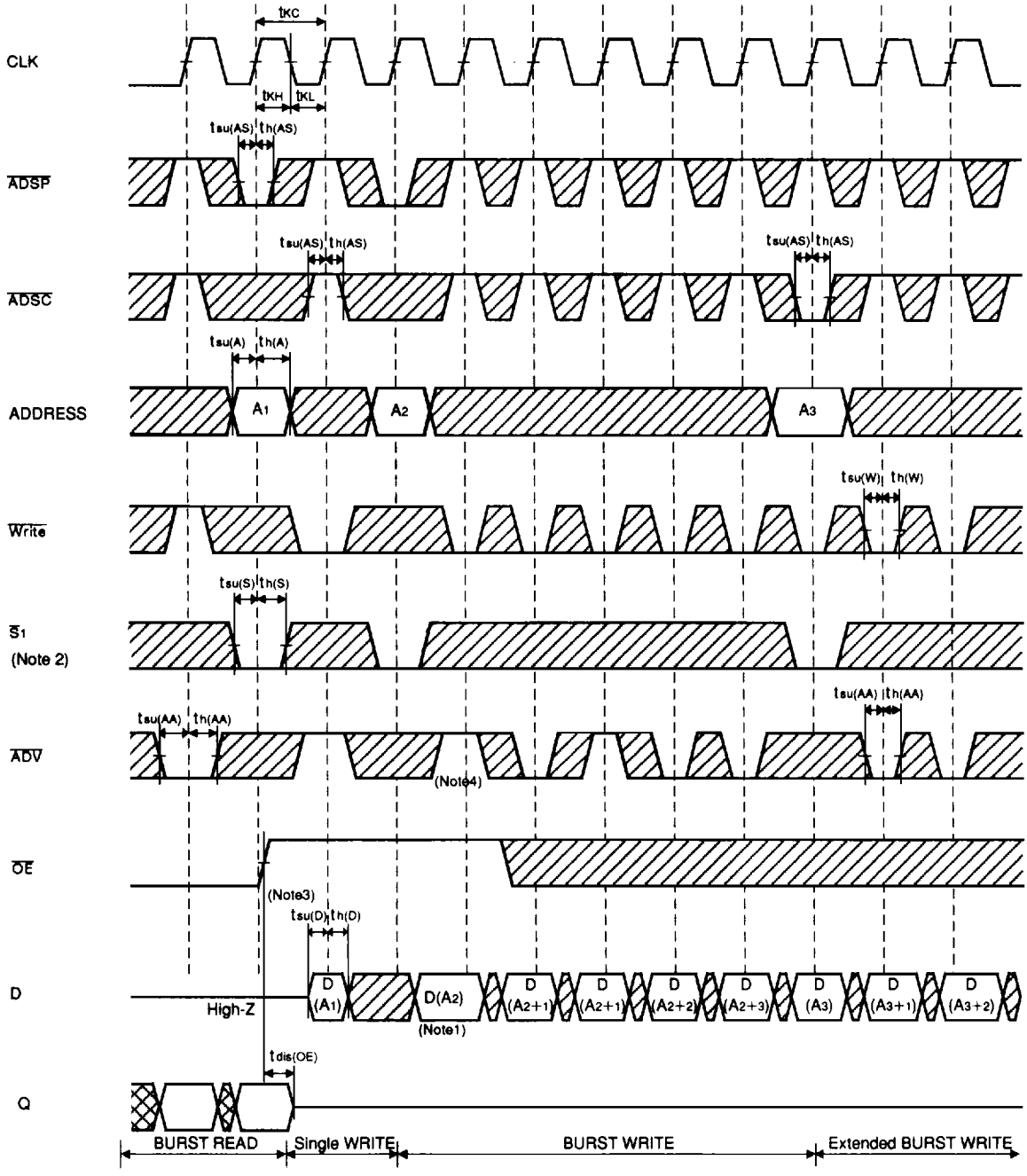
Note 22. All parameters except t_{ZZS}, t_{ZZREC} in this table are measured on condition that ZZ = LOW fix.
23. Test conditions is specified with the output loading shown in Fig. 1 unless otherwise noted.
24. When enable and disable time (t_{en}, t_{dis}) are measured, Output loading is specified with C_L = 5pF as in Fig. 2.
The transition is measured±500mV from steady state voltage.
25. The enable and disable time are sampled.
26. $\overline{ADSP}$ and $\overline{ADSC}$ must not be asserted during t_{ZZS} and t_{ZZREC}, due to a guarantee of data retention for snooze mode.
If synchronous inputs are made combinations of WRITE state during t_{ZZS}, memorized data may be destroyed.
27. Configuration signals (MODE and $\overline{FT}$)are static and must not change during normal operation.

(3) READ TIMING



Note 1. Q(A2) refers to output from address A2. Q(A2+1) refers to output from the next internal burst address following A2.
2. $\overline{S2}$ and S2 have timing identical to $\overline{S1}$. On this diagram, when $\overline{S1}$ is LOW, $\overline{S2}$ is LOW and S2 is HIGH.
When $\overline{S1}$ is HIGH, $\overline{S2}$ is HIGH and S2 is LOW.
3. ZZ = LOW fix.

(4) WRITE TIMING



Note 1. Q(A2) refers to output from address A2. Q(A2+1) refers to output from the next internal burst address following A2.

2. $\overline{S2}$ and S2 have timing identical to $\overline{S1}$. On this diagram, when $\overline{S1}$ is LOW, $\overline{S2}$ is LOW and S2 is HIGH. When S1 is HIGH, S2 is HIGH and S2 is LOW.

3. $\overline{OE}$ must be HIGH before the input data setup and held HIGH throughout the data hold time. This prevents input/output data contention for the time period prior to the byte write enable inputs being sampled.

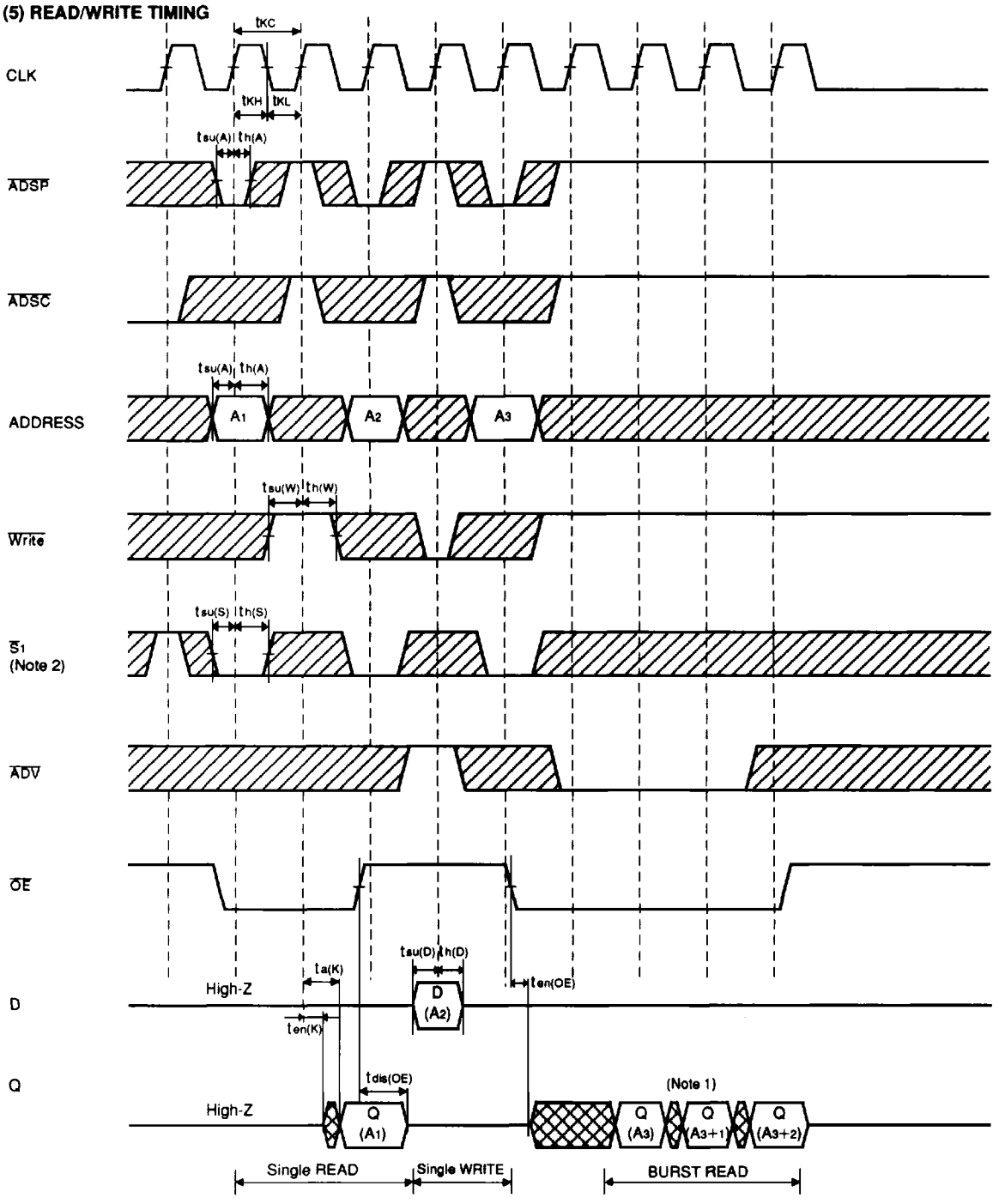
4. $\overline{ADV}$ must be high to permit a write to the loaded address.

5. ZZ = LOW fix.

DON'T CARE

UNDEFINED

(5) READ/WRITE TIMING

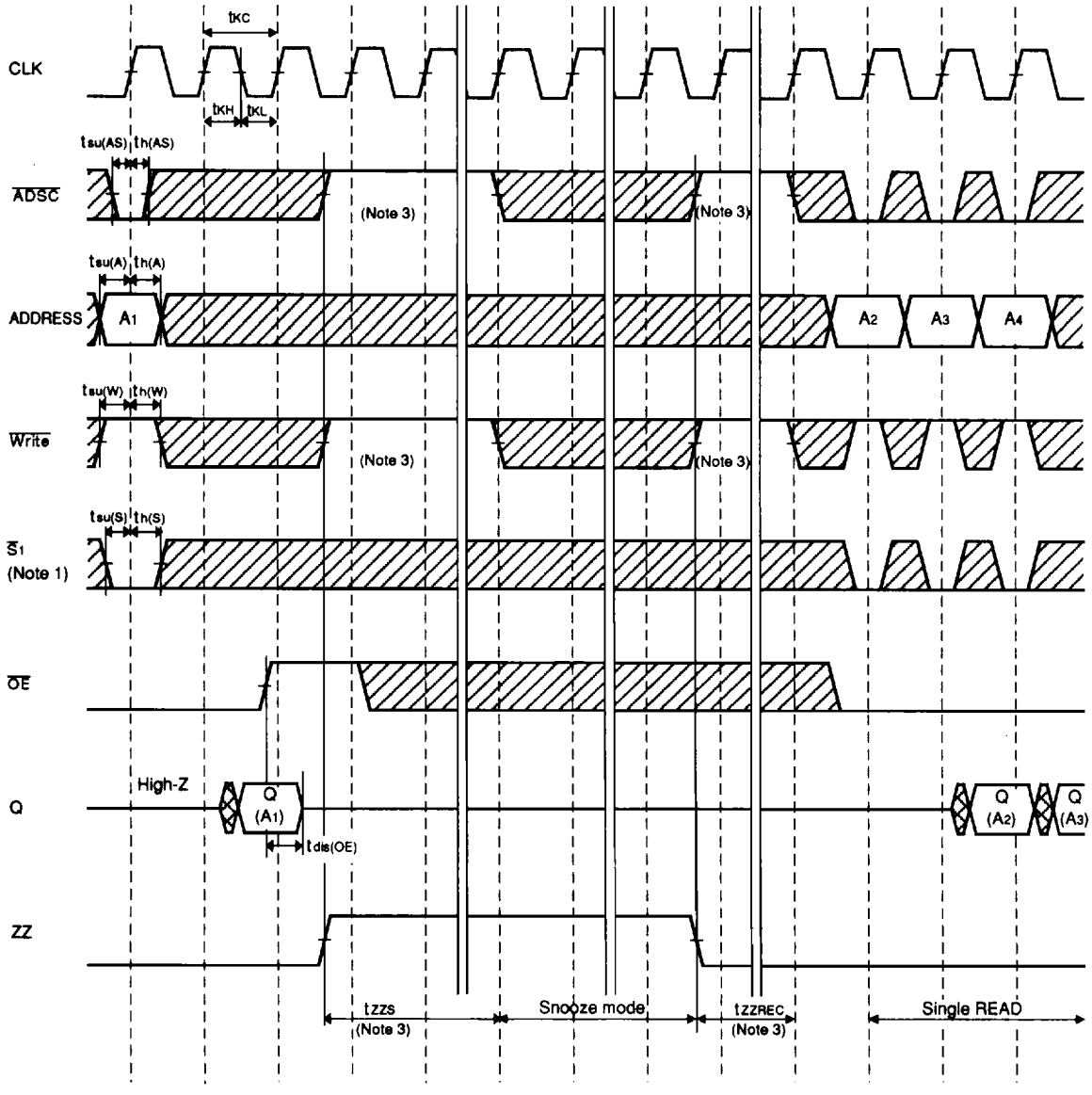


Note 1. Q(A3) refers to output from address A3. Q(A3+1) refers to output from the next internal burst address following A3.
2. $\overline{S2}$ and S2 have timing identical to $\overline{S1}$. On this diagram, when $\overline{S1}$ is LOW, $\overline{S2}$ is LOW and S2 is HIGH. When $\overline{S1}$ is HIGH, $\overline{S2}$ is HIGH and S2 is LOW.
3. ZZ = LOW fix.

DON'T CARE

UNDEFINED

(6) SNOOZE MODE TIMING



Note 1. $\overline{S2}$ and S2 have timing identical to $\overline{S1}$. On this diagram, when $\overline{S1}$ is LOW, $\overline{S2}$ is LOW and S2 is HIGH. When $\overline{S1}$ is HIGH, $\overline{S2}$ is HIGH and S2 is LOW.

2. On this timing chart, $\overline{ADSP}$ = HIGH fix, $\overline{ADV}$ = X.

3. $\overline{ADSP}$ and $\overline{ADSC}$ must not be asserted during tZZS and tZZREC, due to a guarantee of data retention for snooze mode. If synchronous inputs are made combinations of WRITE state during tZZS and tZZREC, memorized data may be destroyed.

DON'T CARE

UNDEFINED