M630x Series
5x7 mm, 3.3/2.5/1.8 Volt, LVPECL/LVDS/CML/CMOS, TCXO/TCVCXO
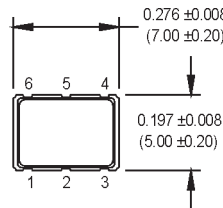
MtronPTI®

QiK Chip™

RoHS Compliant
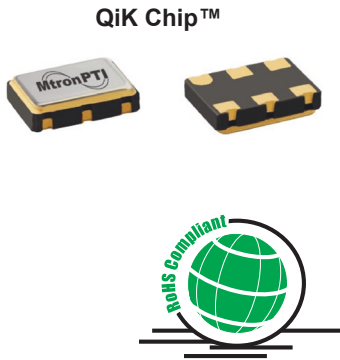
Ordering Information

M630x   1   J   B   V   P   C   XXX.XXXXXX MHz

Product Series
M6300: 3.3 Volt
M6301: 2.5 Volt
M6302: 1.8 Volt

Temperature Range
1: 0°C to +70°C	**3:** -55°C to +105°C *
2: -40°C to +85°C	**4:** -55°C to +125°C
6: -20°C to +70°C	

Stability
G: ± 0.5 ppm	**H:** ± 2.5 ppm
J: ± 1.0 ppm	**L:** ± 4.6 ppm
K: ± 2.0 ppm	**E:** ± 10 ppm

Enable/Disable Function
B: Enable High (Pad 1)	**G:** Enable High (Pad 2)
S: Enable Low (Pad 1)	**M:** Enable Low (Pad 2)
U: No Enable/Disable Function	

Output Type
F: No Voltage Control (TCXO)
V: Voltage Control (VCTCXO)

Output Waveform
P: LVPECL   **L:** LVDS   **M:** CML   **C:** CMOS

Package/Lead Configurations
C: Leadless Ceramic (6 Pad)

Frequency (customer specified)

Features:
- TCXO/TCVCXO Featuring *QiK Chip™* Technology
- Superior Jitter Performance (comparable to SAW based)
- Frequencies from 50 MHz to 1.4 GHz
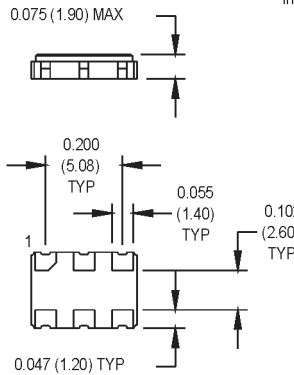- Designed for a short 2 week cycle time

Applications:
- Telecommunications such as SONET / SDH / DWDM / FEC / SERDES / OC-3 thru OC-192
- Wireless base stations / WLAN / Gigabit Ethernet
- Avionic flight controls and military communications

0.276 ±0.008 (7.00 ±0.20)
0.197 ±0.008 (5.00 ±0.20)
6 5 4
1 2 3

ACTUAL SIZE

All dimensions In inches (mm).

0.075 (1.90) MAX

0.200 (5.08) TYP
0.055 (1.40) TYP
0.102 (2.60) TYP
0.047 (1.20) TYP

SUGGESTED SOLDER PAD LAYOUT
0.200 (5.08)
0.071 (1.80)
0.165 (4.20)
0.079 (2.00)

PIN 1 ENABLE
Pad1: Enable/Disable
Pad2: N/C
Pad3: Ground
Pad4: Output Q (LVPECL, LVDS, CML, CMOS)
Pad5: Output Q̄ (LVPECL, LVDS, CML)
Pad6: Vcc

PIN 2 ENABLE
Pad1: N/C, V Control
Pad2: Enable/Disable
Pad3: Ground
Pad4: Output Q (LVPECL, LVDS, CML, CMOS)
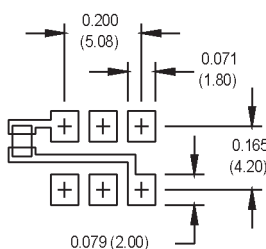Pad5: Output Q̄ (LVPECL, LVDS, CML)
Pad6: Vcc

Temperature vs. Stability

T \ S	G	J	K	H	L
1	A	A	A	A	A
6	N	A	A	A	A
2	N	A	A	A	A
3	N	N	N	N	A
4	N	N	N	N	A

A = Available
N = Contact Factory

Electrical Specifications

Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions/Notes
Frequency Range	F	50		1400	MHz	LVPECL, LVDS, CML (Note 4)
		50		135	MHz	CMOS
Operating Temperature	T_A	See Ordering Information			℃	
Storage Temperature	T_{STG}	-55		+125	℃	
Frequency Stability		See Ordering Information			ppm	See Note 1
Frequency Tolerance at +25℃		-1.0		+1.0	ppm	
Frequency Vs. Aging		-3.0		+ 3.0	ppm	1st year
		-1.0		+ 1.0	ppm	Per year thereafter.
Frequency Vs. Supply Voltage			± 0.4		ppm	5% voltage variation
Frequency Vs. Reflow			± 0.75		ppm	2 reflows max.
Frequency Vs. Load			± 0.2		ppm	5% supply voltage variation
Operating Voltage	$V_{cc}/V_s/V_{dd}$	3.135	3.3	3.465	V	M6300
		2.375	2.5	2.625	V	M6301
		1.71	1.8	1.89	V	M6302
Operating Current	I_{CC}			125	mA	LVPECL
				100	mA	LVDS
				110	mA	CML
				90	mA	CMOS
Rise/Fall Time	Tr/Tf			0.35	ns	PECL, LVPECL, LVDS
				6	ns	CMOS
Logic "1" Level	V_{OH}	V_{CC}-1.02			V	LVPECL
		90% V_{dd}			V	CMOS
Logic "0" Level	V_{OL}			V_{CC}-1.63	V	LVPECL
				10% V_{dd}	V	CMOS
Common Mode Output Voltage	Vcm		1.2		V	LVDS
Symmetry (Duty Cycle)		45		55	%	@ 50% Vdd (CMOS)
		45		55	%	@ 50% of waveform (LVPECL)
		45		55	%	@ 1.25 V (LVDS)
Output Voltage Level		0.7	0.95	1.2	Vp-p	CML
Tuning Range		± 5			ppm	VCTCXO only. See Note 2.
Output Skew			20		ps	LVPECL
			15		ps	CML
			20		ps	LVDS
Output Load		50 Ω to (V_{CC}-2) VDC 100 Ω Differential				See Note 3 LVPECL LVDS, CML
		15			pF	CMOS
Enable/Disable Function		80%				Outputs enabled (Option B or G)
				0.5	V	Outputs disabled
				0.5	V	Outputs enabled (Option S or M)
		80%				Outputs disabled
Phase Noise (Typical)	10 Hz	100 Hz	1 kHz	10 kHz	100 kHz	Offset from carrier
@ 622.080 MHz (LVPECL)	-60	-90	-120	-127	-133	dBc/Hz
@ 100.000 MHz (HCMOS)	-73	-97	-123	-131	-136	dBc/Hz
@ 50.000 MHZ (HCMOS)	-80	-102	-130	-137	-141	dBc/Hz

Environmental

Shock	Per MIL-STD-202, Method 213, Condition C
Vibration	Per MIL-STD-202, Methods 201 & 204
Solderability	Per EIAJ-STD-002
Hermeticity	1 X 10^{-8} atm cc/sec of helium (Crystal only)
Thermal Shock	Per MIL-STD-883, Method 1011, Condition A
Thermal Cycle	Per MIL-STD-883, Method 1010, Condition B

Note 1: Contact factory for less than ± 1ppm frequency stability.
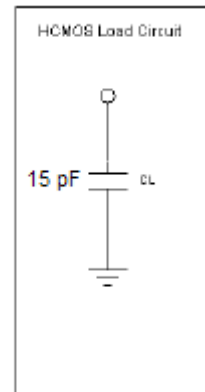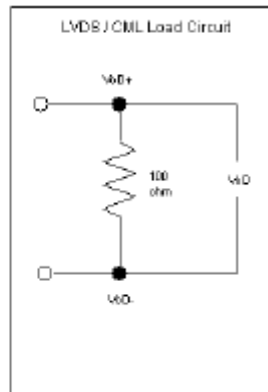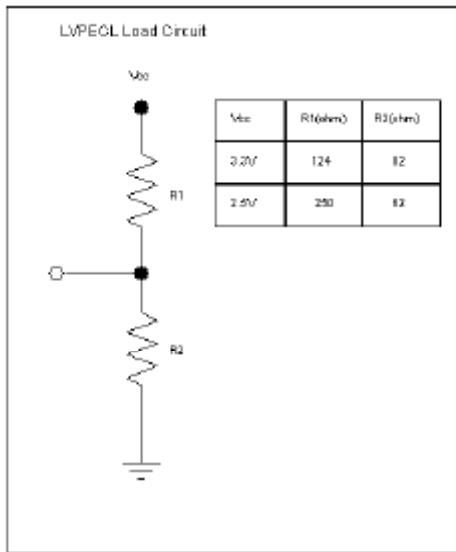Note 2: Contact factory for other Tuning Range options.
Note 3: See Load Circuit Diagram in this data sheet.
Note 4: Contact factory for frequencies over 945 MHz.

Load Circuit Diagrams

LVPECL Load Circuit

Vcc	R1(ohm)	R3(ohm)
3.3V	124	82
2.5V	250	62

Vcc

R1

R3

LVDS / CML Load Circuit

Vod+

100 ohm

Vod

Vod-

HCMOS Load Circuit

15 pF   CL

Lead Free Solder Profile

RAMP-UP
3°C/SECOND MAX.

CRITICAL TEMPERATURE ZONE

RAMP-DOWN
6°C/SECOND

TEMPERATURE

260°C

217°C

200°C

150°C

PREHEAT
180 SECONDS MAX.

90 SECONDS MAX.

8 MINUTES MAX.

260°C MAX. FOR 10 SECONDS MAX.

TIME