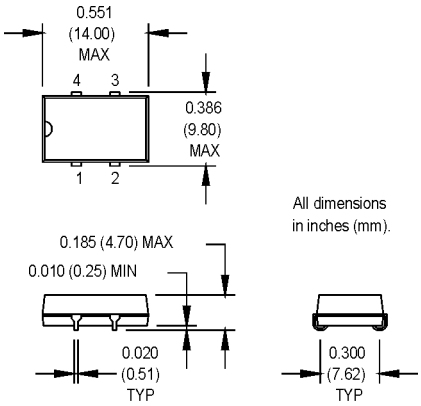
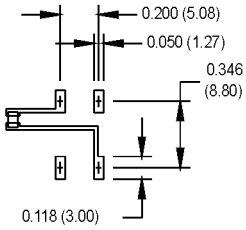
MHR Series
9x14 mm, 5.0 Volt, HCMOS/TTL, Clock Oscillators



SUGGESTED SOLDER PAD LAYOUT



NOTE: A capacitor of value 0.01 µF or greater between Vdd and Ground is recommended.

Pin Connections

PIN	FUNCTION
1	N/C or Tri-state
2	Ground
3	Output
4	+Vdd

Ordering Information

00.0000 MHz

MHR 1 3 T A J

Product Series

Temperature Range
- **1:** 0°C to +70°C
- **2:** -40°C to +85°C
- **6:** -20°C to +70°C

Stability
- **3:** ±100 ppm
- **4:** ±50 ppm
- **6:** ±25 ppm
- ***8:** ±20 ppm

Output Type
- **F:** Fixed
- **T:** Tristate

Symmetry/Logic Compatibility
- **A:** 40/60 TTL/HCMOS (Standard for 1.000 to 50.000 MHz)
- ***B:** 45/55 TTL
- ***C:** 45/55 HCMOS
- **F:** 40/60 TTL (50.001 to 67.000 MHz)
- **G:** 40/60 HCMOS (50.001 to 80.000 MHz)

Package/Lead Configurations
- **J:** J Lead

Frequency (customer specified)

* Consult factory regarding availability of "B" and "C" symmetry codes, and "8" stability code.

	PARAMETER	Symbol	Min.	Typ.	Max.	Units	Condition
Electrical Specifications	**Frequency Range**	**F**	1		80	MHz	
	Frequency Stability	**ΔF/F**	(See Ordering Information)				
	Operating Temperature	**TA**	(See Ordering Information)				
	Storage Temperature	**Ts**	-55		+125	°C	
	Input Voltage	**Vdd**	4.5	5.0	5.5	V	
	Input Current	**Idd**			30	mA	1.000 to 40.000 MHz
					50	mA	40.001 to 50.000 MHz
					55	mA	50.001 to 80.000 MHz
	Symmetry (Duty Cycle) [1]		(See Ordering Information)				½ Vdd and 1.4 V
	Load [2]		10 TTL or 50 pF				1.000 to 50.000 MHz
			5 TTL or 30 pF				50.001 to 67.000 MHz
			15 pF				67.001 to 80.000 MHz
	Rise/Fall Time [3]	**Tr/Tf**					
	1.000 to 40.000 MHz				10	ns	
	40.001 to 50.000 MHz				8	ns	
	50.001 to 80.000 MHz				6	ns	
	Logic "1" Level	**Voh**	90% Vdd			V	HCMOS Load
			Vdd -0.5			V	TTL Load
	Logic "0" Level	**Vol**			10% Vdd	V	HCMOS Load
					0.5	V	TTL Load
	Cycle to Cycle Jitter			15	50	ps RMS	1 Sigma
	Tri-State Function		Input Logic "1" or floating; output active				
			Input Logic "0"; output to high-Z				
Environmental							
	Mechanical Shock	Per MIL-STD-202, Method 213, Condition C					
	Vibration	Per MIL-STD-202, Method 201 & 204					
	Reflow Solder Conditions	See "Figure 2" on page 147					
	Solderability	Per EIAJ-STD-002					

1. Symmetry is measured at 1.4 V with TTL load, and at 50% Vdd with HCMOS load.
2. TTL load - See load circuit diagram #1 on page 148. HCMOS load - See load circuit diagram #2 on page 148.
2. Rise/fall times are measured between 0.5 V and 2.4 V for TTL load, and between 10% and 90% Vdd for HCMOS load.

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