

MSM5299A

80-DOT SEGMENT DRIVER

GENERAL DESCRIPTION

The MSM5299A is a dot matrix LCD segment driver LSI which is fabricated by CMOS low power metal gate technology. This LSI consists of an 80-bit bidirectional shift register, 80-bit latch, 80-bit level shifter and 80-bit 4-level driver.

It receives the display data, which consists of 4-bit parallel, from the LCD controller LSI, then outputs the LCD driving waveform to the LCD.

The MSM5299A has the power down function which enables the MSM5299A's power consumption low.

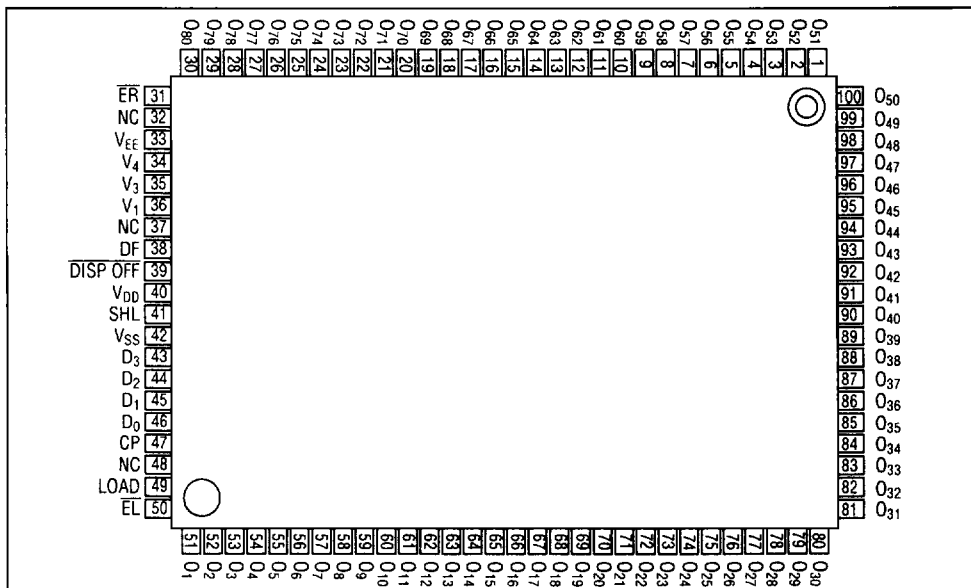
The MSM5299A can drive a variety of LCD panels because the bias voltage, which determines the LCD driving voltage, can be optionally supplied from the external source.

FEATURES

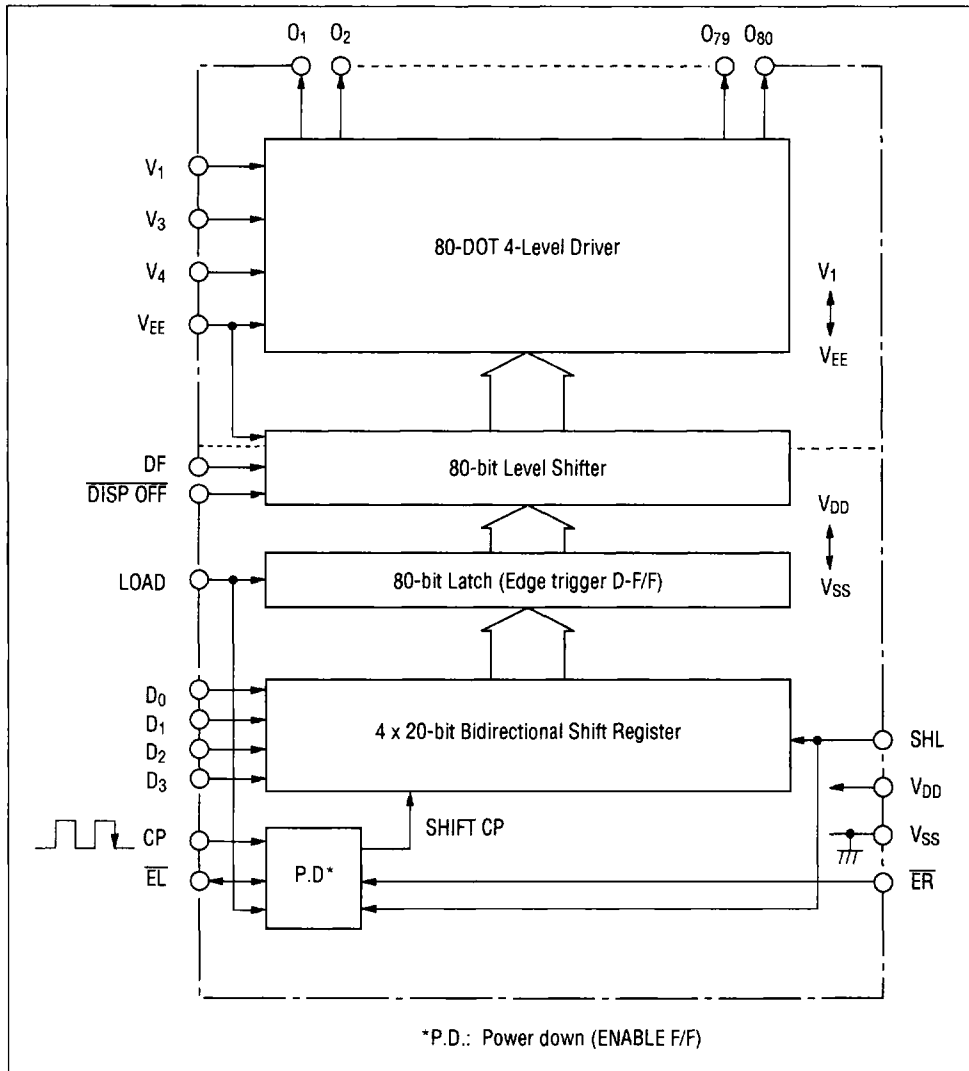
- Supply voltage : 4.5 ~ 5.5V
- LCD driving voltage : 8 ~ 28V
- Applicable LCD duty : 1/64 ~ 1/256
- LCD Output : 80
- Bias voltage can be supplied externally
- Power down function
- 4-bit parallel data processing
- Can be interfaced with the LCD controller LSI MSM6255
- 100 pin plastic QFP (QFP100-P-1420-K)
- 100 pin -V1 plastic QFP (QFP100-P-1420-V1K)

PIN CONFIGURATION (TOP VIEW)

(Top view) 80 pin plastic QFP



FUNCTIONAL BLOCK DIAGRAM



TRUTH TABLE

DF	Latched data	DISP OFF	Display data output level (O ₁ ~O ₈₀)
L	L	H	V ₃
L	H	H	V ₁
H	L	H	V ₄
H	H	H	V _{EE}
X	X	L	V ₁

ELECTRICAL CHARACTERISTICS

• Absolute Maximum Ratings

Parameter	Symbol	Condition	Rating	Unit
Supply Voltage (1)	V_{DD}	$T_a = 25^\circ\text{C}$	-0.3 ~ 6	V
Supply Voltage (2)	$V_{DD} - V_{EE}^{*1}$	$T_a = 25^\circ\text{C}$	0 ~ 30	V
Input Voltage	V_i	$T_a = 25^\circ\text{C}$	-0.3 ~ $V_{DD}+0.3$	V
Storage Temperature	T_{stg}	-	-55 ~ +150	$^\circ\text{C}$

*1 $V_1 > V_3 > V_4 > V_{EE}$, $V_1 \leq V_{DD}$

• Operating Range

Parameter	Symbol	Condition	Rating	Unit
Supply Voltage (1)	V_{DD}	-	4.5 ~ 5.5	V
Supply Voltage (2)	$V_{DD} - V_{EE}^{*1}$	-	8 ~ 28	V
Operating Temperature	T_{OP}	-	-20 ~ +85	$^\circ\text{C}$

*1 $V_1 > V_3 > V_4 > V_{EE}$, $V_1 \leq V_{DD}$

• DC Characteristics

(V_{DD} = 5V ± 10%, T_a = -20 ~ 85°C)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
"H" Input Voltage	V _{IH} *1	-	0.8V _{DD}	-	-	V
"L" Input Voltage	V _{IL} *1	-	-	-	0.2V _{DD}	V
"H" Input Current	I _{IH} *1	V _{IH} = V _{DD} V _{DD} = 5.5V	-	-	1	μA
"L" Input Current	I _{IL} *1	V _{IL} = 0V V _{DD} = 5.5V	-	-	-1	μA
"H" Output Voltage	V _{OH} *2	I _O = -0.2mA V _{DD} = 4.5V	V _{DD} - 0.4	-	-	V
"L" Output Voltage	V _{OL} *2	I _O = 0.2mA V _{DD} = 4.5V	-	-	0.4	V
ON Resistance	R _{ON} *4	V _{DD} - V _{EE} = 23V *3 V _N - V _O = 0.25V V _{DD} = 4.5V	-	2	4	kΩ
Stand-by Current Consumption	I _{DD} SBY	CP = 1MHz V _{DD} = 5.5V V _{DD} - V _{EE} = 26V, No load *5	-	-	200	μA
Current Consumption (1)	I _{DD1}	CP = 1MHz V _{DD} = 5.5V V _{DD} - V _{EE} = 26V, No load *6	-	-	3	mA
Current Consumption (2)	I _v	CP = 1MHz V _{DD} = 5.5V V _{DD} - V _{EE} = 26V, No load *7	-	-	±100	μA
Input Capacitance	C _i	f = 1MHz	-	5	-	pF

*1 Applicable to \overline{LOAD} , CP, D₀ ~ D₃, \overline{EL} , \overline{ER} , SHL, DF, $\overline{DISP\ OFF}$ terminals

*2 Applicable to \overline{EL} , \overline{ER} terminals.

$$*3 V_N = V_{DD} - V_{EE}, V_3 = \frac{13}{15}(V_{DD} - V_{EE}), V_2 = \frac{2}{15}(V_{DD} - V_{EE}), V_{DD} = V_1$$

*4 Applicable to O₁ ~ O₈₀ terminals.

*5 Display data 1010 DF = 40 Hz, Current from V_{DD} to V_{SS} when the display data is not processing.

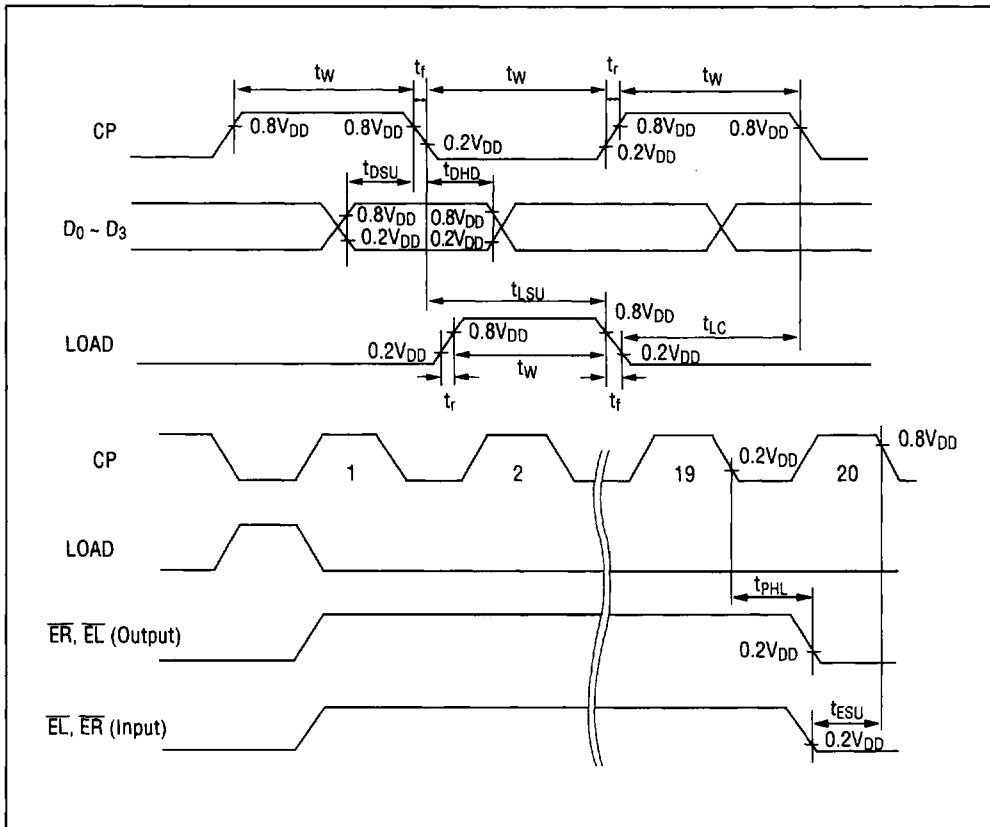
*6 Display data 1010 DF = 40 Hz, Current from V_{DD} to V_{SS} when the display data is processing.

*7 Display data 1010 DF = 40 Hz, Current on V₁, V₃, V₄ and V_{EE} terminals.

• Switching Characteristics

($V_{DD} = 5V \pm 10\%$, $T_a = -20 \sim 75^\circ C$, $C_L = 15pF$)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
MAX. Clock Frequency	f_{CP}	DUTY=50%	3.4	-	-	MHZ
Clock Load Pulse Width	t_w	-	100	-	-	ns
Clock Pulse Rising/Falling Time	t_r, t_f	-	-	-	50	ns
Data Set-up Time	t_{DSU}	-	50	-	-	ns
Data Hold Time	t_{DHD}	-	80	-	-	ns
Load Set-up Time	t_{LSU}	-	90	-	-	ns
Load → Clock Time	t_{LC}	-	200	-	-	ns
Propagation Delay Time	t_{PHL}	-	-	-	224	ns
$\overline{ER}, \overline{EL}$ Set-up Time	t_{ESU}	-	70	-	-	ns



- **D₀, D₁, D₂, D₃**

Display data input pins for 4-bit parallel shift register and it is input synchronized with the clock pulse. The combination of D₀ ~ D₃ level, DF signal, display data output level and the display on the LCD panel is described on the table below.

D ₀ ~ D ₃	DF	Display data output level	Display on the LCD
L	L	V ₃	OFF
H	L	V ₁	ON
L	H	V ₄	OFF
H	H	V _{EE}	ON

- **LOAD**

The signal for latching the shift register contents is input from this pin.

- **DF**

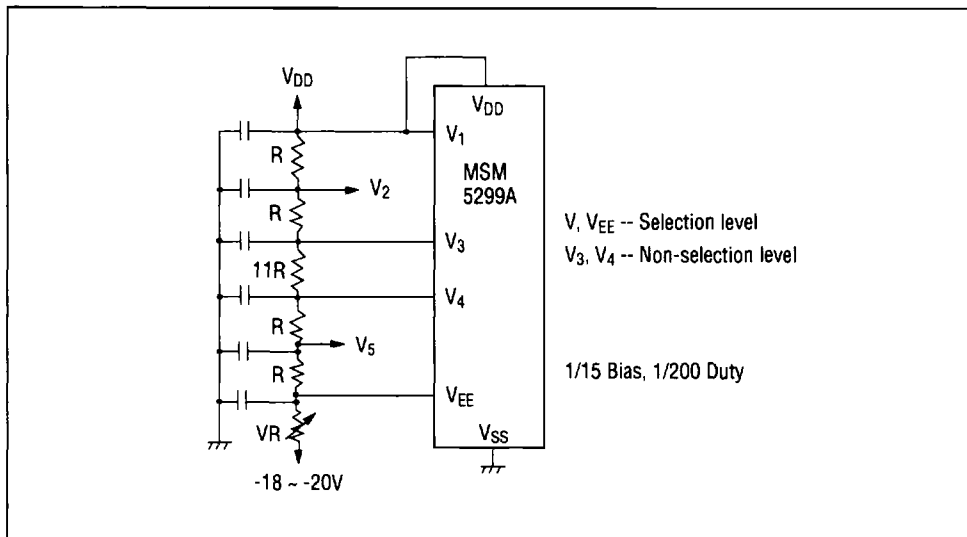
Alternate signal input pin for LCD driving. Frame inversion signal is input to this terminal.

- **V_{DD}, V_{SS}**

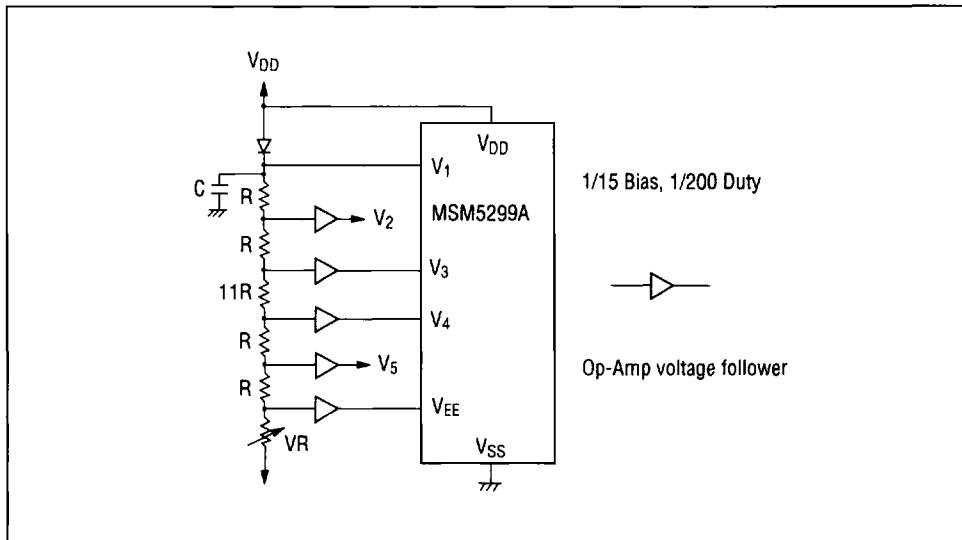
Supply voltage pins, V_{DD} should be 4.5 ~ 5.5V. V_{SS} is a ground pin (V_{SS} = 0V)

- **V₁, V₃, V₄, V_{EE}**

Bias supply voltage pin to drive the LCD. Bias voltage divided by the resistance is usually used as supply voltage source. The figure below shows the case when bias voltage, which determines the LCD driving voltage, is supplied from the external source. V₁ is not necessarily connected with V_{DD}.

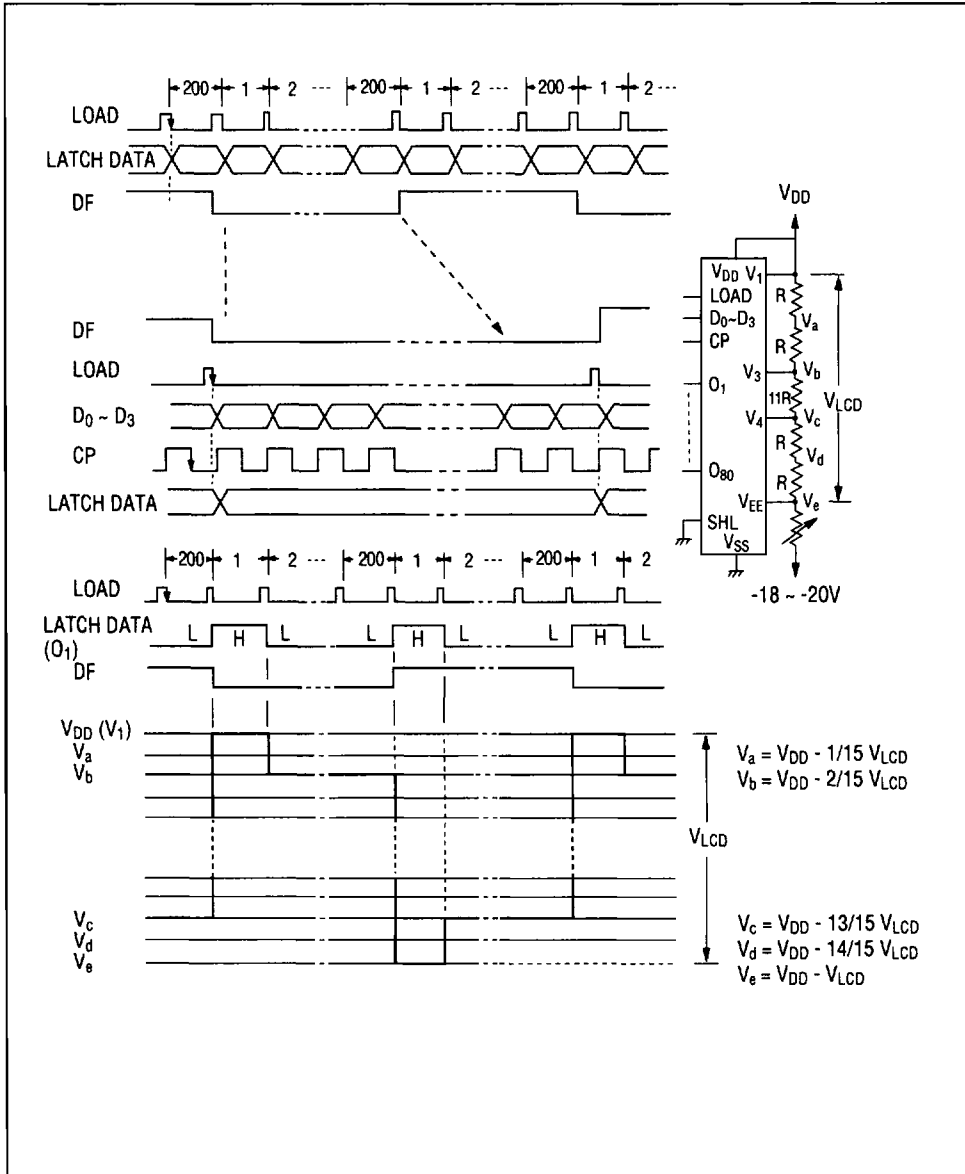


The figure below shows the case when the bias voltage is supplied by using Op-Amps, which enables the bias source low impedance and low power consumption.



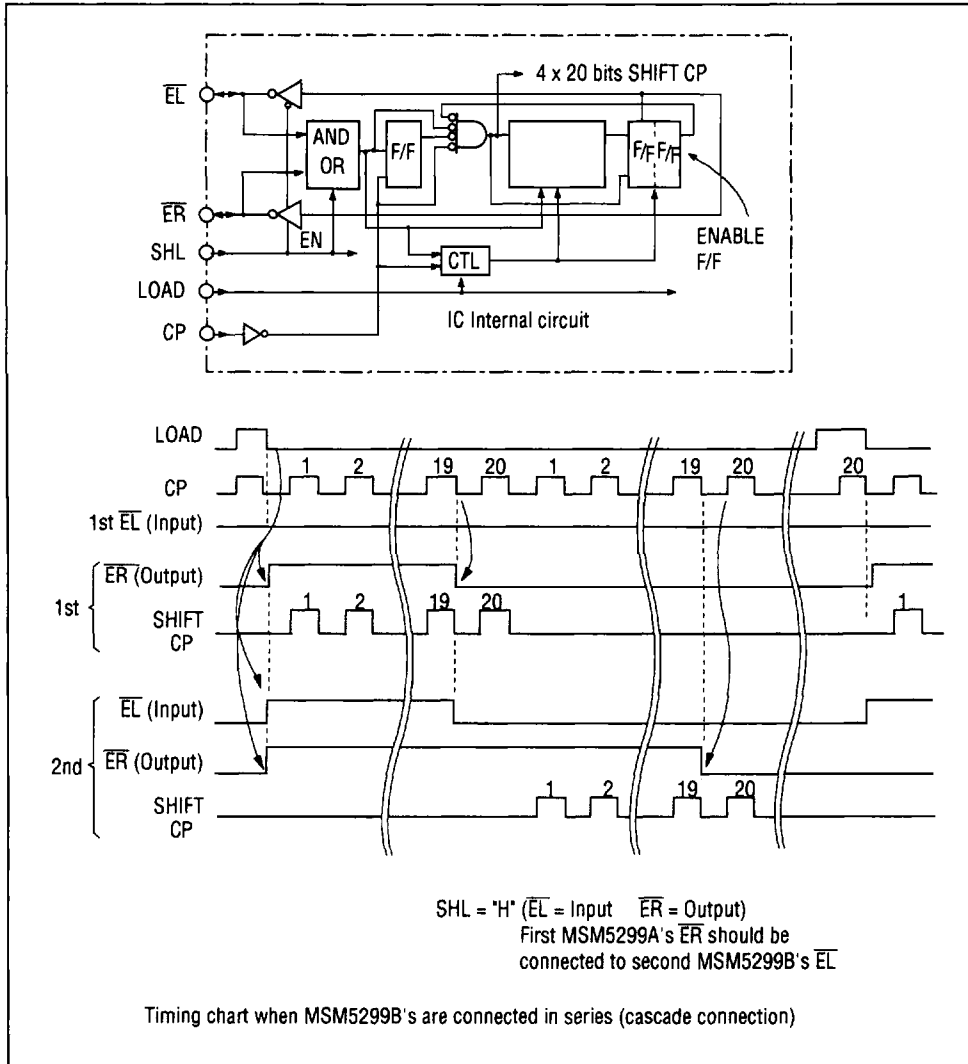
- O₁ ~ O₈₀**
 Display data output pin which corresponds to the respective latch contents. One of V₁, V₃, V₄ and V_{EE} is selected as a display driving voltage source according to the combination of the latched data level and DF signal. (Refer to the truth table).
- DISP OFF**
 Control input pin for display data output level (O₁ ~ O₈₀). V₁ level is output from O₁ ~ O₈₀ pins during "L" level input.
 LCD becomes non-visual by V₁ level output from every output of segment drivers and every output of common drivers.

TIMING CHART (1/200 duty, 1/15 Bias)



POWER SAVE FUNCTION

When more than two MSM5299As are being connected in series, cascade connection, power down function of MSM5299A can be utilized using the ENABLE F/F (flip flop circuit) in individual MSM5299As. (Regarding the internal circuit configuration of MSM5299A, refer to the figure below.) The display data is processed only in the MSM5299A, the ENABLE F/F of which is being activated by setting its \overline{ER} and \overline{EL} at low level, while the display data is not processed in the MSM5299A, the ENABLE F/F of which is not being activated and the low power consumption condition ($I_{DD\ SBY}$) is being held. The activated condition of this ENABLE F/F is being shifted to next MSM5299AGS one after another so that the ENABLE F/F of only one MSM5299A out of the cascade connected MSM5299As should be being activated.



APPLICATION CIRCUIT

