MN40175B/MN40175BS

Quad D-Type Flip-Flop

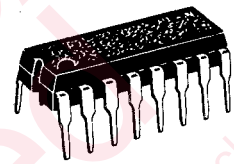
■ Outline

The MN40175B/S consists of four biult-in circuits of D-type flip-flops having common CP and $\overline{MR}$ pins.

The D_n input is transmitted to the O_n output at the rise of the clock input. When the level of the $\overline{MR}$ input is set to "L", all the four circuits of the flip-flops can be simultaneously reset.

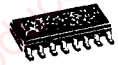
This MN40175B/S is equivalent to Motorola's MC14175B.

P-3



16-pin plastic DIL package

P-4



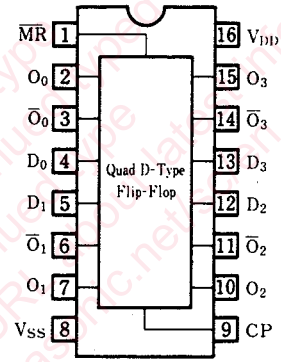
16-pin PANAFLAT package (SO-16D)

■ Truth Table

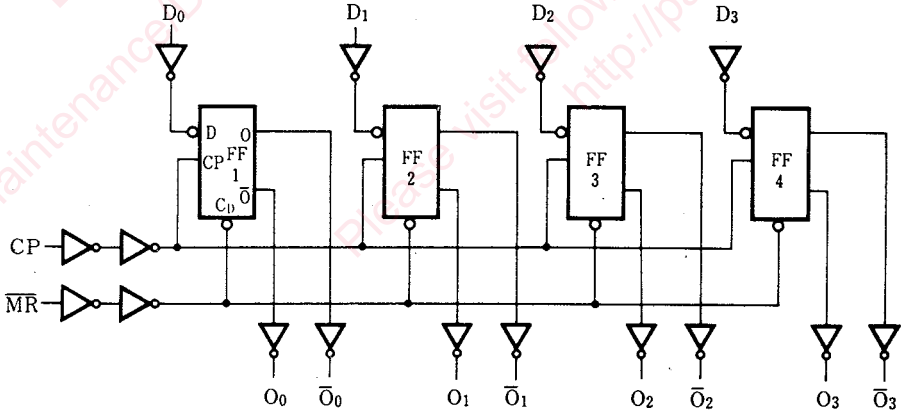
Input			Output	
CP	D	$\overline{MR}$	O	$\overline{O}$
↑	H	H	H	L
↑	L	H	L	H
↓	×	H	No Change	No Change
×	×	L	L	H

Note) ×: don't care

Pin Configuration



■ Logic Diagram



■ Absolute Maximum Ratings (Ta=25°C)

Item		Symbol	Rating	Unit
Supply voltage		V_{DD}	−0.5~+18	V
Input voltage		V_I	−0.5~V_{DD}+0.5*	V
Output pin voltage		V_O	−0.5~V_{DD}+0.5*	V
Peak input · output pin current		$\pm I_I$	max. 10	mA
Power dissipation (per package)	Ta=−40~+60°C	P_D	max. 400	mW
	Ta=+60~+80°C		Decrease to 200mW at the rate of 8mW/°C	
Power dissipation (per output pin)		P_D	max. 100	mW
Operating ambient temperature		T_{opr}	−40~+85	°C
Storage temperature		T_{stg}	−65~+150	°C

* V_{DD}+0.5V should be lower than 18V.

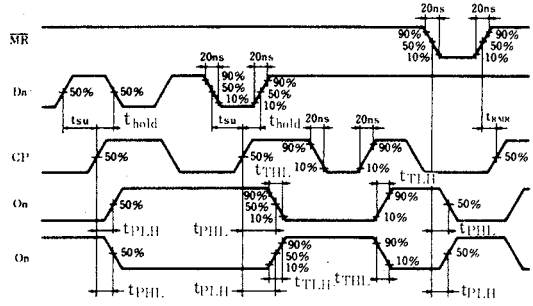
■ DC Characteristics (V_{SS}=0V)

Item	V_{DD} (V)	Symbol	Condition		Ta=−40°C min.	Ta=−40°C max.	Ta=25°C min.	Ta=25°C max.	Ta=85°C min.	Ta=85°C max.	Unit
Static supply current	5	I_{DD}	V_I=V_{SS} or V_{DD}		—	20	—	20	—	150	μA
	10				—	40	—	40	—	300	
	15				—	80	—	80	—	600	
Output voltage low level	5	V_{OL}	V_I=V_{SS} or V_{DD}		—	0.05	—	0.05	—	0.05	V
	10		$\|I_O\|$<1μA		—	0.05	—	0.05	—	0.05	
	15				—	0.05	—	0.05	—	0.05	
Output voltage high level	5	V_{OH}	V_I=V_{SS} or V_{DD}		4.95	—	4.95	—	4.95	—	V
	10		$\|I_O\|$<1μA		9.95	—	9.95	—	9.95	—	
	15				14.95	—	14.95	—	14.95	—	
Input voltage low level	5	V_{IL}	$\|I_O\|$<1μA	V_O=0.5V or 4.5V	—	1.5	—	1.5	—	1.5	V
	10			V_O=1V or 9V	—	3	—	3	—	3	
	15			V_O=1.5V or 13.5V	—	4	—	4	—	4	
Input voltage high level	5	V_{IH}	$\|I_O\|$<1μA	V_O=0.5V or 4.5V	3.5	—	3.5	—	3.5	—	V
	10			V_O=1V or 9V	7	—	7	—	7	—	
	15			V_O=1.5V or 13.5V	11	—	11	—	11	—	
Output current low level	5	I_{OL}	V_O=0.4V, V_I=0 or 5V		0.52	—	0.44	—	0.36	—	mA
	10		V_O=0.5V, V_I=0 or 10V		1.3	—	1.1	—	0.9	—	
	15		V_O=1.5V, V_I=0 or 15V		3.6	—	3	—	2.4	—	
Output current high level	5	$-I_{OH}$	V_O=4.6V, V_I=0 or 5V		0.52	—	0.44	—	0.36	—	mA
	10		V_O=9.5V, V_I=0 or 10V		1.3	—	1.1	—	0.9	—	
	15		V_O=13.5V, V_I=0 or 15V		3.6	—	3	—	2.4	—	
Output current high level	5	$-I_{OH}$	V_O=2.5V, V_I=0 or 5V		1.7	—	1.4	—	1.1	—	mA
Input leakage current	15	$\pm I_I$	V_I=0 or 15V		—	0.3	—	0.3	—	1	μA

■ Switching Characteristics (Ta=25°C, V_{SS}=0V, C_L=50pF)

Item	V_{DD}(V)	Symbol	min.	typ.	max.	Unit
Output rise time	5	t_{TLH}	—	60	180	ns
	10		—	30	90	
	15		—	20	60	
Output fall time	5	t_{THL}	—	60	180	ns
	10		—	30	90	
	15		—	20	60	
Propagation time CP→On, $\overline{On}$ (H→L)	5	t_{PHL}	—	80	240	ns
	10		—	35	105	
	15		—	25	75	
Propagation time CP→On, $\overline{On}$ (L→H)	5	t_{PLH}	—	70	210	ns
	10		—	30	90	
	15		—	25	75	
Propagation time $\overline{MR}$→On (H→L)	5	t_{PHL}	—	75	225	ns
	10		—	30	90	
	15		—	25	75	
Propagation time $\overline{MR}$→$\overline{On}$ (L→H)	5	t_{PLH}	—	70	210	ns
	10		—	30	90	
	15		—	25	75	
Set-up time Dn→CP	5	t_{su}	—	30	90	ns
	10		—	10	30	
	15		—	5	15	
Hold time Dn→CP	5	t_{hold}	—	−5	30	ns
	10		—	0	15	
	15		—	0	15	
Minimum clock pulse width	5	t_{WCPL}	—	45	135	ns
	10		—	15	45	
	15		—	10	30	
Minimum reset pulse width	5	t_{WMRL}	—	40	120	ns
	10		—	15	45	
	15		—	10	30	
Reset recovery time	5	t_{RMR}	—	−30	0	ns
	10		—	−20	0	
	15		—	−15	0	
Maximum clock frequency	5	f_{max}	5	11	—	MHz
	10		15	30	—	
	15		20	45	—	
Input capacitance		C_I	—	—	7.5	pF

• Switching waveforms



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