HARRIS

2N6786

August 1991

N-Channel Enhancement-Mode Power MOS Field-Effect Transistor

Features

- 1.25A, 400V
- $r_{DS(on)} = 3.6\Omega$
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance
- Majority Carrier Device

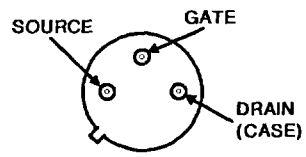
Description

The 2N6786 is an n-channel enhancement-mode silicon-gate power MOS field-effect transistor designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. This type can be operated directly from integrated circuits.

The 2N6786 is supplied in the JEDEC TO-205AF (Low Profile TO-39) metal package.

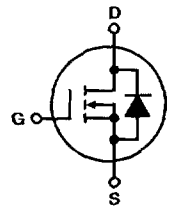
Package

TO-205AF
BOTTOM VIEW



Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



4 N-CHANNEL POWER MOSFETs

Absolute Maximum Ratings (T_C = +25°C) Unless Otherwise Specified

		2N6786	UNITS
Drain-Source Voltage	V_{DS}	400*	V
Drain-Gate Voltage (R_{GS} = 20kΩ)	V_{DGR}	400*	V
Continuous Drain Current			
T_C = +25°C	I_D	1.25*	A
T_C = +100°C	I_D	0.8*	A
Pulsed Drain Current	I_{DM}	5.5*	A
Gate-Source Voltage	V_{GS}	±20*	V
Continuous Source Current	I_S	1.25*	A
Pulse Source Current	I_{SM}	5.5*	A
Maximum Power Dissipation			
T_C = +25°C (See Figure 14)	P_D	15*	W
Above T_C = +25°C, Derate Linearly (See Figure 14)		0.12*	W/°C
Inductive Current, Clamped (L = 100μH)	I_{LM}	5.5	A
Operating and Storage Junction Temperature Range	T_J, T_{STG}	-55 to +150*	°C
Maximum Lead Temperature for Soldering (0.063" (1.6mm) from case for 10s)	T_L	300*	°C

*JEDEC registered values

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

File Number 2207.1

ELECTRICAL CHARACTERISTICS at T_C = 25°C (Unless Otherwise Specified)

CHARACTERISTIC		TEST CONDITIONS	LIMITS			UNITS
			Min.	Typ.	Max.	
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS} = 0 V, I_D = 0.25 mA	400*	—	—	V
Gate Threshold Voltage	$V_{GS(th)}$	V_{GS} = V_{DS}, I_D = 0.5 mA	2.0*	—	4.0*	V
Gate-Source Leakage Forward	I_{GSS}	V_{GS} = 20 V, V_{DS} = 0 V	—	—	100*	nA
Gate-Source Leakage Reverse	I_{GSS}	V_{GS} = -20 V, V_{DS} = 0 V	—	—	100*	nA
Zero-Gate Voltage Drain Current	I_{DSS}	V_{DS} = 400 V, V_{GS} = 0 V	—	—	250*	μA
		V_{DS} = 320 V, V_{GS} = 0 V, T_C = 125°C	—	—	1000*	μA
On-State Voltage[a]	$V_{DS(on)}$	V_{GS} = 10 V, I_D = 1.25 A	—	—	4.5*	V
Static Drain-Source On-State Resistance[a]	$r_{DS(on)}$	V_{GS} = 10 V, I_D = 0.8 A, T_A = 25°C	—	3.3	3.6*	Ω
		V_{GS} = 10 V, I_D = 0.8 A, T_A = 125°C	—	—	7.92*	Ω
Diode Forward Voltage[a]	V_{SD}	T_C = 25°C, I_S = 1.25 A, V_{GS} = 0 V	0.6*	—	1.4*	V
Forward Transconductance[a]	g_{fs}	V_{DS} = 5 V, I_D = 0.8 A	0.7*	1.2	2.1*	S(℧)
Input Capacitance	C_{iss}	V_{GS} = 0 V, V_{DS} = 25 V, f = 1 MHz See Fig. 10	60*	135	200*	pF
Output Capacitance	C_{oss}		15*	35	50*	pF
Reverse Transfer Capacitance	C_{rss}		2*	8	15*	pF
Turn-On Delay Time	$t_{d(on)}$	V_{DD} ≅ 170 V, I_D = 0.8 A, Z_O = 50 Ω See Fig. 15. (MOSFET switching times are essentially independent of operating temperature.)	—	—	15*	ns
Rise Time	t_r		—	—	20*	ns
Turn-Of Delay Time	$t_{d(off)}$		—	—	35*	ns
Fall Time	t_f		—	—	30*	ns
Safe Operating Area	SOA	V_{DS} = 200 V, I_D = 75 mA, See Fig. 16.	15	—	—	W
		V_{DS} = 12 V, I_D = 1.25 A, See Fig. 16.	15	—	—	W

THERMAL RESISTANCE

Junction-to-Case	$R_{\theta JC}$		—	—	8.33*	°C/W
Junction-to-Ambient	$R_{\theta JA}$	Free Air Operation	—	—	175	°C/W

SOURCE-DRAIN DIODE SWITCHING CHARACTERISTICS (TYPICAL)

Reverse Recovery Time	t_{rr}	T_J=150°C, I_F=1.25 A, di_F/dt=100 A/μs	380	ns
Reverse Recovered Charge	Q_{RR}	T_J=150°C, I_F=1.25 A, di_F/dt=100 A/μs	2.7	μC
Forward Turn-On Time	t_{on}	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L_S + L_D.		

*JEDEC registered value.

[a]Pulse Test: Pulse width ≤ 300 μs, duty cycle ≤ 2%.

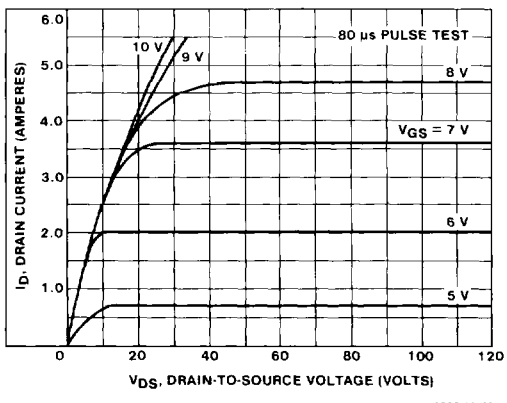


Fig. 1 - Typical output characteristics.

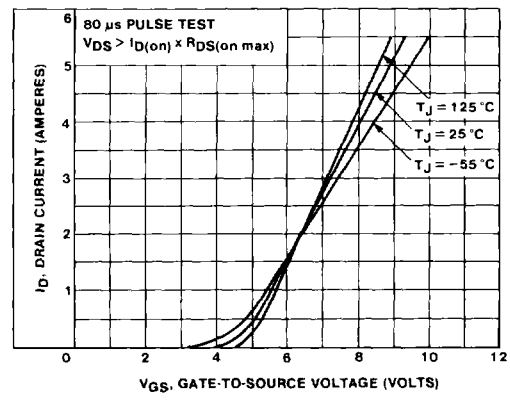


Fig. 2 - Typical transfer characteristics.

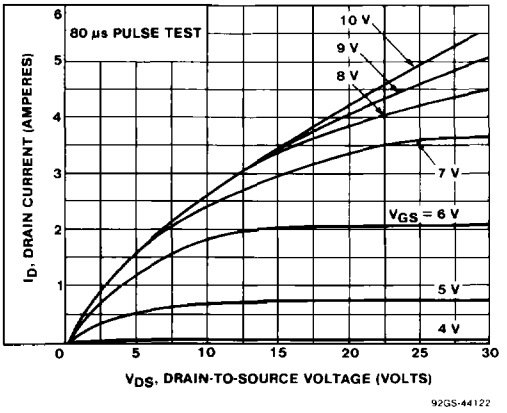


Fig. 3 - Typical saturation characteristics.

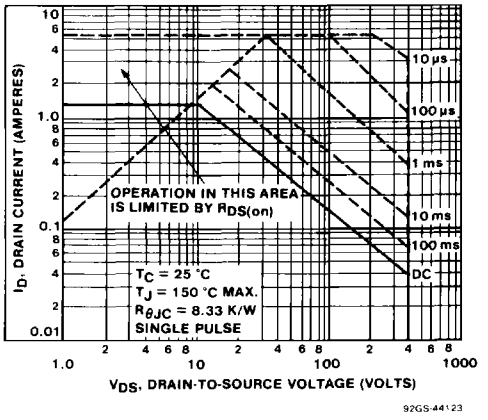


Fig. 4 - Maximum safe operating area.

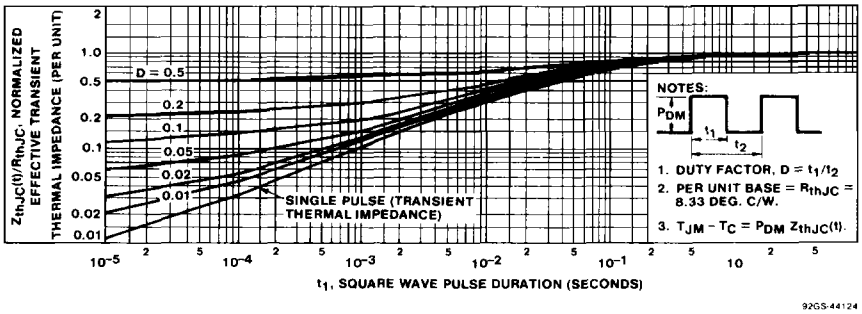


Fig. 5 - Maximum effective transient thermal impedance, junction-to-case vs. pulse duration.

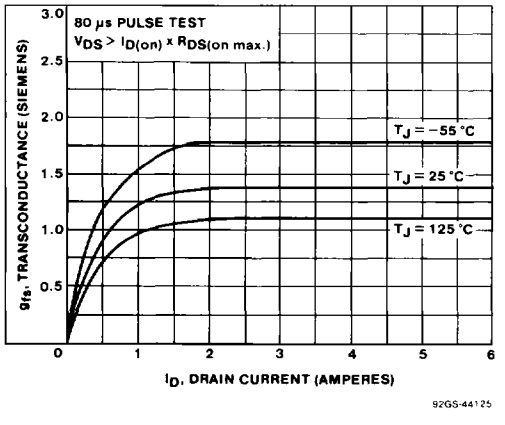


Fig. 6 - Typical transconductance vs. drain current.

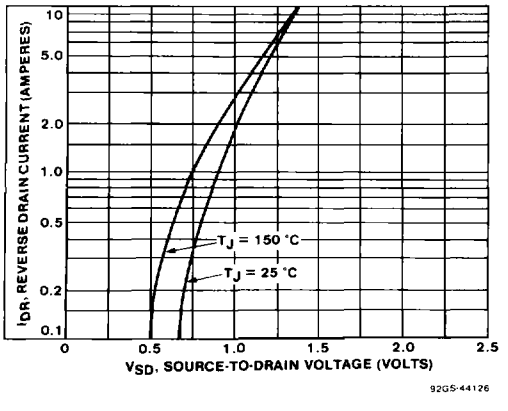


Fig. 7 - Typical source-drain diode forward voltage.

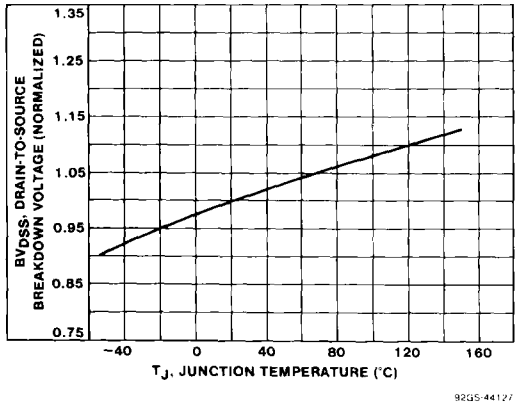


Fig. 8 - Breakdown voltage vs. temperature.

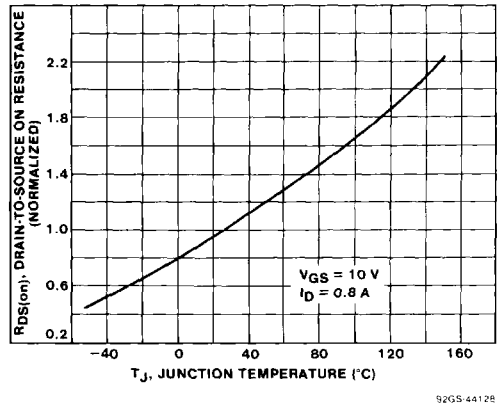


Fig. 9 - Normalized on-resistance vs. temperature.

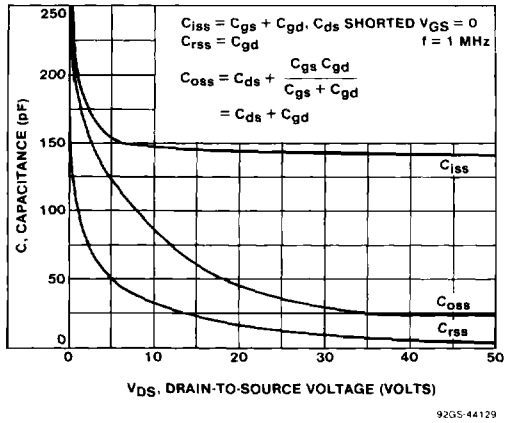


Fig. 10 - Typical capacitance vs. drain-to-source voltage.

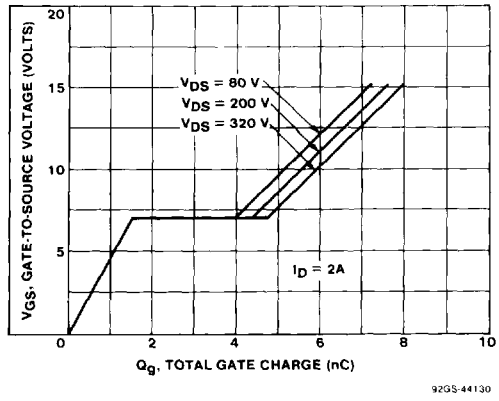


Fig. 11 - Typical gate charge vs. gate-to-source voltage.

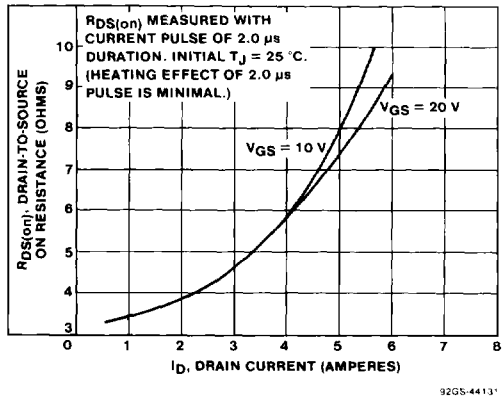


Fig. 12 - Typical on-resistance vs. drain current.

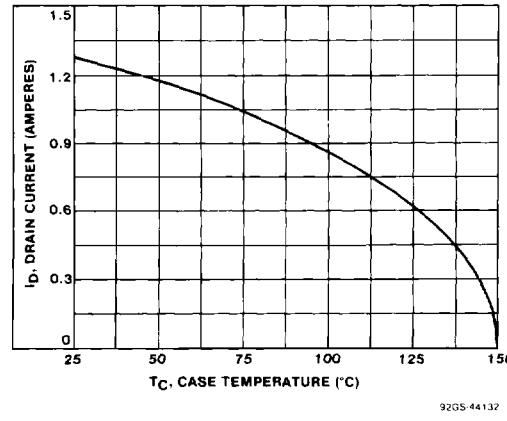


Fig. 13 - Maximum drain current vs. case temperature.

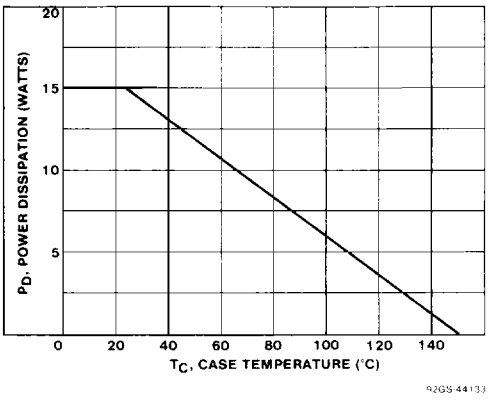
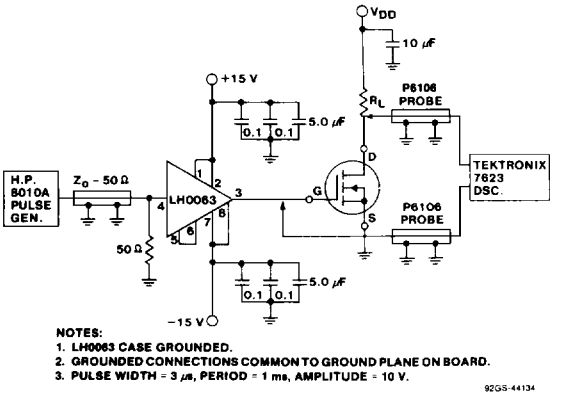


Fig. 14 - Power vs. temperature derating curve.



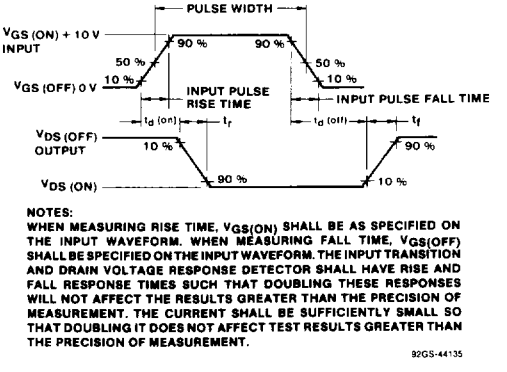
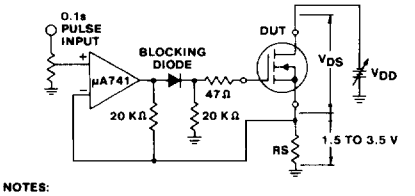


Fig. 15 - Switching time test circuit.



NOTES:
1. SET V_{DS} TO THE VALUE SPECIFIED UNDER DETAILS USING A 0.1-s PULSE WIDTH WITH A MINIMUM OF 1 MINUTE BETWEEN PULSES. INCREASE V_{GS} UNTIL THE SPECIFIED VALUE OF I_D AND V_{DS} ARE OBTAINED. CASE TEMPERATURE = 25°C.
2. SELECT R_S SUCH THAT $I_D \cdot R_S = 2.5 \pm 1$ Vdc.

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Fig. 16 - Safe operating test circuit.