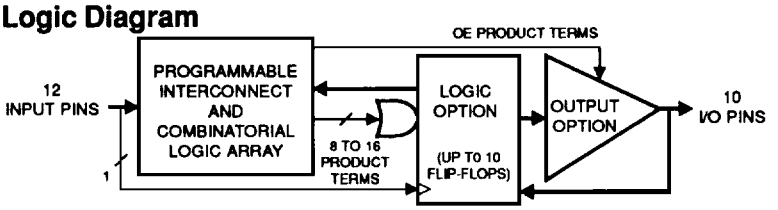
High Performance Flash PLD

Features

- **Industry Standard Architecture**
  - **Low-Cost, Easy-To-Use Software Tools**
- **High Speed Electrically Erasable Programmable Logic Device**
  - **7.5 ns Max Propagation Delay**
- **Low Power ATF22V10BL - 10 mA Maximum Standby**
- **CMOS and TTL Compatible Inputs and Outputs**
  - **Input and I/O Pull-Up Resistors**
- **Advanced Flash Technology**
  - **Reprogrammable**
  - **100% Tested**
- **High Reliability CMOS Technology**
  - **20 Year Data Retention**
  - **100 Erase/Write Cycles**
  - **2,000 V ESD Protection**
  - **200 mA Latchup Immunity**
- **Full Military, Commercial and Industrial Temperature Ranges**
- **Dual-In-Line and Surface Mount Packages in Standard Pinouts**

Logic Diagram



Description

The ATF22V10B and ATF22V10BL are high performance CMOS (Electrically Erasable) Programmable Logic Devices (PLDs) which utilize Atmel's proven electrically erasable Flash memory technology. Speeds down to 7.5 ns and power dissipation as low as 10 mA are offered. All speed ranges are specified over the full 5 V ± 10% range for military and industrial temperature ranges, and 5V ± 5% for commercial ranges.

The ATF22V10BL provides the fastest low power CMOS PLD solution, with low DC power (5.0 mA typical). The ATF22V10BL significantly reduces total system power and enhances system reliability.

The ATF22V10B and ATF22V10BL incorporate a variable product term architecture. Each output is allocated from eight to 16 product terms, which allows highly complex logic functions to be realized.

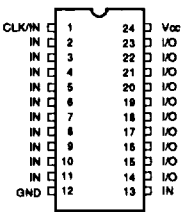
Two additional product terms are included to provide synchronous preset and asynchronous reset. These terms are common to all 10 registers. All registers are automatically cleared upon power up.

Register Preload simplifies testing. A Security Fuse prevents unauthorized copying of programmed fuse patterns.

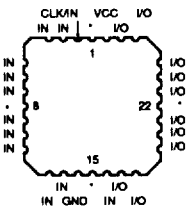
Pin Configurations

Pin Name	Function
CLK	Clock
IN	Logic Inputs
I/O	Bidirectional Buffers
*	No Internal Connection
VCC	+5 V Supply

DIP/SOIC



LCC/PLCC



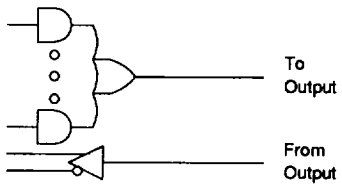
Absolute Maximum Ratings*

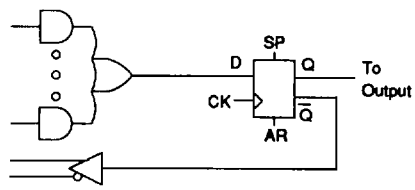
Temperature Under Bias	-55°C to +125°C
Storage Temperature	-65°C to +150°C
Voltage on Any Pin with Respect to Ground	-2.0 V to +7.0 V(1)
Voltage on Input Pins with Respect to Ground During Programming	-2.0 V to +14.0 V(1)
Programming Voltage with Respect to Ground	-2.0 V to +14.0 V(1)

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

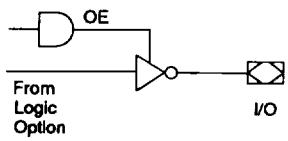
Note:
1. Minimum voltage is -0.6 V dc which may undershoot to -2.0 V for pulses of less than 20 ns. Maximum output pin voltage is V_{CC}+0.75 V dc which may overshoot to +7.0 V for pulses of less than 20 ns.

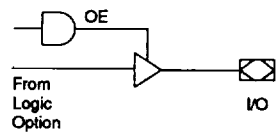
Logic Options





Output Options





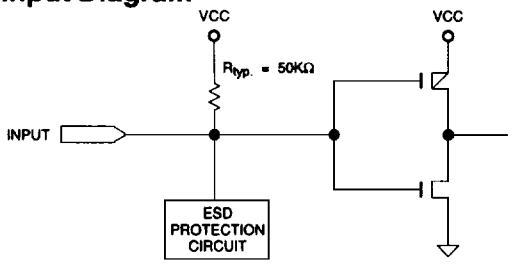
D.C. and A.C. Operating Conditions

	Commercial	Industrial	Military
Operating Temperature (Case)	0°C - 70°C	-40°C - 85°C	-55°C - 125°C
V_{CC} Power Supply	5 V ± 5%	5 V ± 10%	5 V ± 10%

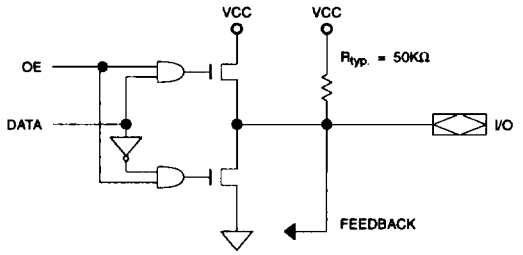
Input and I/O Pull-Ups

The ATF22V10B and ATF22V10BL have internal input and I/O active pull-up resistors. Therefore, whenever inputs or I/Os are not being driven externally, they will float to Vcc. This ensures that all logic array inputs are at known states. These are relatively weak active pull-ups that can easily be overdriven by TTL compatible drivers (see input and I/O diagrams below).

Input Diagram



I/O Diagram

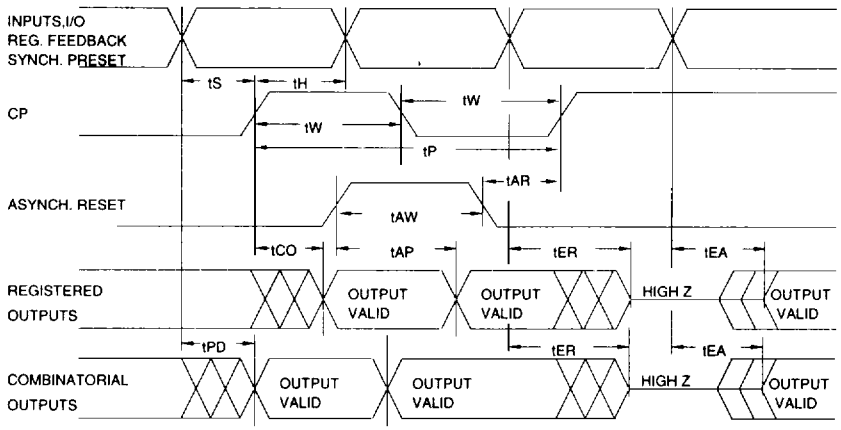


D.C. Characteristics

Symbol	Parameter	Condition			Min	Typ	Max	Units
I_{LI}	Input or I/O Low Leakage Current	$0 \le V_{IN} \le V_{IL}$(MAX)				-35	150	µA
I_{LO}	Input or I/O High Leakage Current	$3.5 \le V_{IN} \le V_{CC}$					10	µA
I_{CC}	Power Supply Current, Standby	V_{CC} = MAX, V_{IN} = MAX, Outputs Open	B-7, -10	Com.		90	120	mA
				Ind., Mil.		90	140	mA
			B-15, -25	Com.		90	120	mA
				Ind., Mil.		90	140	mA
			BL-15	Com.		5	10	mA
				Ind., Mil.		10	15	mA
I_{CC2}	Clocked Power Supply Current	V_{CC} = MAX, Outputs Open	BL-15	Com.		1		mA/MHz(2)
I_{CC3}	Clocked Power Supply Current	V_{CC} = MAX, Outputs Open, f=25 MHz	B-7, -10	Com.		90	120	mA
				Ind., Mil.		90	140	mA
			B-15, -25	Com.		90	120	mA
				Ind., Mil.		90	140	mA
			BL-15	Com.		60	90	mA
				Ind., Mil.		60	130	mA
I_{OS} (1)	Output Short Circuit Current	V_{OUT} = 0.5 V					-130	mA
V_{IL}	Input Low Voltage				-0.5		0.8	V
V_{IH}	Input High Voltage				2.0		V_{CC}+0.75	V
V_{OL}	Output Low Voltage	$V_{IN} = V_{IH}$ or V_{IL}, V_{CC} = MIN	I_{OL} = 16 mA	Com.,Ind.			0.5	V
			I_{OL} = 12 mA	Mil.			0.5	V
			I_{OL} = 24 mA	Com.			0.8	V
V_{OH}	Output High Voltage	$V_{IN}=V_{IH}$ or V_{IL}, V_{CC}=MIN	I_{OH} = -4.0 mA		2.4			V

Notes: 1. Not more than one output at a time should be shorted. Duration of short circuit test should not exceed 30 sec.
2. See I_{CC} versus frequency characterization curves.

A.C. Waveforms[1]



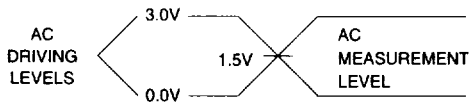
Note: 1. Timing measurement reference is 1.5 V. Input A.C. driving levels are 0.0 V and 3.0 V, unless otherwise specified.

A.C. Characteristics[1]

Symbol	Parameter	-7		-10		-15		-25		Units
		Min	Max	Min	Max	Min	Max	Min	Max	
t_{PD}	Input or Feedback to Combinatorial Output	3	7.5	3	10	3	15	3	25	ns
t_{CO}	Clock to Output	2	4.5 [2]	2	6.5	2	8	2	15	ns
t_{CF}	Clock to Feedback		3.5		4		4.5		13	ns
t_S	Input or Feedback Setup Time	3.5		4.5		10		15		ns
t_H	Hold Time	0		0		0		0		ns
F_{MAX}	External Feedback $1/(t_S + t_{CO})$	125 [3]		90		55.5		33.3		MHz
	Internal Feedback $1/(t_S + t_{CF})$	153		125		69		35.7		MHz
	No Feedback	166		166		83.3		38.5		MHz
t_P	Clock Period	6		8		12		26		ns
t_W	Clock Width	3		3		6		13		ns
t_{EA}	Input or I/O to Output Enable	3	7.5	3	10	3	15	3	25	ns
t_{ER}	Input or I/O to Output Disable	3	7.5	3	9	3	15	3	25	ns
t_{AP}	Input or I/O to Asynchronous Reset of Register	3	10	3	12	3	20	3	25	ns
t_{AW}	Asynchronous Reset Width	7		8		15		25		ns
t_{AR}	Asynchronous Reset Recovery Time	5		6		10		25		ns
t_{SP}	Setup Time, Synchronous Preset	4.5		6/10		10		15		ns
t_{SPR}	Synchronous Preset to Clock Recovery Time	5		8		10		15		ns

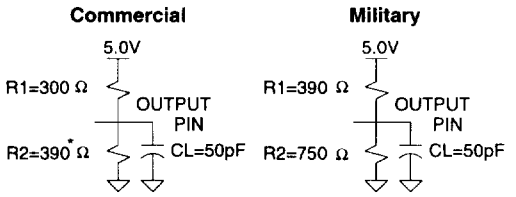
Notes: 1. See ordering information for valid part numbers.
2. 5.5 nsec for DIP package devices.
3. 111 MHz for DIP package devices.

Input Test Waveforms and Measurement Levels



tR, tF < 3 ns (10% to 90%)

Output Test Loads:



* All except -7 which is R2 = 300 Ω

Pin Capacitance (f = 1 MHz, T = 25°C) [1]

	Typ	Max	Units	Conditions
C_{IN}	5	8	pF	V_{IN} = 0 V
C_{OUT}	6	8	pF	V_{OUT} = 0 V

Note: 1. Typical values for nominal supply voltage. This parameter is only sampled and is not 100% tested.

Power Up Reset

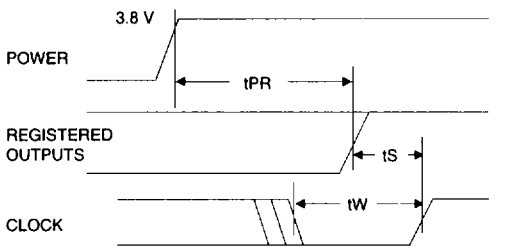
The registers in the ATF22V10B and ATF22V10BL are designed to reset during power up. At a point delayed slightly from V_{CC} crossing 3.8 V, all registers will be reset to the low state. The output state will depend on the polarity of the output buffer.

This feature is critical for state machine initialization. However, due to the asynchronous nature of reset and the uncertainty of how V_{CC} actually rises in the system, the following conditions are required:

1) The V_{CC} rise must be monotonic,

2) After reset occurs, all input and feedback setup times must be met before driving the clock pin high, and

3) The clock must remain stable during t_{PR}.



Parameter	Description	Min	Typ	Max	Units
t_{PR}	Power-Up Reset Time		600	1000	ns

Preload of Registered Outputs

When testing state machine designs, all possible states and state transitions must be verified in the design, not just those required in the normal machine operations. This is because certain events may occur during system operation that throw the logic into an illegal state (power-up, line voltage glitches, brown-outs, etc.). To test a design for proper treatment of these conditions, a way must be provided to break the feedback paths, and force any desired (i.e., illegal) state into the registers. Then the machine can be sequenced and the outputs tested for correct next state conditions.

The ATF22V10B/BL device includes circuitry that allows each registered output to be synchronously set either high or low. Thus, any present state condition can be forced for test sequencing. If necessary, approved programmers capable of executing test vectors perform output register preload automatically.

Device Programming

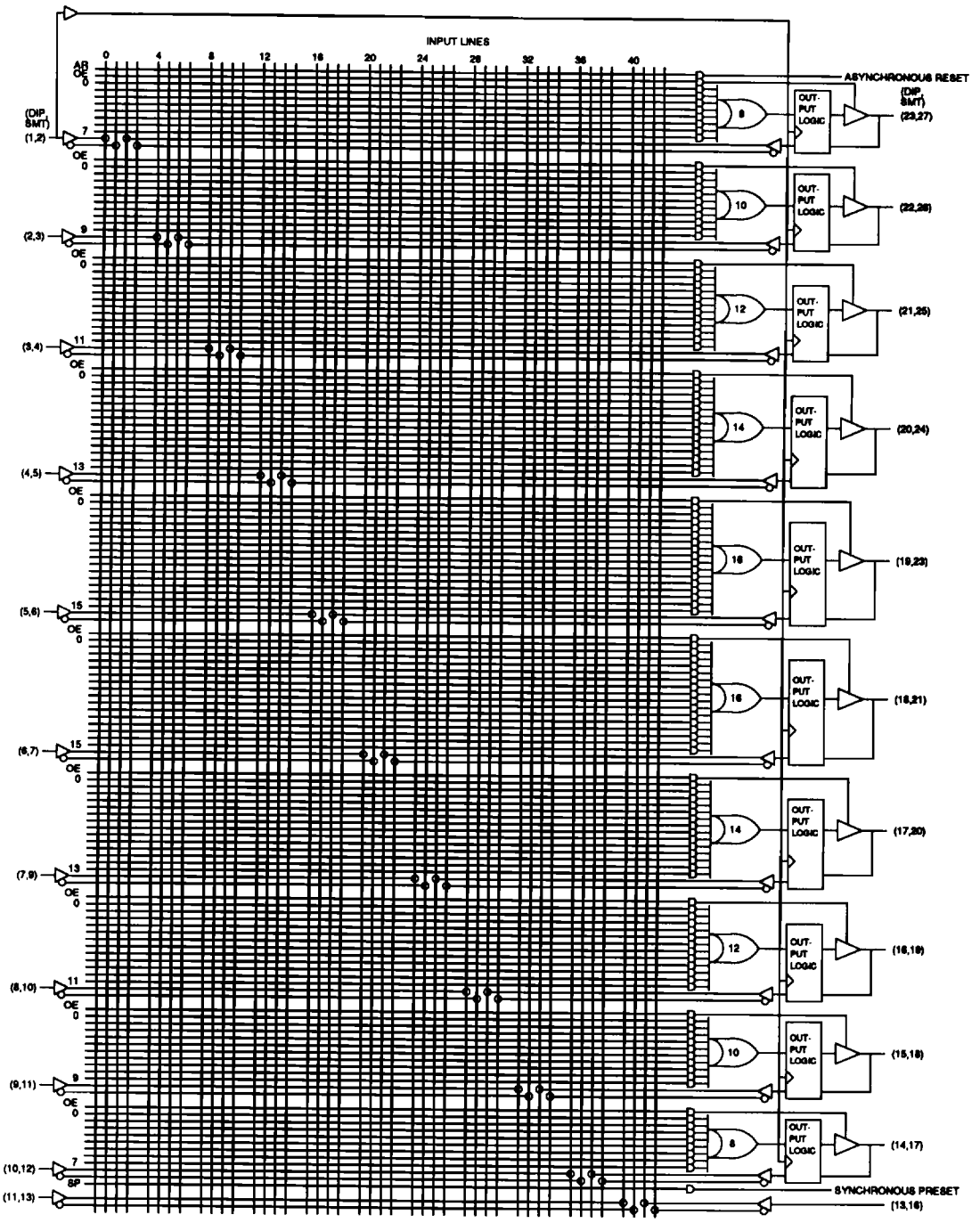
ATF22V10B/BL devices are programmed using an Atmel-approved logic programmer, available from a number of manufacturers. Complete programming of the device takes only a few seconds. Erasing of the device is transparent to the user, and is done automatically as part of the programming cycle.

Security Fuse Usage

A single fuse is provided to prevent unauthorized copying of the ATF22V10B fuse patterns. Once programmed, fuse verify and preload are inhibited. However, the 64 bit User Signiture remains accessible.

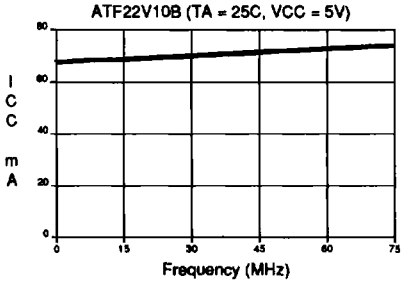
The security fuse should be programmed last, as its effect is immediate.

Functional Logic Diagram ATF22V10B/BL



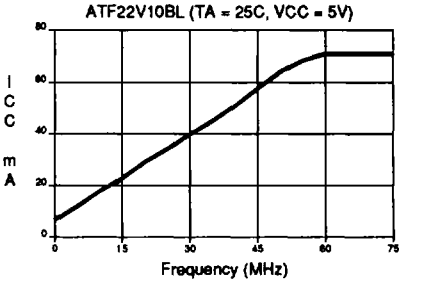
SUPPLY CURRENT vs. INPUT FREQUENCY

ATF22V10B (TA = 25C, VCC = 5V)

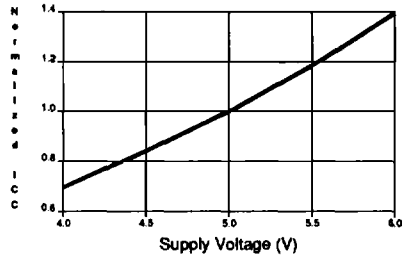


SUPPLY CURRENT vs. INPUT FREQUENCY

ATF22V10BL (TA = 25C, VCC = 5V)

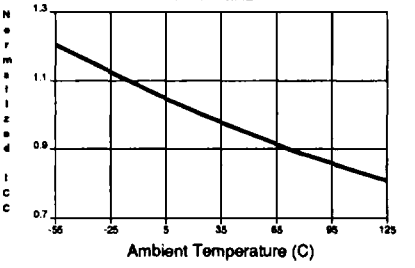


NORMALIZED SUPPLY CURRENT vs. SUPPLY VOLTAGE



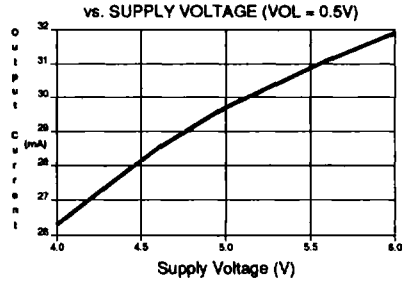
NORMALIZED ICC vs. AMBIENT TEMP.

f = 50 MHz



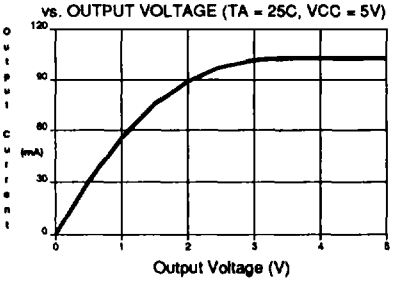
OUTPUT SINK CURRENT

vs. SUPPLY VOLTAGE (VOL = 0.5V)



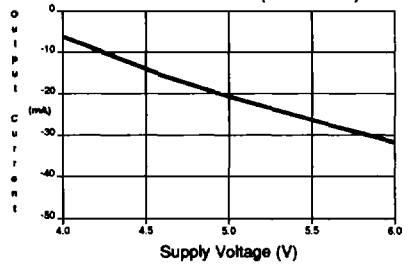
OUTPUT SINK CURRENT

vs. OUTPUT VOLTAGE (TA = 25C, VCC = 5V)



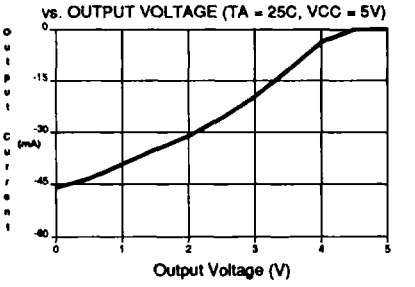
OUTPUT SOURCE CURRENT

vs. SUPPLY VOLTAGE (VOH = 2.4V)

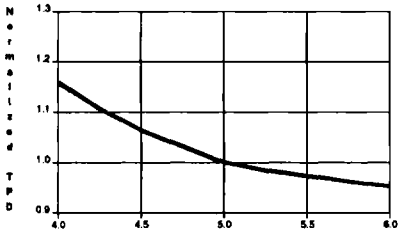


OUTPUT SOURCE CURRENT

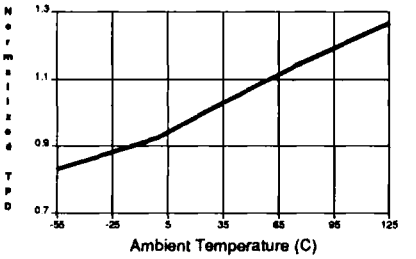
vs. OUTPUT VOLTAGE (TA = 25C, VCC = 5V)



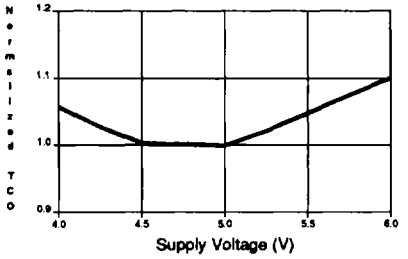
NORMALIZED TPD
vs. SUPPLY VOLTAGE



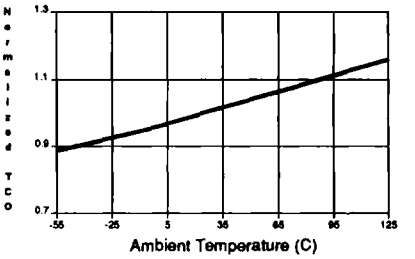
NORMALIZED TPD
vs. TEMPERATURE



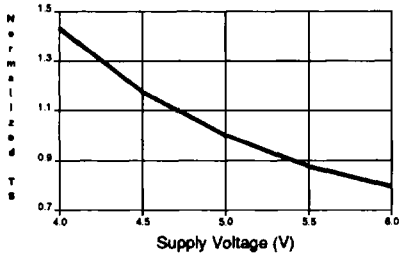
NORMALIZED TCO
vs. SUPPLY VOLTAGE



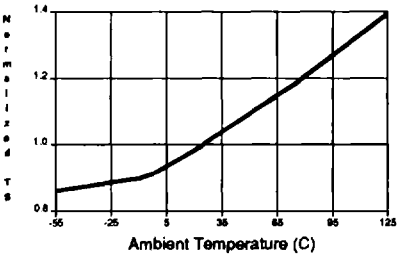
NORMALIZED TCO
vs. TEMPERATURE



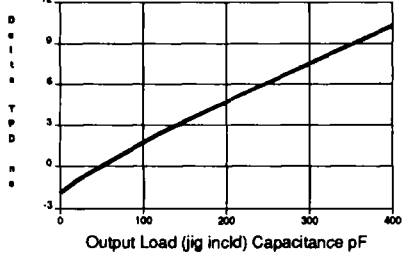
NORMALIZED TS
vs. SUPPLY VOLTAGE



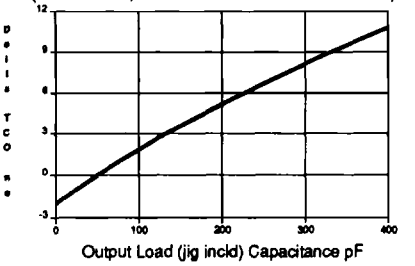
NORMALIZED TS
vs. TEMPERATURE



DELTA TPD vs. OUTPUT LOADING
(VCC = 4.5V, OUTPUT LOAD = COMMERCIAL)



DELTA TCO vs. OUTPUT LOADING
(VCC = 4.5V, OUTPUT LOAD = COMMERCIAL)



Ordering Information

t_{PD} (ns)	t_S (ns)	t_{CO} (ns)	Ordering Code	Package	Operation Range
7.5	6.5	5	ATF22V10B-7GC ATF22V10B-7JC ATF22V10B-7PC	24D3 28J 24P3	Commercial (0°C to 70°C)
10	7	7	ATF22V10B-10GC ATF22V10B-10JC ATF22V10B-10PC ATF22V10B-10SC	24D3 28J 24P3 24S	Commercial (0°C to 70°C)
			ATF22V10B-10GI ATF22V10B-10JI ATF22V10B-10PI ATF22V10B-10SI	24D3 28J 24P3 24S	Industrial (-40°C to 85°C)
			ATF22V10B-10GM ATF22V10B-10NM	24D3 28L	Military (-55°C to 125°C)
			ATF22V10B-10GM/883 ATF22V10B-10NM/883	24D3 28L	Military/883C (-55°C to 125°C) Class B, Fully Compliant
15	10	8	ATF22V10B-15GC ATF22V10B-15JC ATF22V10B-15PC ATF22V10B-15SC	24D3 28J 24P3 24S	Commercial (0°C to 70°C)
			ATF22V10B-15GI ATF22V10B-15JI ATF22V10B-15PI ATF22V10B-15SI	24D3 28J 24P3 24S	Industrial (-40°C to 85°C)
			ATF22V10B-15GM ATF22V10B-15NM	24D3 28L	Military (-55°C to 125°C)
			ATF22V10B-15GM/883 ATF22V10B-15NM/883	24D3 28L	Military/883C (-55°C to 125°C) Class B, Fully Compliant
25	15	15	ATF22V10B-25GC ATF22V10B-25JC ATF22V10B-25PC ATF22V10B-25SC	24D3 28J 24P3 24S	Commercial (0°C to 70°C)
			ATF22V10B-25GI ATF22V10B-25JI ATF22V10B-25PI ATF22V10B-25SI	24D3 28J 24P3 24S	Industrial (-40°C to 85°C)

Ordering Information

t_{PD} (ns)	t_S (ns)	t_{CO} (ns)	Ordering Code	Package	Operation Range
15	10	8	ATF22V10BL-15GC ATF22V10BL-15JC ATF22V10BL-15PC ATF22V10BL-15SC	24D3 28J 24P3 24S	Commercial (0°C to 70°C)
			ATF22V10BL-15GI ATF22V10BL-15JI ATF22V10BL-15PI ATF22V10BL-15SI	24D3 28J 24P3 24S	Industrial (-40°C to 85°C)
			ATF22V10BL-15GM ATF22V10BL-15NM	24D3 28L	Military (-55°C to 125°C)
			ATF22V10BL-15GM/883 ATF22V10BL-15NM/883	24D3 28L	Military/883C (-55°C to 125°C) Class B, Fully Compliant

Package Type	
24D3	24 Lead, 0.300" Wide, Ceramic Dual Inline Package (Cerdip)
28J	28 Lead, Plastic J-Leaded Chip Carrier (PLCC)
28L	28 Pad, Ceramic Leadless Chip Carrier (LCC)
24P3	24 Lead, 0.300" Wide, Plastic Dual Inline Package (PDIP)
24S	24 Lead, 0.300" Wide, Plastic Gull Wing Small Outline (SOIC)