SRAM

128 K x 16 SRAM

HIGH SPEED CMOS SRAM

FEATURES

- Fast access times : 10, 12, and 15ns
- Fast $\overline{OE}$ access times : 5, 6, and 7ns
- Single +3.3V± 0.3V power supply
- Fully static -- no clock or timing strobes necessary
- All inputs and outputs are TTL-compatible
- Three state outputs
- Center power and ground pins for greater noise immunity
- Easy memory expansive with $\overline{CE}$ and $\overline{OE}$ options
- Automatic $\overline{CE}$ power down
- High-performance, low-power consumption, CMOS triple-poly, double-metal process

ORDERING INFORMATION

44-pin 400mil SOJ
44-pin 400mil TSOP (TypeII)

PRODUCT NO.	Acess Time (ns)	PACKING TYPE
M21L216128A-10J	10	SOJ
M21L216128A-10T		TSOP
M21L216128A-12J	12	SOJ
M21L216128A-12T		TSOP
M21L216128A-15J	15	SOJ
M21L216128A-15T		TSOP

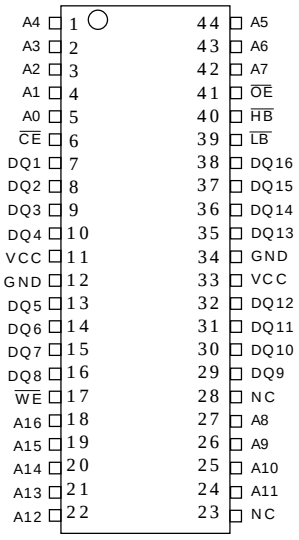
GENERAL DESCRIPTION

The M21L216128A is a high speed, low power asynchronous SRAM containing 2,097,152 bits and organized as 131,072 by 16 bits, it is produced by high performance CMOS process.

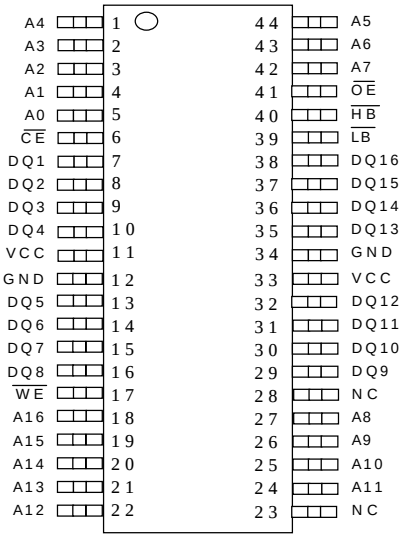
This device offers center power and ground pins for improved performance and noise immunity. Static design eliminates the need for external clocks or timing strobes. For increased system flexibility and eliminating bus contention problems, this device offers chip enable ($\overline{CE}$), separate byte enable controls ($\overline{LB}$ and $\overline{HE}$) and output enable ($\overline{OE}$) with this organization.

PIN ASSIGNMENT

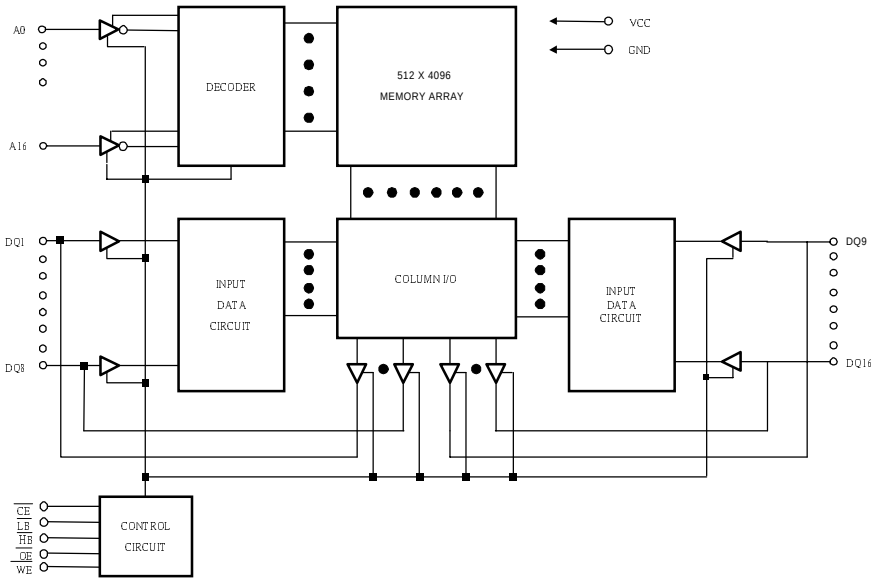
SOJ Top View



TSOP (TypeII) Top View



Block Diagram



Pin Descriptions

Pin No.	Symbol	Description
1 - 5, 18 - 22, 24-27, 42 - 44	A0 - A16	Address Inputs
6	$\overline{CE}$	Chip Enable Input
7 - 10, 13 - 16, 29 - 32, 35 - 38	DQ1 - DQ16	Data Inputs/Outputs
17	$\overline{WE}$	Write Enable Input
39	$\overline{LB}$	Lower Byte Enable Input (DQ1 to DQ8)
40	$\overline{HB}$	Higher Byte Enable Input (DQ9 to DQ16)
41	$\overline{OE}$	Output Enable Input
11, 33	VCC	Power
12, 34	GND	Ground
23, 28	NC	No Connection

ABSOLUTE MAXIMUM RATINGS *

Voltage on V_{CC} Supply Relative to Vss ... ……-0.5V to +4.6V

V_{IN} ……..-0.5V to V_{CC}+1.0V

Operating Temperature, Topr …….. 0 °C to +70 °C

Storage Temperature (plastic) ……-55 °C to +125 °C

Junction Temperature ……+125 °C

Power Dissipation ……1.0W

Short Circuit Output Current ……50mA

*Stresses greater than those listed under Absolute Maximum. Ratings may permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATIONS

(All Temperature Ranges ; V_{CC} = 3.3V ± 0.3V unless otherwise noted)

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input High (Logic 1) Voltage		V_{IH}	2.2	V_{CC}+0.5	V	1,2
Input Low (Logic 0) Voltage		V_{IL}	-0.5	0.8	V	1,2
Input Leakage Current	$0V \le V_{IN} \le V_{CC}$	I_{LI}	-10	10	µA	
Output Leakage Current	Output(s) disable $0V \le V_{OUT} \le V_{CC}$	I_{LO}	-5	5	µA	
Output High Voltage	I_{OH} = -4.0 mA	V_{OH}	2.4		V	1
Output Low Voltage	I_{OL} = 8.0 mA	V_{OL}		0.4	V	1
Supply Voltage		V_{CC}	3.0	3.6	V	1

DESCRIPTION	CONDITIONS	SYMBOL	MAX			UNITS	NOTES
			-10	-12	-15		
Power Supply Current : Operating	Device selected; $\overline{CE} \le V_{IL}$; V_{CC}=MAX; $f=f_{MAX}$; outputs open	I_{CC}	190	160	130	mA	3
TTL Standby	$\overline{CE} \ge V_{IH}$; V_{CC}=MAX; $f=f_{MAX}$	I_{SB1}	35	30	25	mA	
CMOS Standby	$\overline{CE1} \ge V_{CC}$-0.2; V_{CC} = MAX; all other inputs ≤ GND +0.2 or ≥ V_{CC}-0.2; all inputs static ; f=0	I_{SB2}	10	10	10	mA	

CAPACITANCE

DESCRIPTION	CONDITIONS	SYMBOL	MAX	UNITS	NOTES
Input Capacitance	T_A= 25°C ; f=1 MHz	C_I	6	pF	4
Input/Output Capacitance(DQ)	V_{CC}=3.3V	$C_{I/O}$	8	pF	4

AC ELECTRICAL CHARACTERISTICS

(Note 5)(All Temperature Ranges; V_{CC} =3.3V ± 0.3V)

DESCRIPTION	SYMBOL	-10		-12		-15		UNIT	Notes
		MIN	MAX	MIN	MAX	MIN	MAX		
Read Cycle									
Read Cycle Time	t_{RC}	10		12		15		ns	
Access access time	t_{AA}		10		12		15	ns	
Chip Enable access time	t_{ACE}		10		12		15	ns	
Output hold from address change	t_{OH}	3		4		4		ns	
Chip Enable to output in Low-Z	t_{CLZ}	3		4		4		ns	4,7
Chip disable to output in High-Z	t_{CHZ}		5		6		7	ns	4,6,7
Output Enable access time	t_{OE}		5		6		7	ns	
Output Enable to output in Low-Z	t_{OLZ}	0		0		0		ns	
Output Disable to output in High-Z	t_{OHZ}		5		6		7	ns	4,6
Byte Enable access time	t_{BE}		6		7		8	ns	
Byte Enable to output in Low-Z	t_{BLZ}	0		0		0		ns	4,7
Byte disable to output in High-Z	t_{BHZ}		5		6		7	ns	4,6,7
Write Cycle									
Write cycle time	t_{WC}	10		12		15		ns	
Chip Enable to end of write	t_{CW}	8		8		9		ns	
Address valid to end of write, with $\overline{OE}$ HIGH	t_{AW}	8		8		9		ns	
Address setup time	t_{AS}	0		0		0		ns	
Address hold from end of write	t_{WR}	0		0		0		ns	
Write pulse width	t_{WP2}	10		10		11		ns	
Write pulse width, with $\overline{OE}$ HIGH	t_{WP1}	8		8		9		ns	
Data setup time	t_{DW}	5		6		7		ns	
Data hold time	t_{DH}	0		0		0		ns	
Write disable to output in Low-Z	t_{OW}	3		4		5		ns	4,7
Byte Enable to output in High-Z	t_{WHZ}		5		6		7	ns	4,6,7
Byte Enable to end of write	t_{BW}	8		8		9		ns	

TRUTH TABLE

MODE	$\overline{CE}$	$\overline{WE}$	$\overline{OE}$	$\overline{LE}$	$\overline{HE}$	DQ1-DQ8	DQ9-DQ16	POWER
LOW BYTE READ (DQ1-DQ8)	L	H	L	L	H	Q	HIGH-Z	ACTIVE
HIGH BYTE READ (DQ9-DQ16)	L	H	L	H	L	HIGH-Z	Q	ACTIVE
WORD READ (DQ1-DQ16)	L	H	L	L	L	Q	Q	ACTIVE
LOW BYTE WRITE (DQ1-DQ8)	L	L	X	L	H	D	HIGH-Z	ACTIVE
HIGH BYTE WRITE (DQ9-DQ16)	L	L	X	H	L	HIGH-Z	D	ACTIVE
WORD WRITE (DQ1-DQ16)	L	L	X	L	L	D	D	ACTIVE
OUTPUT DISABLE	L	X	X	H	H	HIGH-Z	HIGH-Z	ACTIVE
	L	H	H	X	X	HIGH-Z	HIGH-Z	ACTIVE
STANDBY	H	X	X	X	X	HIGH-Z	HIGH-Z	STANBY

AC TEST CONDITIONS

Input plus levels	0V to 3.0V
Input rise and fail times	1.5ns
Input timing reference levels	1.5V
Output reference levels	1.5V
Output load	See Figures 1 and 2

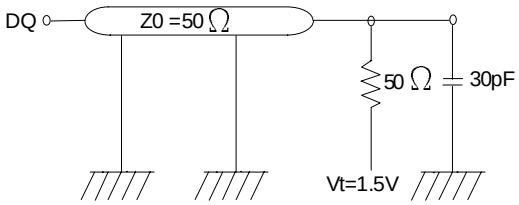


Fig.1 OUTPUT LOAD EQUIVALENT

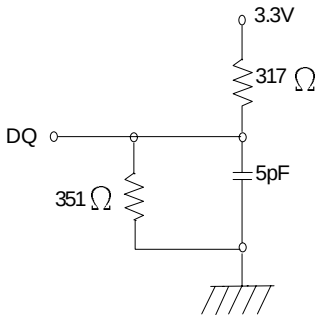


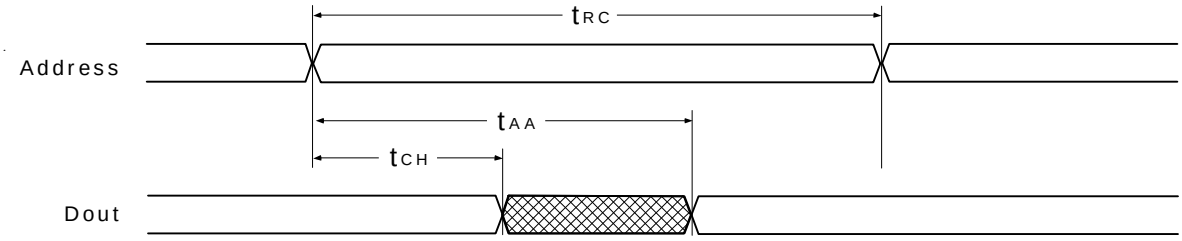
Fig.2 OUTPUT LOAD EQUIVALENT

NOTES

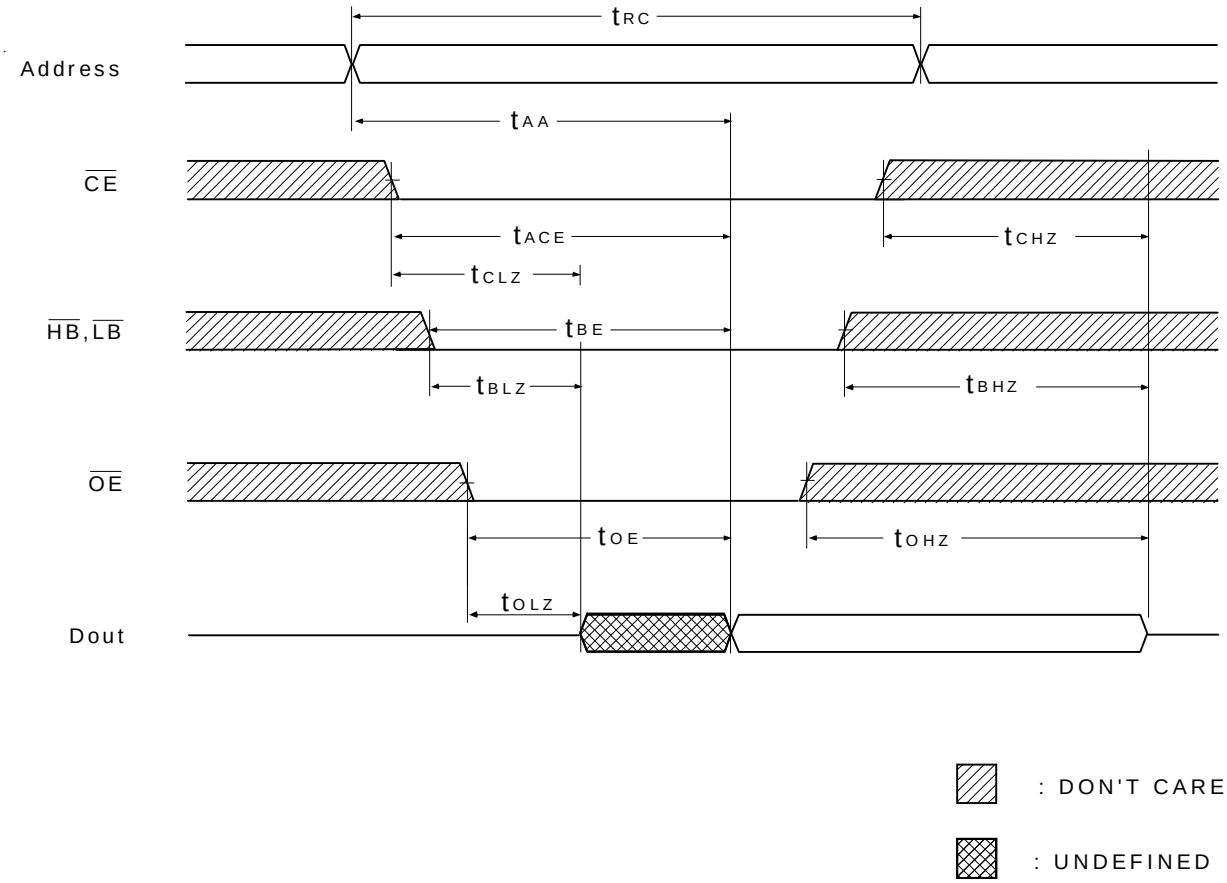
1. All voltages referenced to GND (VSS).
2. Overshoot : $V_{IH} \leq +6.0V$ for $t \leq t_{RC}/2$.
   Undershoot : $V_{IL} \leq -2.0V$ for $t \leq t_{RC}/2$.
3. I_{CC} is given without output current. ICC increases with greater output loading and faster cycle times.
4. This parameter is sampled.
5. Test conditions as specified with the output loading as shown in Fig. 1 unless otherwise noted.
6. Output loading is specified with CL=5pF as in Fig.2. Transition is measured $\pm$ 500mV from steady static voltage.
7. At any give temperature and voltage conditions, t_{CHZ} is less than t_{CLZ} and t_{WHZ} is less than t_{OW}
8. $\overline{WE}$ is High for Read cycle.
9. Device is continuously selected. Chip enable and output enables are held in their active state.
10. Address valid prior to, or coincident with, latest occurring chip enable.
11. t_{RC}=Read Cycle Time.
12. Chip Enable and Write Enable can initiate and terminate a Write cycle.
13. Capacitance derating applies to capacitance different from the load capacitance shown in Fig. 1.

Timing Waveforms

Read Cycle 1[8, 9]



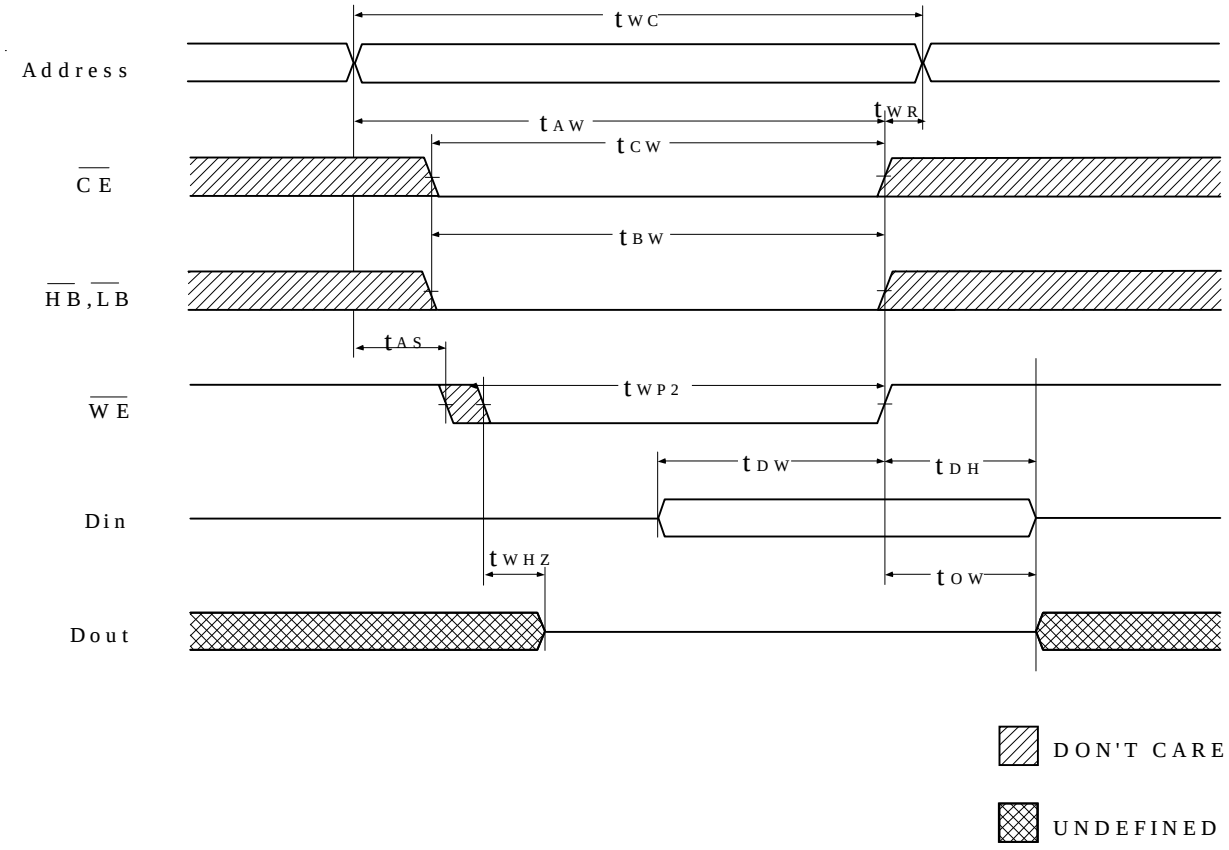
Read Cycle 2[7, 8, 9, 10]



Timing Waveforms (continued)

Write Cycle 1[7, 12, 13]

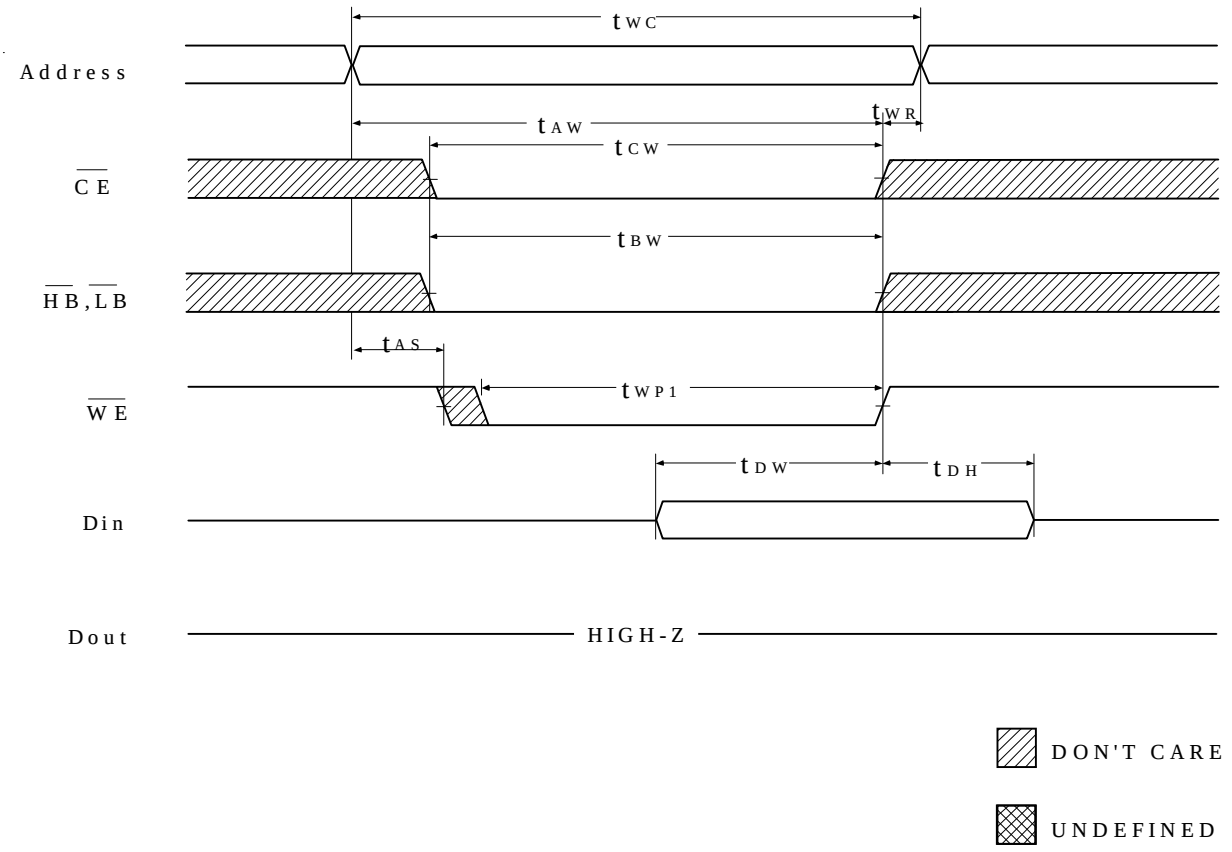
(Write Enable Controlled with Output Enable $\overline{OE}$ active LOW)



Timing Waveforms (continued)

Write Cycle 2[12, 13]

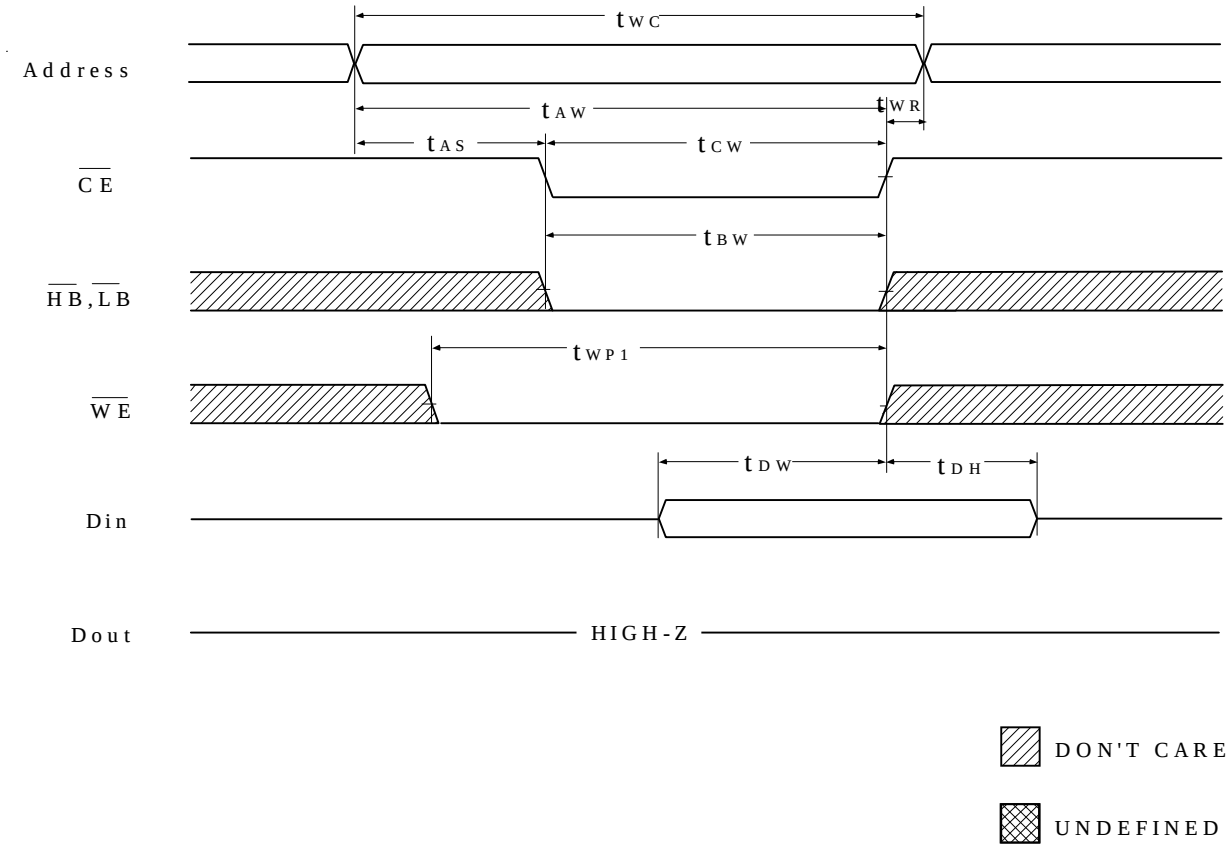
(Write Enable Controlled with Output Enable $\overline{OE}$ active HIGH)



Timing Waveforms (continued)

Write Cycle 3[12, 13]

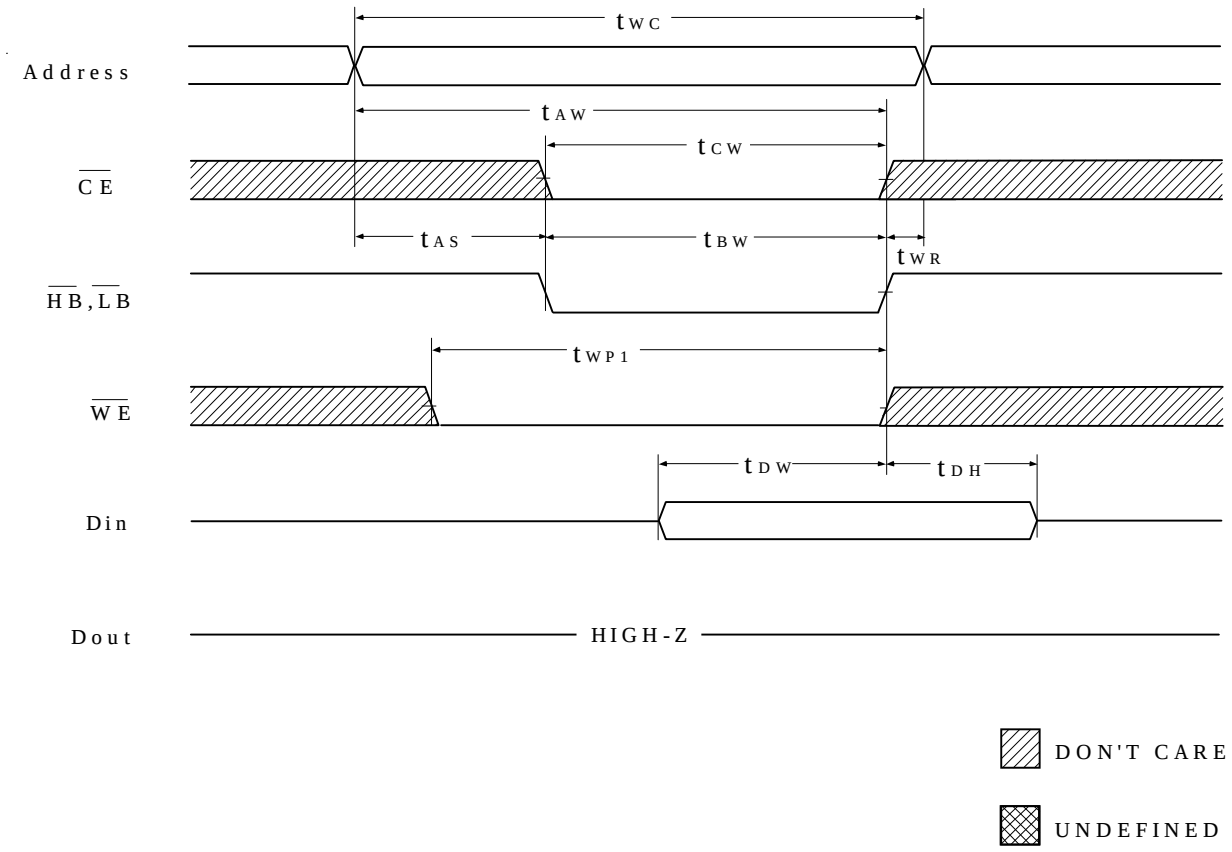
(Chip Enable Controlled)



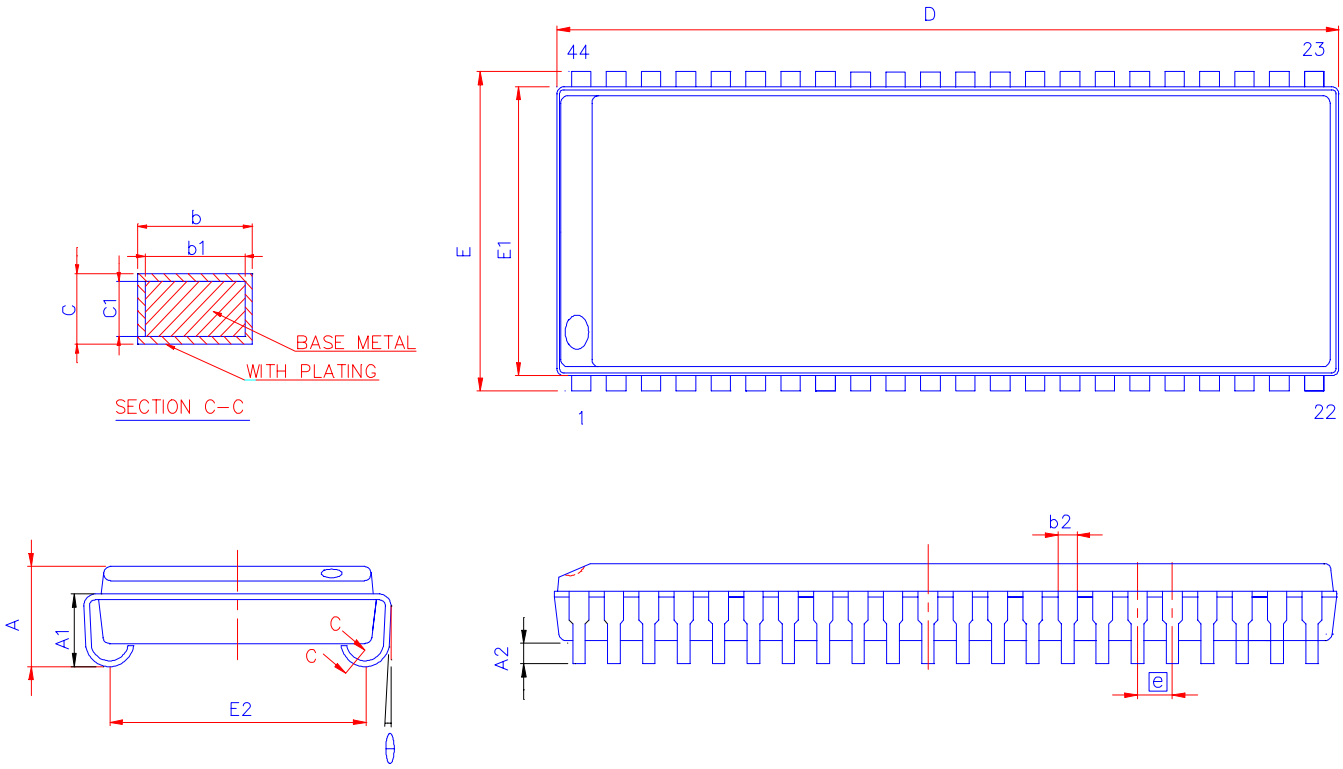
Timing Waveforms (continued)

Write Cycle 4(12, 13)

(Byte Enable Controlled)

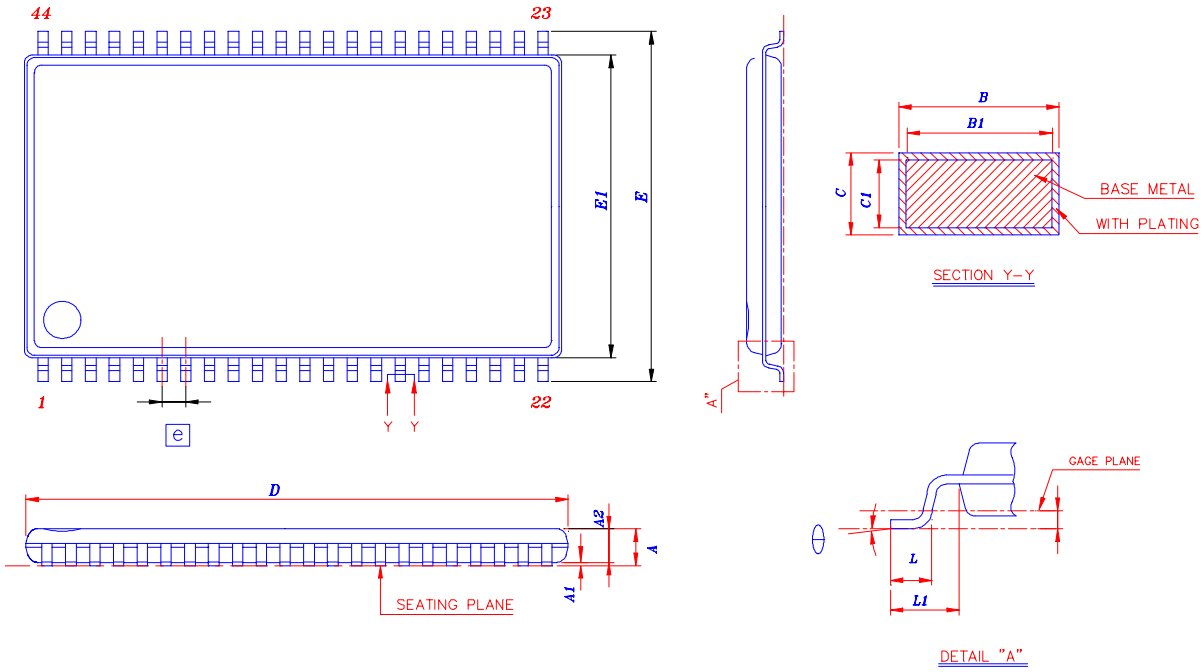


PACKING DIMENSIONS
44-LEAD SOJ SRAM(400mil)



SYMBOL	DIMENSION (INCH)			DIMENSION (MM)		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.128	0.138	0.148	3.25	3.51	3.76
A1	0.082	-	-	2.08	-	-
A2	0.025	-	-	0.60	-	-
b	0.015	-	0.020	0.38	-	0.51
b1	0.015	-	0.018	0.38	-	0.46
c	0.007	-	0.013	0.18	-	0.21
c1	0.007	0.008	0.011	0.18	0.20	0.28
D	1.120	1.125	1.130	28.45	28.58	28.70
E	0.435	0.440	0.445	11.05	11.18	11.30
E1	0.394	0.400	0.405	10.01	10.16	10.29
θ	0º		10º	0º		10º
e	0.050BSC			1.27 BSC		

PACKING DIMENSIONS
44-LEAD TSOP(II) SRAM(400mil)



Symbol	Dimension in mm			Dimension in inch		
	Min	Norm	Max	Min	Norm	Max
A	—	—	1.20	—	—	0.047
A1	0.05	—	0.15	0.002	—	0.006
A2	0.95	1.00	1.05	0.037	0.039	0.042
B	0.30	—	0.45	0.012	—	0.018
B1	0.30	0.35	0.40	0.012	0.014	0.016
C	0.12	—	0.21	0.005	—	0.008
C1	0.10	—	0.16	0.004	—	0.006
D	18.28	18.41	18.54	0.720	0.725	0.730
ZD	0.805 REF			0.0317 REF		
E	11.56	11.76	11.96	0.455	0.463	0.471
E1	10.03	10.16	10.29	0.395	0.400	0.4
L	0.40	0.59	0.69	0.016	0.023	0.027
L1	0.80 REF			0.031 REF		
e	0.80 BSC			0.0315 BSC		
θ	0°	—	8°	0°	—	8°

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