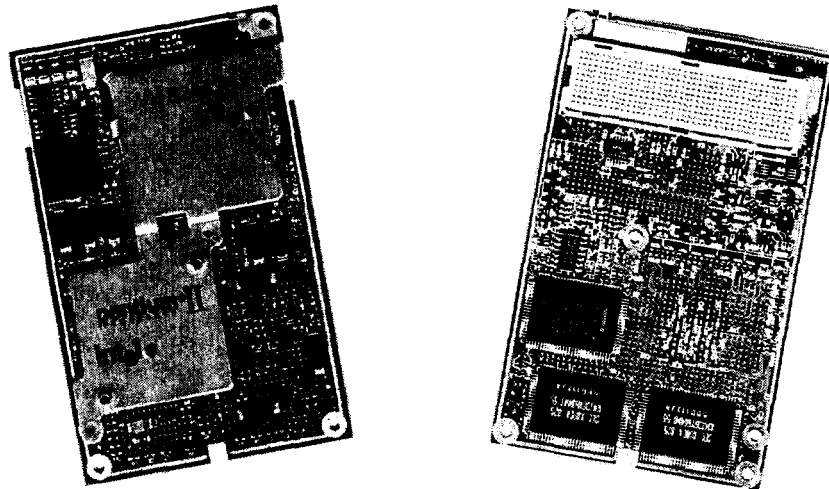# intel.

# INTEL PENTIUM® II PROCESSOR MOBILE MODULE : MOBILE MODULE CONNECTOR 2 (MMC-2)

- Intel Mobile Pentium® II processor running at 233/266/300 MHz
- Second-level cache of pipeline burst SRAM
  - Dedicated 64-bit wide bus for high speed data transfer
  - 512K Byte cache data array
  - Clock to BSRAM turns off when processor is in low power states
- Processor core voltage regulation supports input voltages from 5V to 21V
  - Above 80 percent peak efficiency
- Thermal transfer plate for heat dissipation
- Support single AGP-66 3.3V device

- Intel 443BX Host Bridge system controller
  - DRAM controller supports EDO and SDRAM at 3.3V
  - Supports PCI CLKRUN# protocol
  - SDRAM clock enable support and self refresh of EDO or SDRAM during Suspend mode
  - Compatible SMRAM (C_SMRAM) and Extended SMRAM (E_SMRAM) modes of power management; E_SMRAM mode supports write-back cacheable SMRAM up to 1 MB
  - 3.3V PCI bus control, Rev 2.1 compliant
- Active Thermal Feedback (ATF) sensing
  - Internal A/D - digital signaling (SMBUS) across the module interface
  - Programmable trip point interrupt or poll mode for temperature reading

The Intel Pentium® II Processor Mobile Module (400-pin MMC-2) is a small, highly integrated assembly containing an Intel Pentium II Mobile processor and its immediate system-level support. Specifically, the processor module contains a power supply for the processor's unique voltage requirements, a system Level 2 cache memory and the core logic required to bridge the processor to the standard system buses. The module interfaces electrically to its host system via a 3.3-volt PCI bus, a 3.3-volt memory bus and some Intel 443BX Host Bridge control signals.

## 1.0.   INTRODUCTION

The Intel Pentium II Processor Mobile Module is a fundamental building block for a system manufacturer to incorporate into a notebook system. The Intel Mobile Module incorporates an Intel Mobile Pentium II processor core, second-level cache with Tag RAM, Intel 443BX Host Bridge system controller "Northbridge," voltage regulator, and an SMBus thermal sensor on a single printed circuit board.

Intel's Host Bridge architecture allows for physical partitioning at the PCI, AGP and DRAM interfaces; therefore the electrical interconnect defined for the Intel Mobile Module includes the PCI bus, AGP bus, DRAM memory bus and some Host Bridge sideband signals. An onboard voltage regulator provides the DC conversion from the system manufacturer's system DC voltage to the processor's core and I/O voltage. This isolation of the processor voltage requirements allows the system manufacturer to incorporate Intel Mobile Modules with different processor variants into a single notebook system.

Building around this modular design gives the system manufacturer these advantages:

* Avoids complexities associated with designing high-speed processor core logic boards
* Provides an upgrade path from previous Intel Mobile Modules for notebook designs using a standard interface

This document provides the technical information required to assist the OEM in developing the latest notebook systems for today's notebook market.

### 1.1.   Pentium® II Processor Mobile Module Terminology

The following terms are used often in this document and are explained here for clarification:

**Pentium II processor**—The Central Processing Unit including cache components.

**Processor core**—The processor's execution engine.

**Thermal Transfer Plate (TTP)**—The surface used by the OEM to attach a system level thermal solution to the Intel Mobile Module.

**Thermal Design Power (TDP)**—The typical power consumed by the CPU while executing a standard application.

The L2 cache (TagRAM, BSRAM) die keep standard industry names.

### 1.2.   Revision History

Revision 2.0 is the original version of this document.

## 2.0.   ARCHITECTURE OVERVIEW

The Intel Mobile Module is a small, highly integrated assembly containing the Mobile Pentium II processor core with internal/bus frequencies of 300/66, 266/66, or 233/66 MHz and its immediate system-level support. The module interfaces electrically to its host system via a 3.3V PCI bus, a 3.3V AGP bus, a 3.3V memory bus and the Intel 443BX Host Bridge system controller.

The Pentium II Processor Mobile Module includes a second-level cache of pipeline burst SRAM supporting up to 512 KB. The ZZ "snooze" mode power management featured in previous mobile modules is not supported. Instead it supports the "Stop Clock" mode of power management for the L2 SRAMs. In this mode, the clock signals to the L2 SRAMs are stopped or "parked" in a low power state by the processor.

The Intel Mobile Module contains key features of the Intel 443BX Host Bridge system controller. The DRAM controller supports EDO at 3.3V with a burst read at 7-2-2-2 (60 ns) or SDRAM at 3.3V with a burst read at 8-1-1-1 (66 MHz, CL=2). The system controller provides a PCI CLKRUN# signal to request PIIX4E to start or maintain the PCI clock on the PCI bus. The 82443BXclock enable support enables Self Refresh mode of EDO or SDRAM during Suspend mode and is compatible with SMRAM (C_SMRAM) and Extended SMRAM (E_SMRAM) modes of power management; E_SMRAM mode supports write-back cacheable SMRAM up to 1 MB. The Intel 443BX Host Bridge system controller is a 3.3V PCI bus control which is compliant with PCI Rev 2.1 specifications.

The 443BX Host Bridge (Northbridge) is one of two physical VLSI devices that constitute the Intel 440BX AGPset. The second device (Southbridge) is known as the PIIX4E PCI/ISA bridge. The system manufacturer's system electronics, which connnects to the Intel

Mobile Module, must include a PIIX4E device. The PIIX4E provides extensive power management capabilities and is designed to support the 443BX Host Bridge in the Intel Pentium II Processor Mobile Module.

The processor core voltage regulation supports input voltages from 5V to 21V, enabling an above 80 percent peak efficiency and decouples processor voltage requirements from the system.

The Intel Mobile Module incorporates Active Thermal Feedback (ATF) sensing compliant to the ACPI Rev 1.0 specification. This is accomplished by including an SMBus compliant thermal sensor capable of supporting internal and external temperature sensing with programmable trip points.

A thermal transfer plate for heat dissipation from the processor and 443BX provides a standard thermal attach point to which the system manufacturer connects a system thermal solution.

Figure 1 illustrates the block diagram of the Intel Mobile Module.
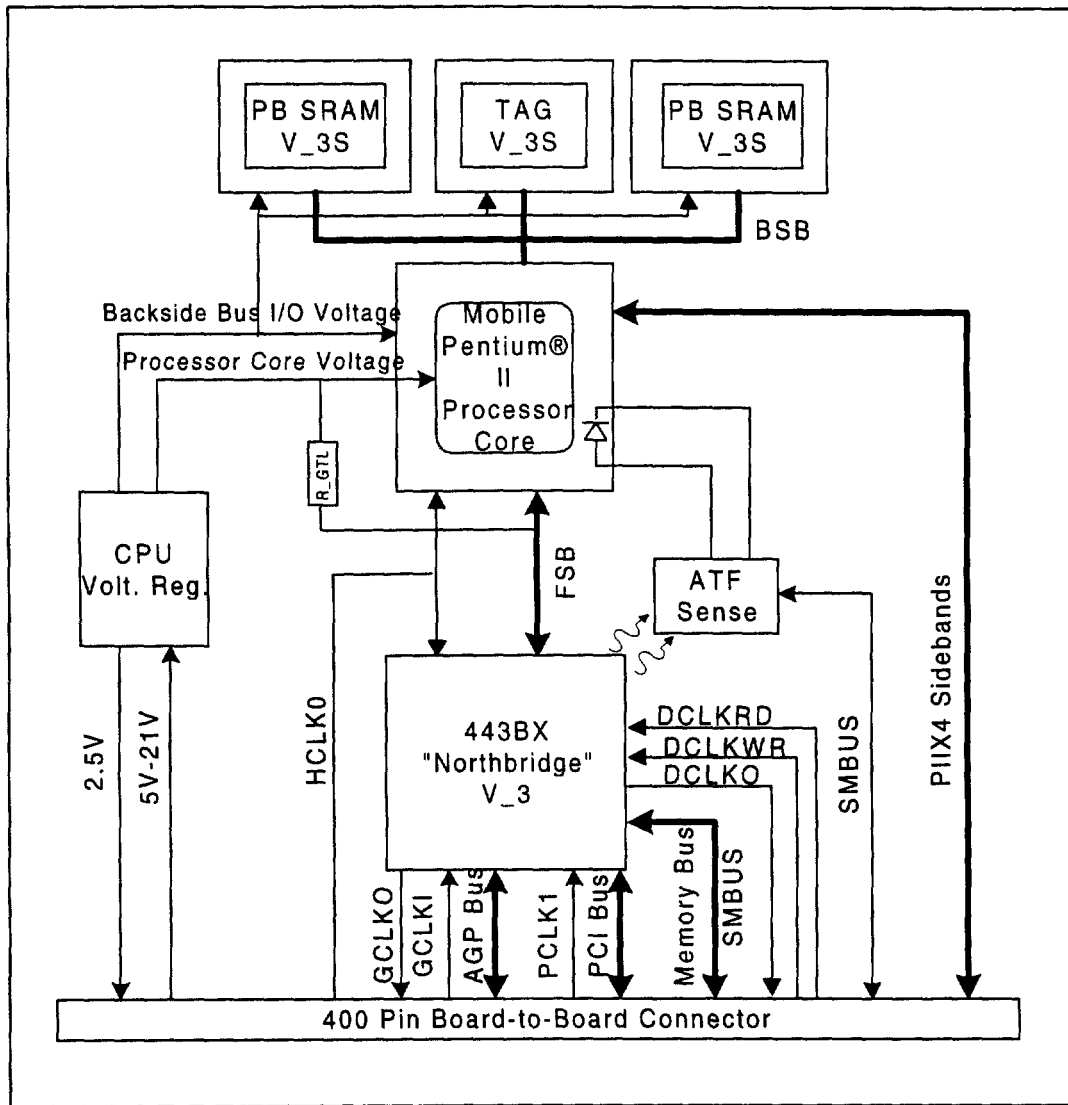
**Figure 1. Block Diagram of the Intel Mobile Module**

## 3.0. MODULE CONNECTOR INTERFACE

### 3.1. Signal Definitions

The Intel Mobile Module connector signals are defined with the intention of supporting future modules. Table 1 provides a list of signals by category and the corresponding number of signals in each category.

For proper signal termination, please contact your Intel sales representative for further information.

**Table 1. Module Connector Signal Summary**

| Signal Group | Number |
|---|---|
| Memory | 109 |
| AGP | 60 |
| PCI | 58 |
| Processor/PIIX4E Sideband | 8 |
| Power Management/Geyserville | 11 |
| Clocks | 9 |
| Voltage: V_DC | 20 |
| Voltage: V_3S | 9 |
| Voltage: V_5 | 3 |
| Voltage: V_3 | 16 |
| Voltage: VCCAGP | 4 |
| Voltage: V_CPUPU | 1 |
| Voltage: V_CLK | 1 |
| ITP/JTAG | 9 |
| Module ID | 4 |
| Ground | 45 |
| Reserved | 33 |
| **TOTAL PINS** | **400** |

### 3.1.1.    SIGNAL LIST

The following notations are used to denote the signal type:

I           Input pin

O          Output pin

O D        Open Drain Output pin. This pin requires a pull up resistor.

I D        Open Drain Input pin. This pin requires a pull up resistor.

I/O D      Input / Open Drain Output pin. This pin requires a pull up resistor.

I/O        Bi-directional Input / Output pin

The signal description also includes the type of buffer used for a particular signal:

GTL+       Open Drain GTL+ interface signal.

PCI        PCI bus interface signals.

AGP        AGP interface signals.

CMOS       The Mobile Module has Low Voltage TTL compatible (LVTTL) interfacing.

### 3.1.2.    MEMORY (109 SIGNALS)

Table 2 lists the Intel Mobile Module memory interface signals.

**Table 2. Memory Signal Descriptions**

| Name | Type | Voltage | Description |
|---|---|---|---|
| MECC[7:0] | I/O CMOS | V_3 | **Memory ECC Data:** These signals carry Memory ECC data during access to DRAM. These pins are implemented by design but not tested on MMC-2. |
| RASA[5:0]# or CSA[5:0]# | O CMOS | V_3 | **Row Address Strobe (EDO):** These pins select the DRAM row. **Chip Select (SDRAM):** These pins activate the SDRAMs. SDRAM accepts any command when its CS# pin is active low. |
| CASA[7:0]# or DQMA[7:0] | O CMOS | V_3 | **Column Address Strobe (EDO):** These pins select the DRAM column. **Input/Output Data Mask (SDRAM):** These pins act as synchronized output enables during a read cycle and as a byte mask during a write cycle.[1] |
| MAB[9:0]# MAB[10] MAB[12:11]# MAB[13] | O CMOS | V_3 | **Memory Address (EDO/SDRAM):** This is the row and column address for DRAM. The 443BX Host Bridge system controller has two identical sets of address lines (MAA and MAB#). The Pentium® II Processor Mobile Module supports only the MAB set of address lines. For additional addressing features, please refer to the *Intel 440BX AGPset* datasheet (Order Number 290633-001).[2] |
| MWEA# | O CMOS | V_3 | **Memory Write Enable (EDO/SDRAM):** MWEA# should be used as the write enable for the memory data bus. |
| SRASA# | O CMOS | V_3 | **SDRAM Row Address Strobe (SDRAM):** When active low, this signal latches Row Address on the positive edge of the clock. This signal also allows Row access and pre-charge. |
| SCASA# | O CMOS | V_3 | **SDRAM Column Address Strobe (SDRAM):** When active low, this signal latches Column Address on the positive edge of the clock. This signal also allows Column access. |
| CKE[5:0] | O CMOS | V_3 | **SDRAM Clock Enable (SDRAM):** SDRAM clock enable pin. When these signals are de-asserted, SDRAM enters power-down mode. **Each row is individually controlled by its own clock enable.** |
| MD[63:0] | I/O CMOS | V_3 | **Memory Data:** These signals are connected to the DRAM data bus. They are not terminated on the Intel Mobile Module. |

**NOTES:**

1.  DQMA signals are non-inverted now. Please refer to 82443BX Spec Update

2.  MAB[13] is a non-inverted address signal now. Please refer to 82443BX Spec Update.

### 3.1.3.    AGP (60 SIGNALS)

Table 3 lists the Intel Mobile Module's AGP interface signals.

#### Table 3. AGP Signal Descriptions

| Name | Type | Voltage | Description |
|---|---|---|---|
| GAD[31:0] | I/O<br><br>AGP | V_3 | **AGP Address/Data:** The standard AGP address and data lines. This bus functions in the same way as the PCI AD[31:0] bus. The address is driven with FRAME# assertion, and data is driven or received in following clocks. |
| GC/BE[3:0]# | I/O<br><br>AGP | V_3 | **AGP Command/Byte Enable:** This bus carries the command information during AGP cycles when PIPE# is being used. During an AGP write, this bus contains byte enable information. The command is driven with FRAME# assertion, and byte enables corresponding to supplied or requested data are driven on the following clocks. |
| GFRAME# | I/O<br><br>AGP | V_3 | **AGP Frame:** Not used during AGP transactions. Remains de-asserted by an internal pullup resistor. Assertion indicates the address phase of a PCI transfer. Negation indicates that one more data transfer is desired by the cycle initiator. |
| GDEVSEL# | I/O<br><br>AGP | V_3 | **AGP Device Select:** Same function as PCI DEVSEL#. Not used during AGP transactions. This signal is driven by the 443BX Host Bridge system controller when a PCI initiator is attempting to access DRAM. DEVSEL# is asserted at medium decode time. |
| GIRDY# | I/O<br><br>AGP | V_3 | **AGP Initiator Ready:** Indicates the AGP compliant target is ready to provide ALL write data for the current transaction. Asserted when the initiator is ready for a data transfer. |
| GTRDY# | I/O<br><br>AGP | V_3 | **AGP Target Ready:** Indicates the AGP compliant master is ready to provide ALL write data for the current transaction. Asserted when the target is ready for a data transfer. |
| GSTOP# | I/O<br><br>AGP | V_3 | **AGP Stop:** Same function as PCI STOP#. Not used during AGP transactions. Asserted by the target to request the master to stop the current transaction. |
| GREQ# | I<br><br>AGP | V_3 | **AGP Request:** AGP master requests for AGP. |
| GGNT# | O<br><br>AGP | V_3 | **AGP Grant:** Same function as on PCI. Additional information is provided on the ST[2:0] bus. PCI Grant: Permission is given to the master to use PCI. |
| GPAR | I/O<br><br>AGP | V_3 | **AGP Parity:** A single parity bit is provided over GAD[31:0] and GC/BE[3:0]. This signal is not used during AGP transactions. |
| PIPE# | I<br><br>AGP | V_3 | **Pipelined Request:** Asserted by the current master to indicate a full width address is to be queued by the target. The master queues one request each rising clock edge while PIPE# is asserted. |

**Table 3. AGP Signal Descriptions** (Continued)

| Name | Type | Voltage | Description |
|---|---|---|---|
| SBA[7:0] | I<br><br>AGP | V_3 | **Sideband Address:** This bus provides an additional conduit to pass address and commands to the 443BX Host Bridge System Controller from the AGP master. |
| RBF# | I<br><br>AGP | V_3 | **Read Buffer Full:** Indicates if the master is ready to accept previously requested low priority read data. |
| ST[2:0] | O<br><br>AGP | V_3 | **Status Bus:** Provides information from the arbiter to a AGP Master on what it may do. These bits only have meaning when GGNT is asserted. |
| ADSTB[B:A] | I/O<br><br>AGP | V_3 | **AD Bus Strobes:** Provide timing for double clocked data on the GAD bus. The agent that is providing data drives these signals. These are identical copies of each other. |
| SBSTB | I<br><br>AGP | V_3 | **Sideband Strobe:** Provides timing for a side-band bus. It is always driven by the agent driving SBA[7:0], i.e., by the AGP master. |

### 3.1.4. PCI (58 SIGNALS)

Table 4 lists the Intel Mobile Module's PCI interface signals.

**Table 4. PCI Signal Descriptions**

| Name | Type | Voltage | Description |
|---|---|---|---|
| AD[31:0] | I/O<br>PCI | V_3 | **Address/Data:** The standard PCI address and data lines. The address is driven with FRAME# assertion, and data is driven or received in following clocks. |
| C/BE[3:0]# | I/O<br>PCI | V_3 | **Command/Byte Enable:** The command is driven with FRAME# assertion, and byte enables corresponding to supplied or requested data are driven on the following clocks. |
| FRAME# | I/O<br>PCI | V_3 | **Frame:** Assertion indicates the address phase of a PCI transfer. Negation indicates that one more data transfers are desired by the cycle initiator. |
| DEVSEL# | I/O<br>PCI | V_3 | **Device Select:** This signal is driven by the 443BX Host Bridge when a PCI initiator is attempting to access DRAM. DEVSEL# is asserted at medium decode time. |
| IRDY# | I/O<br>PCI | V_3 | **Initiator Ready:** Asserted when the initiator is ready for data transfer. |
| TRDY# | I/O<br>PCI | V_3 | **Target Ready:** Asserted when the target is ready for a data transfer. |
| STOP# | I/O<br>PCI | V_3 | **Stop:** Asserted by the target to request the master to stop the current transaction. |

**Table 4. PCI Signal Descriptions** (Continued)

| Name | Type | Voltage | Description |
|------|------|---------|-------------|
| PLOCK# | I/O PCI | V_3 | **Lock:** Indicates an exclusive bus operation and may require multiple transactions to complete. When LOCK# is asserted, non-exclusive transactions may proceed. The 443BX supports lock for CPU initiated cycles only. PCI initiated locked cycles are not supported |
| REQ[4:0]# | I PCI | V_3 | **PCI Request:** PCI master requests for PCI. |
| GNT[4:0]# | O PCI | V_3 | **PCI Grant:** Permission is given to the master to use PCI. |
| PHOLD# | I PCI | V_3 | **PCI Hold:** This signal comes from the expansion bridge; it is the bridge request for PCI. The 443BX Host Bridge will drain the DRAM write buffers, drain the processor-to-PCI posting buffers, and acquire the host bus before granting the request via PHLDA#. This ensures that GAT timing is met for ISA masters. The PHOLD# protocol has been modified to include support for passive release. |
| PHLDA# | O PCI | V_3 | **PCI Hold Acknowledge:** This signal is driven by the 443BX Host Bridge to grant PCI to the expansion bridge. The PHLDA# protocol has been modified to include support for passive release. |
| PAR | I/O PCI | V_3 | **Parity:** A single parity bit is provided over AD[31:0] and C/BE[3:0]# |
| SERR# | I/O PCI | V_3 | **System Error:** The 443BX asserts this signal to indicate an error condition. Please refer to the *Intel 440BX AGPset* datasheet (Order Number 290633-001) for further information. |
| CLKRUN# | I/O D PCI | V_3 | **Clock Run:** An open-drain output and also an input. The 443BX Host Bridge requests the central resource (PIIX4E) to start or maintain the PCI clock by asserting CLKRUN#. The 443BX Host Bridge tri-states CLKRUN# upon deassertion of Reset (since CLK is running upon deassertion of Reset). |
| PCI_RST# | I CMOS | V_3 | **Reset:** When asserted, this signal asynchronously resets the 443BX Host Bridge. The PCI signals also tri-state, compliant with PCI Rev 2.1 specifications. |

### 3.1.5. PROCESSOR/PIIX4E SIDEBAND (8 SIGNALS)

Table 5 lists the Intel Mobile Module's processor and PIIX4E sideband signals at the connector interface. The voltage level for these signals is determined by V_CPUPU, which is supplied by the Intel Mobile Module.

**Table 5. Processor/PIIX4E Sideband Signal Descriptions**

| Name | Type | Voltage | Description |
|------|------|---------|-------------|
| FERR# | O CMOS | V_CPUPU | **Numeric Coprocessor Error:** This pin functions as a FERR# signal supporting coprocessor errors. This signal is tied to the coprocessor error signal on the processor and is driven by the processor to the PIIX4E. |
| IGNNE# | I D CMOS | V_CPUPU | **Ignore Error:** This open drain signal is connected to the ignore error pin on the processor and is driven by the PIIX4E. |
| INIT# | I D CMOS | V_CPUPU | **Initialization:** INIT# is asserted by the PIIX4E to the processor for system initialization. This signal is an open drain. |
| INTR | I D CMOS | V_CPUPU | **Processor Interrupt:** INTR is driven by the PIIX4E to signal the processor that an interrupt request is pending and needs to be serviced. This signal is an open drain. |
| NMI | I D CMOS | V_CPUPU | **Non-Maskable Interrupt:** NMI is used to force a non-maskable interrupt to the processor. The PIIX4E ISA bridge generates an NMI when either SERR# or IOCHK# is asserted, depending on how the NMI Status and Control Register is programmed. This signal is an open drain. |
| A20M# | I D CMOS | V_CPUPU | **Address Bit 20 Mask:** When enabled, this open drain signal causes the processor to emulate the address wraparound at one Mbyte which occurs on the Intel 8086 processor. |
| SMI# | I D CMOS | V_CPUPU | **System Management Interrupt:** SMI# is an active low synchronous output from the PIIX4E that is asserted in response to one of many enabled hardware or software events. The SMI# open drain signal can be an asynchronous input to the processor. However, in this chip set SMI# is synchronous to PCLK. |
| STPCLK# | I D CMOS | V_CPUPU | **Stop Clock:** STPCLK# is an active low synchronous open drain output from the PIIX4E that is asserted in response to one of many hardware or software events. STPCLK# connects directly to the processor and is synchronous to PCICLK. When the processor samples STPCLK# asserted it responds by entering a low power state (Quick Start). The processor will only exit this mode when this signal is de-asserted. |

### 3.1.6.    POWER MANAGEMENT/ GEYSERVILLE (11 SIGNALS)

Table 6 lists the Intel Mobile Module's Power Management signals. The SM_CLK and SM_DATA signals refer to the two-wire serial SMBus interface. Although this interface is currently used solely for the digital thermal sensor thermal sensor, there are reserved serial addresses for future use. See Section 4.7. for more details.

**Table 6. Power Management/Geyserville Signal Descriptions**

| Name | Type | Voltage | Description |
|---|---|---|---|
| SUS_STAT1# | I<br>CMOS | V_3ALWAYS* | **Suspend Status:** This signal connects to the SUS_STAT1# output of PIIX4E. It provides information on host clock status and is asserted during all suspend states. |
| VR_ON | I<br>CMOS | V_3S | **VR_ON:** Voltage regulator ON. This 3.3V (5V tolerant) signal controls the operation of the Intel Mobile Module's voltage regulator. VR_ON should be generated as a function of the PIIX4E SUSB# signal which is used for controlling the "Suspend State B" voltage planes. |
| VR_PWRGD | O | V_3S | **VR_PWRGD:** This signal is driven high by the Intel Mobile Module to indicate the voltage regulator is stable and is pulled low using a 131.6K resistor when inactive. It can be used in some combination to generate the system PWRGOOD signal. |
| BXPWROK | I<br>CMOS | V_3 | **Power OK to BX:** This signal must go active 1mS after the V_3 power rail is stable. |
| SM_CLK | I/O D<br>CMOS | V_3 | **Serial Clock:** This clock signal is used on the SMBUS interface to the digital thermal sensor. |
| SM_DATA | I/O D<br>CMOS | V_3 | **Serial Data:** Open-drain data signal on the SMBUS interface to the digital thermal sensor. |
| ATF_INT# | O D<br>CMOS | V_3 | **ATF Interrupt:** This signal is an open-drain output signal of the digital thermal sensor. |
| G_SUS_STAT1# | I<br>CMOS | V_3 | **G_SUS_STAT1#:** The SUS_STST1# signal gated by the Geyserville control logic. G_SUS_STAT1# should be used in place of the SUS_STAT1# signal in the system electronics design. This signal is not implemented on the current Intel Mobile Modules, and is defined for future upgradeability purposes only. |
| G_LO/HI# | I<br>CMOS | V_3 | New signal from a PIIX4E GPIO pin that defines entry into a Geyserville state change to the Geyserville control logic. |
| G_CPU_STP# | I<br>CMOS | V_3 | The CPU_STP# signal gated by the Geyserville control logic. |
| VRChgng# | O<br>CMOS | V_3 | A Geyserville control logic signal that indicates that the actual state change is in progress. The VR setpoint has changed and the VR is settling. When this signal de-asserts the new state is sent to the processor. System electronics will use this signal to generate an SCI to force a transition out of deep sleep. |

**NOTE:**
*    V_3ALWAYS: 3.3V voltage supply. It is generated whenever V_DC is available and supplied to PIIX4E resume well.

### 3.1.7. CLOCK (9 SIGNALS)

Table 7 lists the Intel Mobile Module's clock signals.

**Table 7. Clock Signal Descriptions**

| Name | Type | Voltage | Description |
|------|------|---------|-------------|
| PCLK | I<br>PCI | V_3S | **PCI Clock In:** PCLK is an input to the module is one of the system's PCI clocks. This clock is used by all of the 443BX Host Bridge logic in the PCI clock domain. This clock is stopped when the PIIX4E PCI_STP# signal is asserted and/or during all suspend states. |
| HCLK[1:0] | I<br>CMOS | V_CLK | **Host Clock In:** Only HCLK0 is an input to the MMC-2 module from the CK100-M clock source and is used by the processor and 443BX Host Bridge system controller.  HCLK0 is the only clock input supplied to the module.  This clock is stopped when the PIIX4E CPU_STP# signal is asserted and/or during all suspend states. |
| DCLKO | O<br>CMOS | V_3 | **SDRAM Clock Out:** 66 MHz SDRAM clock reference generated internally by the 443BX Host Bridge system controller onboard PLL. It feeds an external buffer that produces multiple copies for the SODIMMs. |
| DCLKRD | I<br>CMOS | V_3 | **SDRAM Read Clock:** Feedback reference from the SDRAM clock buffer. This clock is used by 443BX Host Bridge System Controller when reading data from the SDRAM array. |
| DCLKWR | I<br>CMOS | V_3 | **SDRAM Write Clock:** Feedback reference from the SDRAM clock buffer. This clock is used by the 443BX Host Bridge system controller when writing data to the SDRAM array. |
| GCLKIN | I<br>CMOS | V_3 | **AGP Clock In:** The GCLKIN input is a feedback reference from the GCLKO signal. |
| GCLKO | O<br>CMOS | V_3 | **AGP Clock Out:** This signal is generated by the 443BX Host Bridge system controller onboard PLL from the HCLK0 host clock reference. The frequency of GCLKO is 66 MHz. The GCLKO output is used to feed both the PLL reference input pin on the 443BX Host Bridge system controller and the AGP device. The board layout must maintain complete symmetry on loading and trace geometry to minimize AGP clock skew. |
| FQS | O<br>CMOS | V_3S | **Frequency Select:** This output indicates the desired host clock frequency for the module.<br><br>FQS=0 indicates 66 MHz<br><br>**FQS=1 indicates RESERVED** |

### 3.1.8.    VOLTAGES (54 SIGNALS)

Table 8 lists the Intel Mobile Module's voltage signal definitions.

**Table 8. Voltage Descriptions**

| Name | Type | Number | Description |
|------|------|--------|-------------|
| V_DC | I | 20 | **DC Input:** 5 - 21V |
| V_3S | I | 9 | **SUSB# controlled 3.3V:** Power-managed 3.3V voltage supply. An output of the voltage regulator on the system electronics. This rail is off during STR, STD, and Soff. |
| V_5 | I | 3 | **SUSC# controlled 5V:** Power-managed 5V voltage supply. An output of the voltage regulator on the system electronics. This rail is off during STD and Soff. |
| V_3 | I | 16 | **SUSC# controlled 3.3V:** Power-managed 3.3V voltage supply. An output of the voltage regulator on the system electronics. This rail is off during STD and Soff. |
| VCCAGP | I | 4 | **AGP I/O Voltage:** For this revision of the module, this rail must be connected to V_3. |
| V_CPUPU | O | 1 | **Processor I/O Ring:** Driven by the Intel Mobile Module to power processor interface signals such as the PIIX4E open-drain pullups for the processor/PIIX4E sideband signals. |
| V_CLK | O | 1 | **Processor Clock Rail:** Driven by the Intel Mobile Module to power CK100-M VDDCPU rail. |

### 3.1.9.    ITP/JTAG (9 SIGNALS)

Table 9 lists the Intel Mobile Module's ITP/JTAG signals, which the system electronics can use to implement a JTAG chain and ITP port, if desired. The definition of the ITP interface has changed between the Pentium processor and Mobile Pentium II processor generations.

**Table 9. ITP/JTAG Pins**

| Name | Type | Voltage | Description |
|------|------|---------|-------------|
| TDO | O | V_CPUPU | **JTAG Test Data Out:** Serial output port. TAP instructions and data are shifted out of the processor from this port. |
| TDI | I | V_CPUPU | **JTAG Test Data In:** Serial input port. TAP instructions and data are shifted into the processor from this port. |
| TMS | I | V_CPUPU | **JTAG Test Mode Select:** Controls the TAP controller change sequence. |
| TCLK | I | V_CPUPU | **JTAG Test Clock:** Testability clock for clocking the JTAG boundary scan sequence. |
| TRST# | I | V_CPUPU | **JTAG Test Reset:** Asynchronously resets the TAP controller in the processor. |
| FS_RESET# | O | GTL+ | **Processor Reset:** Processor reset status to the ITP. |
| VTT | O | V_Core | **GTL+ Termination Voltage:** Used by the POWERON pin on the ITP debug port to determine when target system is on. POWERON pin is pulled up using a 1KΩ resistor to VTT. |
| FS_PREQ# | I | V_CPUPU | **Debug Mode Request:** Driven by the ITP - makes request to enter debug mode. |
| FS_PRDY# | O | GTL+ | **Debug Mode Ready:** Driven by the processor - informs the ITP that the processor is in debug mode. |

**NOTE:**

Recommendation: DBREST# (reset target system) on the ITP debug port can be "logically AND'ed" with the signal VR_PWRGD and connected to the PIIX4E input PWROK.

### 3.1.10.    MISCELLANEOUS (82 SIGNALS)

Table 10 lists the Intel Mobile Module's miscellaneous signal pins.

**Table 10. Miscellaneous Pins**

| Name | Type | Number | Description |
|---|---|---|---|
| Module ID[3:0] | O<br><br>CMOS | 4 | **Module Revision ID**: These pins track the revision level of the processor module. A 100K pull up resistor to V_3S is required on these signals and to be placed on the system electronics for these signals. |
| Ground | I | 45 | Ground |
| Reserved | RSVD | 33 | Unallocated Reserved pins and should not be connected. |

## 3.2. Connector Pin Assignments

Table 11 and Table 12 list the signals for each pin of the connector from the Intel Mobile Module to the system electronics. Refer to Section 3.3. for the pin assignments of the pads on the connector.

**Table 11. Connector Pin Assignments**

| Pin# | Row A | Row B | Row C | Row D | Row E |
|------|-------|-------|-------|-------|-------|
| 1 | SBA5 | ADSTBB | Gnd | GAD31 | SBA7 |
| 2 | GAD25 | GAD24 | SBA6 | SBA4 | SBA0 |
| 3 | GAD30 | GAD29 | GAD26 | GAD27 | Gnd |
| 4 | Gnd | VCCAGP | GAD4 | GAD6 | GAD8 |
| 5 | RBF# | GAD1 | GAD3 | GAD5 | GC/BE0# |
| 6 | BXPWROK | Reserved | GAD2 | ADSTBA | Gnd |
| 7 | MD0 | MD1 | V_3 | CLKRUN# | GAD7 |
| 8 | MD2 | MD33 | Gnd | MD32 | GAD0 |
| 9 | MD36 | MD4 | MD3 | MD35 | MD34 |
| 10 | MD7 | MD38 | MD37 | MD6 | MD5 |
| 11 | MD41 | MD42 | MD40 | MD39 | MD8 |
| 12 | MD43 | MD11 | Gnd | MD10 | MD9 |
| 13 | MD14 | MD45 | MD44 | MD13 | MD12 |
| 14 | MECC4 | MECC0 | MD15 | MD47 | MD46 |
| 15 | SCASA# | WEA# | MECC5 | Reserved | Gnd |
| 16 | Gnd | MID1 | DQMA0 | DQMA1 | Reserved |
| 17 | V_3 | DQMA4 | MID0 | DQMA5 | CSA0# |
| 18 | CSA1# | CSA2# | CSA4# | CSA3# | Gnd |
| 19 | SRASA# | CSA5# | MAB0# | MAB1# | Reserved |
| 20 | Reserved | Reserved | MAB2# | Reserved | MAB3# |
| 21 | Reserved | MAB4# | Gnd | Reserved | MAB6# |
| 22 | Reserved | Reserved | MAB5# | Reserved | MAB7# |
| 23 | MAB8# | Reserved | Reserved | MAB9# | MAB10 |
| 24 | Reserved | MAB11# | MAB12# | Reserved | DCLKO |
| 25 | MAB13 | V_3 | Gnd | CKE0 | DCLKRD |

**Table 11. Connector Pin Assignments** (Continued)

| Pin# | Row A | Row B | Row C | Row D | Row E |
|------|-------|-------|-------|-------|-------|
| 26 | CKE1 | MID2 | CKE3 | CKE4 | Gnd |
| 27 | CKE5 | CKE2 | MID3 | G_CPU_STP# | VRChgng# |
| 28 | Reserved | G_LO/HI# | DQMA2 | DCLKWR | Gnd |
| 29 | Gnd | VTT | Reserved | FS_PREQ# | DQMA3 |
| 30 | FS_RESET# | V_3 | MD26 | Gnd | MD25 |
| 31 | FS_PRDY# | Gnd | MD58 | MD57 | MD60 |
| 32 | G_SUS_STAT1# | SMCLK | TDO | TCLK | FERR# |
| 33 | Reserved | SMDAT | TDI | TMS | IGNNE# |
| 34 | Reserved | FQS | Reserved | TRST# | ATF_INT# |
| 35 | Reserved | V_5 | V_3S | V_3S | V_3S |
| 36 | V_CPUPU | V_5 | V_3S | V_3S | V_3S |
| 37 | V_CLK | V_5 | V_3S | V_3S | V_3S |
| 38 | Reserved | Reserved | Reserved | Reserved | Reserved |
| 39 | V_DC | V_DC | V_DC | V_DC | V_DC |
| 40 | V_DC | V_DC | V_DC | V_DC | V_DC |

**Table 12. Connector Pin Assignments**

| Pin# | Row F | Row G | Row H | Row J | Row K |
|------|-------|-------|-------|-------|-------|
| 1 | GREQ# | Gnd | PIPE# | SBA3 | Gnd |
| 2 | ST0 | ST1 | SBA1 | SBSTB | GCLKI |
| 3 | GGNT# | ST2 | SBA2 | Gnd | GCLKO |
| 4 | GAD13 | GSTOP# | GAD16 | GAD20 | GAD23 |
| 5 | GAD12 | GPAR | GAD18 | GAD17 | GC/BE3# |
| 6 | GAD10 | GAD15 | GFRAME# | Gnd | GAD22 |
| 7 | GAD11 | GC/BE1# | GTRDY# | GC/BE2# | GAD21 |
| 8 | GAD9 | GAD14 | GDEVSEL# | GIRDY# | GAD19 |
| 9 | Gnd | VCCAGP | Gnd | VCCAGP | GAD28 |
| 10 | AD0 | AD4 | AD2 | AD3 | AD1 |
| 11 | Gnd | C/BE0# | AD6 | Gnd | AD5 |

**Table 12. Connector Pin Assignments** (Continued)

| Pin# | Row F | Row G | Row H | Row J | Row K |
|------|-------|-------|-------|-------|-------|
| 12 | VCCAGP | AD10 | AD7 | AD8 | AD9 |
| 13 | MECC1 | AD13 | Gnd | AD12 | AD11 |
| 14 | SERR# | PAR | AD15 | C/BE1# | AD14 |
| 15 | AD16 | TRDY# | STOP# | DEVSEL# | PLOCK# |
| 16 | AD19 | Gnd | AD17 | Gnd | AD18 |
| 17 | AD23 | AD30 | AD24 | C/BE2# | AD21 |
| 18 | AD27 | AD22 | C/BE3# | AD26 | PCLK |
| 19 | PCI_RST# | Gnd | AD20 | AD28 | Gnd |
| 20 | Reserved | PHOLD# | AD31 | AD29 | AD25 |
| 21 | IRDY# | FRAME# | Gnd | REQ1# | REQ0# |
| 22 | Gnd | GNT2# | REQ2# | REQ3# | GNT3# |
| 23 | GNT1# | GNT4# | GNT0# | REQ4# | Gnd |
| 24 | Gnd | PHLDA# | Gnd | V_3 | MD59 |
| 25 | DQMA6 | MECC7 | MD50 | MD51 | MD54 |
| 26 | MECC2 | MD48 | MD18 | MD52 | MD24 |
| 27 | DQMA7 | MD16 | MD19 | Gnd | MD23 |
| 28 | MECC6 | MD17 | MD21 | MD53 | MD55 |
| 29 | MECC3 | MD49 | MD20 | MD22 | MD56 |
| 30 | MD27 | MD28 | Gnd | MD62 | MD63 |
| 31 | Gnd | MD29 | MD61 | MD30 | MD31 |
| 32 | SMI# | INTR | VR_ON | Gnd | Gnd |
| 33 | NMI | SUS_STAT1# | VR_PWRGD | Gnd | HCLK0 |
| 34 | A20M# | STPCLK# | INIT# | Gnd | Gnd |
| 35 | V_3 | V_3 | V_3 | Gnd | HCLK1 |
| 36 | V_3 | V_3 | V_3 | Gnd | Gnd |
| 37 | V_3 | V_3 | V_3 | V_3 | V_3 |
| 38 | Reserved | Reserved | Reserved | Reserved | Reserved |
| 39 | V_DC | V_DC | V_DC | V_DC | V_DC |
| 40 | V_DC | V_DC | V_DC | V_DC | V_DC |

## 3.3.    Pin and Pad Assignments

The Intel Mobile Module connector is a surface mount, 1.27 mm pitch BGA style, 400-pin connector. There are currently three unique mating connectors that are offered by vendors for the Intel Mobile Module. Please check with your local Intel sales representative for additional information.

Figure 2 shows the connector pad assignments for the manufacturer's system electronics. This footprint is viewed from the secondary side of the processor module (the side of the printed circuit board on which the 400-pin connector is soldered).



**400-Pin Connector**
**OEM Pad Assignments**
(Viewed from Secondary Side)
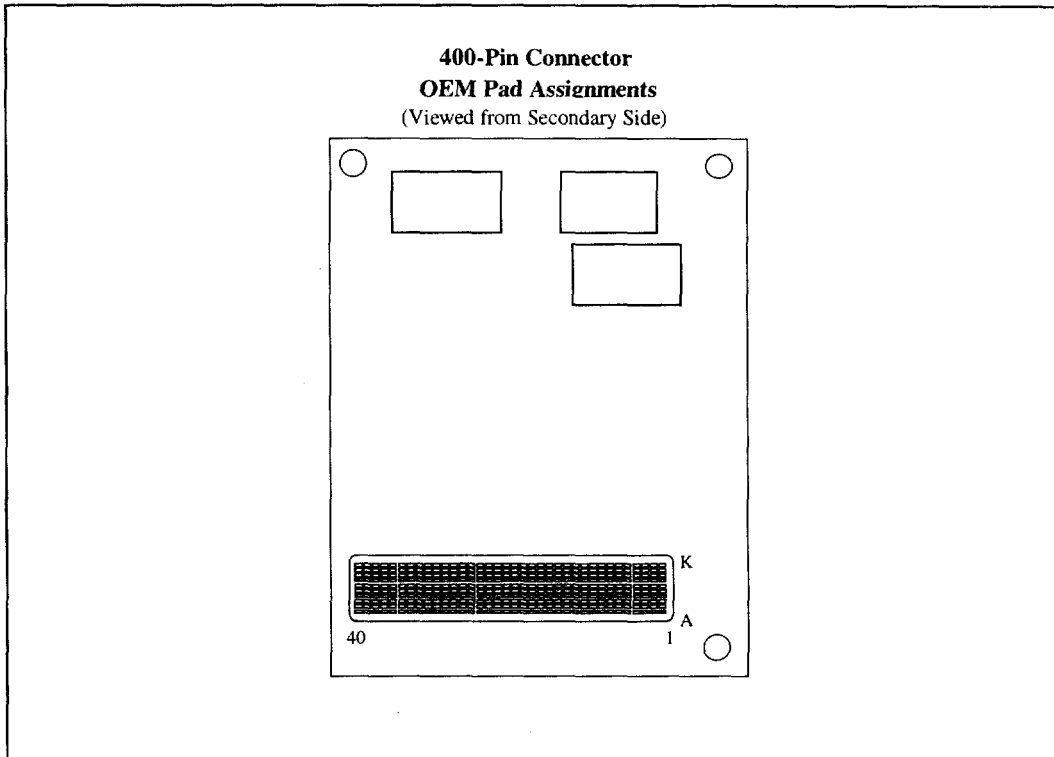
**Figure 2. 400-Pin Connector Footprint Pad Numbers, Module Secondary Side**

**Table 13. Connector Specifications**

| Parameter | Condition | Specification |
|---|---|---|
| Material | Contact | Copper Alloy |
| | Housing | Thermo Plastic Molded Compound: LCP |
| Electrical | Current | 0.5 A |
| | Voltage | 50 VAC |
| | Insulation Resistance | 100MΩ min. @ 500 VDC |
| | Termination Resistance | 20mΩ max. @ 20mV open circuit with 10mA |
| | Capacitance | 5pF max. Per contact |
| Mechanical | Mating Cycles | 50 cycles |
| | Connector Mating Force | 0.9N (90gf) max. Per contact |
| | Contact Un-mating Force | 0.1N (10gf) min. Per contact |

Table 13 summarizes some of the more critical specifications for the connector.

## 4.0. FUNCTIONAL DESCRIPTION

### 4.1. Intel Mobile Module

The Intel Mobile Module supports the Mobile Pentium II processor core running at 66/233, 66/266, and 66/300 MHz with 32 KB L1 code and data cache sizes.

### 4.2. L2 Cache

The Mobile Pentium II processor core's internal cache is complimented with a second-level cache using a high-performance pipeline burst SRAM which uses a dedicated high speed bus into the processor core. The L2 cache can support 512 MB of system memory, while the maximum amount of cacheable system memory supported by the 443BX Host Bridge system controller is 256 MB with 16 Mbit DRAMs. (The system controller can support up to 1 GB of system memory using 64 Mbit technology.) The Intel Mobile Module has two 100-pin TQFP footprints for 512K direct-mapped write-back L2 cache.

The Intel Mobile Module supports the "Stop Clock" mode of power management for the L2 SRAMs. In this mode, the clock signals to the synchronous SRAMs are stopped or "parked" in a low power state.

### 4.3. 443BX Host Bridge System Controller

Intel's 443BX Host Bridge system controller is a highly integrated device that combines the Mobile Pentium II processor bus controller, the DRAM controller, and the PCI bus controller into one component. The 443BX Host Bridge has multiple power management features designed specifically for notebook systems:

- CLKRUN# is a feature that enables controlling of the PCI clock on or off

- 443BX Host Bridge suspend modes include Suspend-to-RAM (STR), Suspend-to-Disk (STD) and Powered-On-Suspend (POS)

- System Management RAM (SMRAM) power management modes include Compatible SMRAM (C_SMRAM) and Extended SMRAM (E_SMRAM). C_SMRAM is the traditional SMRAM feature implemented in all Intel PCI chipsets. E_SMRAM is a new feature that supports write-back cacheable SMRAM space up to 1Mbyte. To minimize power consumption while the system is idle, the internal 443BX Host Bridge clock is turned off (gated off) when there is no processor and PCI activity.

The Intel Mobile Module supports only the 443BX
Host Bridge features in mobile "compatible" or legacy
mode. Refer to Intel's latest revision of the 443BX
Host Bridge specification for complete details.

### 4.3.1.    MEMORY ORGANIZATION

The complete memory interface of the 443BX Host
Bridge is available at the Intel Mobile Module's
connector; all of the 443BX Host Bridge standard
Mode memory configurations and modes of operation
are supported on the MMC-2 signaling interface. This
allows the memory interface to support the following:

- One set of memory control signals, sufficient to
  support up to three SO_DIMM sockets and six
  banks of SDRAM at 66 MHz
- One CKE signal for each banks

Key memory features not supported by the 443BX
Host Bridge system controller standard MMC-2 Mode
are:

- Support for 8 banks of memory
- Second set of memory address lines (MAA[13:0])
- 100 MHz SDRAM (and Front Side Bus)

DRAM technologies supported by 443BX Host
Bridge system controller include Extended Data Out
(EDO) and SDRAM. These memory types may not
be mixed in the system. In other words, all DRAM in

all rows (RAS[5:0]#) must be of the same technology.
The 443BX Host Bridge system controller targets
60ns EDO DRAMs. and 66 MHz SDRAMs.

The Intel Mobile Module's clocking architecture
supports the use of SDRAM. Due to the tight timing
requirements of 66-MHz SDRAM clocks, the clocking
mode for SDRAM or system manufacturer custom
memory configurations allows all host and SDRAM
clocks to be generated from the same clocking
architecture on the OEM's system electronics. For
complete details about using SDRAM memory, and
for trace length guidelines, please contact your local
Intel sales representative for the latest updates.

For details on memory device support, organization,
size and addressing, refer to the *Intel 440BX AGPset*
datasheet (Order Number 290633-001).

### 4.3.2.    RESET STRAP OPTIONS

The 443BX Host Bridge system controller has
several strap options on the memory address bus
which define the behavior of the device after reset.
For the Intel Pentium II Processor Mobile Module,
several of these strap options are implemented on
the module.

Other straps are allowed to override the default
settings. Table 14 shows the various straps and how
they are handled by the Intel Pentium II Processor
Mobile Module (MMC-2.)

**Table 14. Configuration Straps for 443BX Host Bridge System Controller**

| Signal | Function | Module Default Setting | Optional Override on System Electronics |
|---|---|---|---|
| MAB[12]# | Host Frequency Select | No strap. (66 MHz default) | None |
| MA[11]# | In order queue depth | No strap. (Maximum Queue Depth is set (i.e., 8)) | None |
| MA[10] | Quick Start Select | Strapped high on the module for Quick Start mode. | None |
| MA[9]# | AGP disable | No strap. AGP is enabled | Pull up this signal to disable AGP interface. |
| MA[7]# | MM Config | No strap. Standard (MMC-2) mode. | None |
| MA[6]# | Host Bus Buffer Mode Select | Strapped high on the module for mobile FSB buffers. | None |

### 4.3.3. PCI INTERFACE

The 443BX Host Bridge system controller is compliant with the PCI 2.1 specification, which improves the worst-case PCI bus access latency from earlier PCI specifications. The complete PCI interface of the 443BX Host Bridge is available at the Intel Pentium II Processor Mobile Module connector. The 443BX Host Bridge supports the PCI Clockrun protocol for PCI bus power management. In this protocol, PCI devices assert the CLKRUN# open-drain signal when they require the use of the PCI interface. (Refer to the PCI Mobile Design Guide for complete details on the PCI Clockrun protocol.)

The 443BX Host Bridge is responsible for arbitrating the PCI bus. Since the Intel Pentium II Processor Mobile Module is configured in Mobile Module Connector 2 (MMC-2) Mode, the 443BX Host Bridge can support only up to five PCI bus masters. There are five PCI Request/Grant pairs, REQ[4:0]# and GNT[4:0]#, available on the connector to the manufacturer's system electronics.

The PCI interface on MMC2 is 3.3V only. 5V PCI devices are not supported, specifically all devices which drive outputs to a 5 volt nominal Voh level.

The 443BX Host Bridge supports only Mechanism #1 for accessing PCI configuration space, as detailed in the PCI specification. This implies that signals AD[31:11] are available for PCI IDSEL signals. However, since the 443BX Host Bridge is always device #0; AD11 will never be asserted during PCI configuration cycles as an IDSEL. AD12 is reserved by the 443BX for the AGPbus. Thus, AD13 is the first

available address line usable as an IDSEL. AD18 is recommended to be used by the PIIX4E South Bridge.

### 4.3.4. AGP INTERFACE

The 443BX Host Bridge system controller is compliant with the AGP Rev 1.0 specification, which supports only an asynchronous AGP interface coupling to the 443BX core frequency. The AGP interface can reach a theoretical ~500 Mbytes/sec transfer rate (i.e., using AGP 2X/133 devices). The actual bandwidth will be limited by the capability of the 443BX memory subsystem.

## 4.4. Electrical Requirements

The following section provides information on the DC requirements for the Pentium II Processor Mobile Module.

### 4.4.1. DC REQUIREMENTS

Please refer to Table 15 for power supply design criteria to ensure compliance with the Pentium II Processor Mobile Module DC power requirements.

Table 16 contains the power supply design requirements to ensure proper operation of the future Pentium II Processor Mobile Modules. Please note, this does not apply to the current products **233/266/300 MHz Pentium II Processor Mobile Modules** included in this version of specifications.

### 4.4.2.   AC REQUIREMENTS

Please refer to Table 17 for Pentium II processor module AC timing requirements for BCLK.

BCLK system timing is specified in terms of signal quality. The waveform of Figure 6 describes a typical system bus clock as seen at the processor core pin. Contact your intel sales representative to obtain complete information on proper probe points for timing measurements.

**Table 15. Pentium® II Processor Mobile Module Power Requirements**

| Voltage Plane | Minimum Voltage | Typical Voltage | Absolute Maximum Voltage | DC Minimum Operating Current | DC Typical Operating Current | DC Maximum Operating Current | Instan-taneous Peak Current | Leakage[3] Typical 25°C |
|---|---|---|---|---|---|---|---|---|
| V_DC | 5.0 V | 12.0 V[4] | 21.0 V | 75 mA | 0.6 A[1] | 2.85 A[2] | 14.2 A | 4.0 uA |
| V_5 | 4.75 V | 5.0 V | 5.25 V | 13 mA | 32 mA | 60 mA | 500 mA | 1 uA |
| V_3 | 3.135 V | 3.3 V | 3.465 V | 0.2 A | 0.7 A | 1.60 A | 2.0 A | 1.1 mA |
| V_3S | 3.135 V | 3.3 V | 3.465 V | 30 mA | 0.2 A | 0.52 A | 0.7 A | 2 uA |
| V_CPUPU | 2.375 V | 2.5 V | 2.625 V | 0.0 mA[4] | 10 mA[4] | 20 mA | NA | NA |
| V_CLK | 2.375 V | 2.5 V | 2.625 V | 24 mA[4] | 35 mA[4] | 80 mA | NA | NA |

**NOTES:**
1.  V_DC is set for 18V in order to determine typical V_DC current.
2.  V_DC is set for 5V in order to determine Maximum Operating V_DC current.
3.  Leakage current that can be expected when VR_ON is deactivated and V_DC is still applied.
4.  These values are OEM system dependent.

**Table 16. FUTURE Mobile Module Family Power Requirements**

| Voltage Plane | Minimum Voltage | Typical Voltage | Absolute Maximum Voltage | DC Minimum Operating Current | DC Typical Operating Current | DC Maximum Operating Current | Instan-taneous Peak Current | Leakage[3] Typical 25°C |
|---|---|---|---|---|---|---|---|---|
| V_DC | 5.0 V | 12.0 V[4] | 21.0 V | 100 mA | 0.9 A[1] | 3.5 A[2] | 17.3 A | 4.0 uA |
| V_5 | 4.75 V | 5.0 V | 5.25 V | 17 mA | 32 mA | 60 mA | 600 mA | 1 uA |
| V_3 | 3.135 V | 3.3 V | 3.465 V | 0.8 A | 1.2 A | 2.0 A | 2.8 A | 1.1 mA |
| V_3S | 3.135 V | 3.3 V | 3.465 V | 52 mA | 0.22 A | 0.7 A | 0.9 A | 2 uA |
| V_CPUPU | 2.375 V | 2.5 V | 2.625 V | 0.0 mA[4] | 10 mA[4] | 20 mA | NA | NA |
| V_CLK | 2.375 V | 2.5 V | 2.625 V | 24 mA[4] | 35 mA[4] | 80 mA | NA | NA |

NOTES:
1. V_DC is set for 18V in order to determine typical V_DC current.
2. V_DC is set for 5V in order to determine Maximum Operating V_DC current.
3. Leakage current that can be expected when VR_ON is deactivated and V_DC is still applied.
4. These values are OEM system dependent.

### 4.4.3.    AC REQUIREMENTS

Table 17 lists the Pentium II Processor Mobile Module AC requirements for BCLK.

**Table 17. Pentium® II Processor Mobile Module AC Specifications (BCLK) at the Processor Core Pins [1, 2, 3]**

| T# | Parameter | Min | Nom | Max | Unit | Figure | Notes |
|---|---|---|---|---|---|---|---|
| | System Bus Frequency | | 66.67 | | MHz | | All processor core frequencies [4] |
| T1: | BCLK Period | | 15. | | ns | | 4, 5, 6 |
| T2: | BCLK Period Stability | | | ±250 | ps | | 6, 7, 8, 9 |
| T3: | BCLK High Time | 5.3 | | | ns | | @>1.765V [6] |
| T4: | BCLK Low Time | 5.3 | | | ns | | @<0.5V [6] |
| T5: | BCLK Rise Time | 0.175 | | 0.875 | ns | | (0.9V-1.6V) [6, 9] |
| T6: | BCLK Fall Time | 0.175 | | 0.875 | ns | | (1.6V–0.9V) [6, 9] |

**NOTES:**

1. Unless otherwise noted, all specifications in this table apply to all Intel Pentium® II Processor Mobile Modules.

2. All AC timings for the GTL+ signals are referenced to the BCLK rising edge at 1.25V at the processor core pin. All GTL+ signal timings (address bus, data bus, etc.) are referenced at 1.00V at the processor core pins.

3. All AC timings for the CMOS signals are referenced to the BCLK rising edge at 1.25V at the processor core pin. All CMOS signal timings (compatibility signals, etc.) are referenced at 1.25V at the processor core pins.

4. The internal core clock frequency is derived from the system bus clock. The system bus clock to core clock ratio is determined during initialization as described and is predetermined by the Intel Mobile Module.

5. The BCLK period allows a +0.5 ns tolerance for clock driver variation. See the *CK97 Clock Synthesizer/Driver Specification* for further information.

6. This specification applies to the Pentium II processor system bus frequency of 66 MHz.

7. Due to the difficulty of accurately measuring clock jitter in a system, it is recommended that a clock driver be used that is designed to meet the period stability specification into a test load of 10 to 20 pF. This should be measured on the **rising edges of adjacent BCLKs crossing 1.25V at the processor core pin**. The jitter present must be accounted for as a component of BCLK timing skew between devices.

8. The clock driver's closed loop jitter bandwidth must be set low to allow any PLL-based device to track the jitter created by the clock driver. The –20 dB attenuation point, as measured into a 10 to 20 pF load, should be less than 500 kHz. This specification may be ensured by design characterization and/or measured with a spectrum analyzer. See the *CKDM66-M Clock Synthesizer/Driver Specification* for further details.

9. Not 100% tested. Specified by design characterization as a clock driver requirement.

**4.4.3.1. System Bus Clock (BCLK) Signal Quality Specifications and Measurement Guidelines**

Table 18 describes the signal quality specifications at the processor core for the Pentium II Processor

Mobile Module system bus clock (BCLK) signal. Figure 3 describes the signal quality waveform for the system bus clock at the processor core pins.

**Table 18. BCLK Signal Quality Specifications for Simulation at the Processor Core [1]**

| T# | Parameter | Min | Nom | Max | Unit | Figure | Notes |
|---|---|---|---|---|---|---|---|
| V1: | BCLK $V_{IL}$ | | | 0.5 | V | 3 | |
| V2: | BCLK $V_{IH}$ | 1.765 | | | V | 3 | 2 |
| V3: | $V_{IN}$ Absolute Voltage Range | –0.8 | | 3.3 | V | 3 | 2 |
| V4: | Rising Edge Ringback | 1.765 | | | V | 3 | 3, 4 |
| V5: | Falling Edge Ringback | | | 0.5 | V | 3 | 4 |
| | | | | | | | |

**NOTES:**

1. Unless otherwise noted, all specifications in this table apply to all Intel Pentium® II Processor Mobile Modules.

2. This is the Pentium II processor system bus clock overshoot and undershoot specification for 66-MHz system bus operation.

3. Clock signal must be monotonic from +0.5V to +1.765V.

4. The rising and falling edge ringback voltage specified is the minimum (rising) or maximum (falling) absolute voltage the BCLK signal can dip back to after passing the $V_{IH}$ (rising) or $V_{IL}$ (falling) voltage limits. This specification is an absolute value.
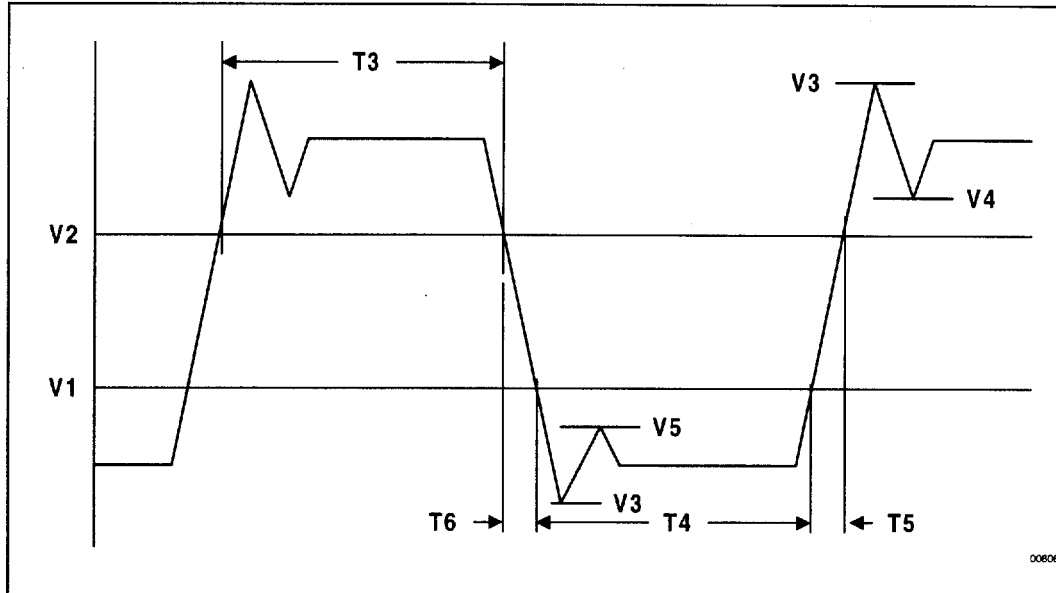
**Figure 3. BCLK, TCK, PICCLK Generic Clock Waveform at the Processor Core Pins**

## 4.5. Pentium® II Processor Mobile Module Signal Termination

System design requirements for signal termination for the Intel Mobile Module have been split between the processor module and the system electronics. The OEM system designer is responsible for ensuring proper termination on the signals.

## 4.6. Processor Core Voltage Regulation

The Intel Mobile Module's DC voltage regulator (DC/DC converter) is designed to support the core voltage and I/O ring voltage for current and future processors. The DC voltage regulator provides the appropriate Mobile Pentium II processor core voltage, the processor sideband signal pull-up voltage, and the I/O voltage for the components on the processor core backside bus. Of these voltages,

only the processor sideband pull-up voltage (V_CPUPU) is delivered to the system electronics.

The Intel Mobile Module supports an input DC voltage range of 5V - 21V from the system battery, or power supply.

### 4.6.1. VOLTAGE REGULATOR EFFICIENCY

There are three voltage regulators on the Intel Pentium II Processor Mobile Module. These voltage regulators generate the core voltage used by the CPU, the voltage for the backside bus, and the voltage for the CPU I/O ring voltage. The core voltage regulator provides the required current from the V_DC (battery or A/C voltage adapter) supply. Its relative efficiencies are shown in Table 19. The Backside bus I/O and CPU I/O ring voltage regulators tap the V_3 plane and are about 85 percent efficient at typical loads.

**Table 19. Typical Voltage Regulator Efficiency**

| Icore, A[3] | V_DC, V | I_DC, A[2] | Efficiency[1] | V_DC, V | I_DC, [2] | Efficiency[1] |
|---|---|---|---|---|---|---|
| 1 | 5.00 | 0.394 | 83% | 18.00 | 0.135 | 68% |
| 2 | 5.00 | 0.752 | 88% | 18.00 | 0.233 | 80% |
| 3 | 5.00 | 1.212 | 82% | 18.00 | 0.340 | 82% |
| 4 | 5.00 | 1.506 | 88% | 18.00 | 0.451 | 82% |
| 5 | 5.00 | 1.921 | 86% | 18.00 | 0.561 | 82% |
| 6 | 5.00 | 2.290 | 86% | 18.00 | 0.674 | 82% |
| 7 | 5.00 | 2.683 | 85% | 18.00 | 0.790 | 81% |
| 1 | 12.00 | 0.186 | 74% | 21.00 | 0.129 | 62% |
| 2 | 12.00 | 0.335 | 83% | 21.00 | 0.215 | 74% |
| 3 | 12.00 | 0.491 | 85% | 21.00 | 0.304 | 79% |
| 4 | 12.00 | 0.652 | 85% | 21.00 | 0.396 | 81% |
| 5 | 12.00 | 0.816 | 85% | 21.00 | 0.493 | 81% |
| 6 | 12.00 | 0.980 | 84% | 21.00 | 0.592 | 80% |
| 7 | 12.00 | 1.149 | 83% | 21.00 | 0.692 | 80% |

**NOTES:**

1. These efficiencies will change with future voltage regulators that accommodate wider ranges of input voltages.
2. With V_DC applied and the voltage regulator off, typical leakage is 0.3mA with a maximum of 0.7mA.
3. Icore indicates the CPU core current being drawn during test and measurement.

### 4.6.2. VOLTAGE REGULATOR CONTROL

The VR_ON pin on the connector allows a digital signal (3.3V, 5V safe) to control the voltage regulator. The system manufacturer can use this signal to turn the Intel Mobile Module's voltage regulator on or off. VR_ON should be controlled as a function of the same digital control signal (SUSB#) used to control the system's switched 5V/3.3V power planes. The PIIX4E South Bridge defines Suspend B as the power management state in which power is physically removed from the processor, L2 cache, 443BX Host Bridge, and voltage regulator. In this state, the SUSB# pin on the PIIX4E controls these power planes.

VR_ON should switch high only when the following conditions are met; V_5(s) => 4.5V, and V_DC => 4.75V. Turning on VR_ON prior to meeting these conditions will severely damage the Intel Mobile Module. See Figure 4 in Section 4.6.2.1. for the proper timing sequencing.

### CAUTION

VR_ON should switch high only when the following conditions are met: V_5(s) => 4.5V, and V_DC => 4.75V. Turning on VR_ON prior to meeting these conditions will severely damage the Intel Mobile Module.

### 4.6.2.1.   Voltage Signal Definition and Sequencing

**Table 20. Voltage Signal Definitions and Sequences**

| Signal | Source | Definitions and Sequences |
|---|---|---|
| V_DC | System Electronics | DC voltage driven from the power supply and is required to be between 5V and 21V DC. V_DC powers the Mobile Module's DC-to-DC converter for processor core and I/O voltages. The Intel Mobile Module cannot be hot inserted or removed while V_DC is powered on. |
| V_3 | System Electronics | V_3 is supplied by the system electronics for the 443BX. |
| V_5 | System Electronics | V_5 is supplied by the system electronics for the 443BX's 5V reference voltage and Intel Mobile Module's voltage regulator. |
| V_3S | System Electronics | V_3S is supplied by the system electronics for the L2 cache devices. Each must be powered off during system STR and STD states. |
| VR_ON | System Electronics | Enables the Mobile Module's voltage regulator circuit. When driven active high (3.3V) the voltage regulator circuit on the Mobile Module is activated. The signal driving VR_ON should be a digital signal with a rise/fall time of less than or equal to 1 µs. |
| V_CORE (also used as host bus GTL+ termination voltage VTT) | Intel Mobile Module Only; not on module interface. | A result of VR_ON being asserted, V_CORE is an output of the DC-DC regulator on the Mobile Module and is driven to the core voltage of the processor. It is also used as the host bus GTL+ termination voltage, known as VTT. |
| V_BSB_IO | Intel Mobile Module Only; not on module interface. | V_BSB_IO is 1.8V. The system electronics uses this voltage to power the L2 cache-to-processor interface circuitry. |
| VR_PWRGD | Intel Mobile Module | Upon sampling the voltage level of V_CORE for the processor, minus tolerances for ripple, VR_PWRGD is driven active high (3.3V) for the system electronics to sample prior to providing PWROK to the PIIX4E. If VR_PWRGD is not sampled active within 1 second of the assertion of VR_ON the system electronics should deassert VR_ON. |
| V_CPUPU | Intel Mobile Module | V_CPUPU is 2.5V. The system electronics uses this voltage to power the PIIX4E-to-processor interface circuitry. |
| V_CLK | Intel Mobile Module | V_CLK is 2.5V. The system electronics uses this voltage to power the HCLK_(0:1) drivers for the processor clock. |

Figure 4 details the sequencing of Signals and Voltage planes required for normal operation of the Intel Mobile Module.

The Intel Mobile Module provides the VR_PWRGD signal, which indicates that the voltage regulator power is operating at a stable voltage level. The system manufacturer should use this signal on the system electronics to control power inputs and to gate PWROK to the PIIX4E South Bridge.

**NOTE**

The VR_ON signal should be driven by a digital signal with a rise/fall time of less than or equal to 1us and signaling voltage levels that meet the requirement of Vil(max)=0.4V and Vih(min)=3.0V.



## POWER SEQUENCE TIMING

1. PWROK on I/O board should be active on when VR_PWRGD is active and V_3S is good.
2. CPU_RST from I/O board should be active for a minimum of 6 ms after PWROK is active and PLL_STP# and CPU_STP# are inactive. Note that PLL_STP# is an AND condition of RSMRST# and SUSB# on the PIIX4.
3. V_DC >= 4.7V, V_5>=4.5V, V_3S>=3.0V.
4. V_CPUPU and V_CLK are generated on the Intel Mobile Module.
5. This is the 5V power supplied to thep rocessor module connector. This should be the first 5V plane to power up.

**Figure 4. Power On Sequence Timing**

### 4.6.3. POWER PLANES: BULK CAPACITANCE REQUIREMENTS

In order to provide adequate filtering and in-rush current protection for any system design, bulk capacitance is required. A small amount of bulk capacitance is supplied on the Intel Pentium II Processor Mobile Module, however, in order to achieve proper filtering additional capacitance should be placed on the system electronics. Table 21 details the bulk capacitance requirements for the system electronics when using the Intel Pentium II Processor Mobile Module.

### 4.6.4. SURGE CURRENT STUDY

Surge current analysis was performed on a typical system power supply to determine the maximum amount of surge current that the Intel Mobile Module is capable of handling. This information was then used to develop the module system I/O bulk capacitance requirements (Table 21). This section provides is the results of this study.

Figure 5 shows an electrical model used when analyzing instantaneous power-on conditions. The following analysis is provided as a worst case analysis. Depending on the system electronics design, different impedances may be seen yielding different results. The OEM should perform a thorough analysis to understand the implications of surge current on their system.

As previously stated, the following study was performed in a "worst-case" situation with no bulk capacitance on the V_DC line on the system electronics. Given that, the Intel Mobile Module has two 4.7µf with an ESR of 0.3Ωs each. The Intel Mobile Module connector is approximately 30mΩ of series resistance for a total series resistance of .33Ω. If the user powers the system with the A/C adapter (18V), the amount of surge current seen by the capacitors on the module would be greater than 50Amps! Figure 6 illustrates the results of this situation with a SPICE simulation.

**Table 21. Capacitance Requirement Per Power Plane**

| Power Plane | Capacitance Requirements | ESR | Ripple Current | Rating |
|---|---|---|---|---|
| V_DC | 100uf, 0.1uf, 0.01uf [1] | 20mΩ | 1-3.5 Amp [3] | 20% tolerance @ 35V |
| V_5 | 100uf, 0.1uf, 0.01uf [1] | 100mΩ | 1 Amp | 20% tolerance @ 10V |
| V_3 | 470uf, 0.1uf, 0.01uf [1] | 100mΩ | 1 Amp | 20% tolerance @ 6V |
| V_3S | 100uf, 0.1uf, 0.01uf [1] | 100mΩ | 1 Amp | 20% tolerance @ 6V |
| VCC_AGP | 22uf, 0.1uf, 0.01uf [1] | 100mΩ | 1 Amp | 20% tolerance @ 6V |
| V_CPUPU | 2.2uf, 8200pf [2] | n/a | n/a | 20% tolerance @ 6V |
| V_CLK | 10uf, 8200pf [2] | n/a | n/a | 20% tolerance @ 6V |

**NOTES:**
1. Placement of above capacitance requirements should be located near the Mobile Module connector.
2. V_CLK filtering should be located next to the system clock synthesizer.
3. Ripple current specification depends on V_DC input. For 5.0V V_DC, a 3.5A device is required. For V_DC at 18V or higher, 1A is sufficient.
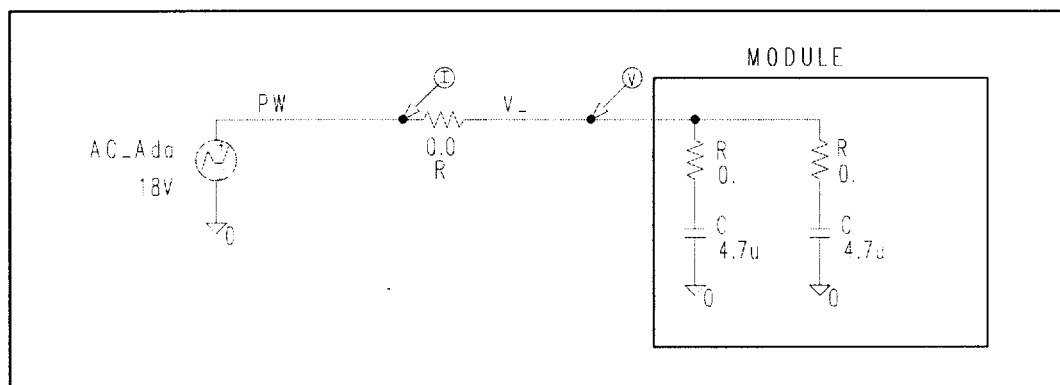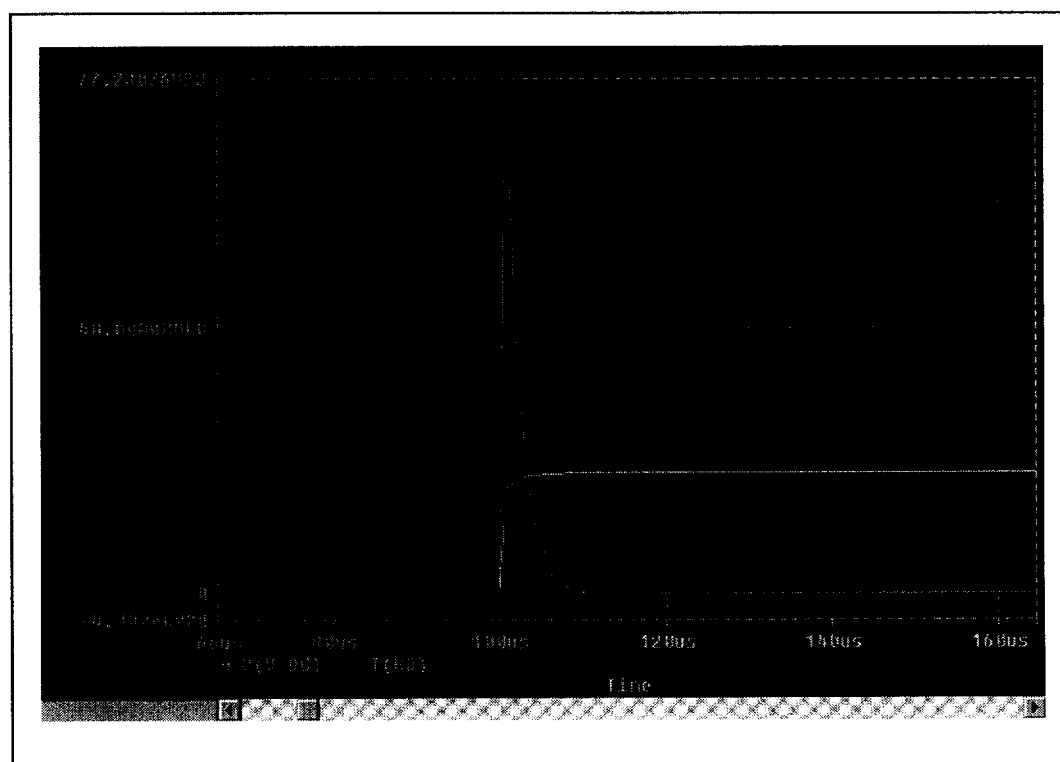
Figure 5. Instantaneous In-Rush Current Model



Figure 6. Instantaneous In-Rush Current

Due to the stringent component height requirements (≤ 4mm) of the Intel Pentium II Processor Mobile Module, tantalum capacitors must be used as input bulk capacitance in the voltage regulator circuit. Because of tantalum capacitor's susceptibility to high in-rush current, special care must be taken to soften the initial rush of current applied to these capacitors. One way to soften the in-rush current and provide over voltage/over current protection is to ramp up V_DC slowly using a circuit similar to the one shown in Figure 7.
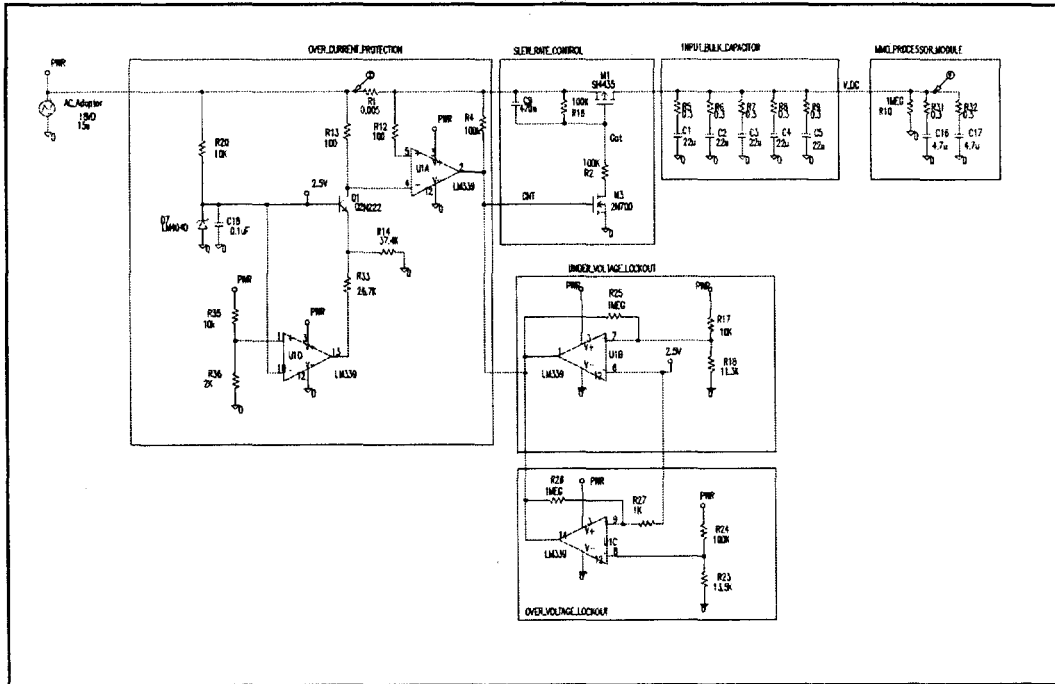


**Figure 7. Over Current Protection Circuit**

#### 4.6.4.1. Slew-Rate Control: Circuit Description

In Figure 8, PWR is the voltage generated by applying the AC Adaptor or Battery. M1 is a low RDS(on) P-Channel MOSFET such as a Siliconix SI4435DY. When the voltage on PWR is applied and increased to over 4.75V, the UNDER_VOLTAGE_LOCKOUT Circuit allows R4 to pull up the gate of M3 to start a turn-on sequence. M3 pulls its drain toward ground forcing current to flow through R2. M1 will not start to source any current until after t_delay with t_delay defined as:

$$t\_delay := -R2 \cdot C9 \cdot \ln\left(1 - \frac{Vt}{Vpwr - Vgs\_max}\right)$$

$$Vgs\_max = \frac{R16}{R16 \ R2} \cdot Vpwr$$

The manufacturer's Vgs_max specification of 20V must never be exceeded. However, Vgs_max must be high enough to keep the RDS (on) of the device as low as possible. After the initial t_delay, M1 will begin to source current and V_DC will start to ramp up. The ramp up time, t_ramp, is defined as:

$$t\_ramp := -R2 \cdot C9 \cdot \ln\left(1 - \frac{Vsat}{Vgs\_max}\right) - t\_delay$$

Maximum current during the voltage ramping is:

$$I = Ctotal \cdot \frac{Vpwr}{t\_ramp}$$

With the circuit shown in Figure 10, t_delay = 5.53 ms, t_tran = 14.0 ms and I_max = 146 mA.

Figure 8 shows a SPICE simulation of the circuit in Figure 10.

To increase the reliability of Tantalum capacitors, use a slew rate control circuit described in Figure 7 and voltage-derate the capacitor about 50 percent. That is, for a maximum input voltage of 18V, use a 35V capacitor with low ESR with high ripple current capability.

On the base board, place five 22µF/35V capacitors directly at the V_DC pins of the processor module connector. An acceptable capacitor for this application would be the component from AVX: TPSE226K035R0300.

One more issue that must be raised here is that the Slew Rate Control circuit should be applied to every input power source to the system V_DC to provide the most protection. If all power sources (i.e., battery or batteries, AC Adaptor, etc.) are OR'ed together at the PWR node, there is still a potential problem. For example, if a 3X3 Li-Ion battery pack is powering the system (12V at PWR), and the AC Adaptor (18V) is plugged into the system, it will immediately source current to the PWR node and V_DC rapidly. This is because the Slew Rate Control is already ON. Therefore, the slew rate control must be applied to every input power source to provide the most protection.

Also shown in Figure 10 are Under and Over Voltage and Over-current protection circuits that can be used to increase the protection level for the Intel Pentium II Processor Mobile Module.
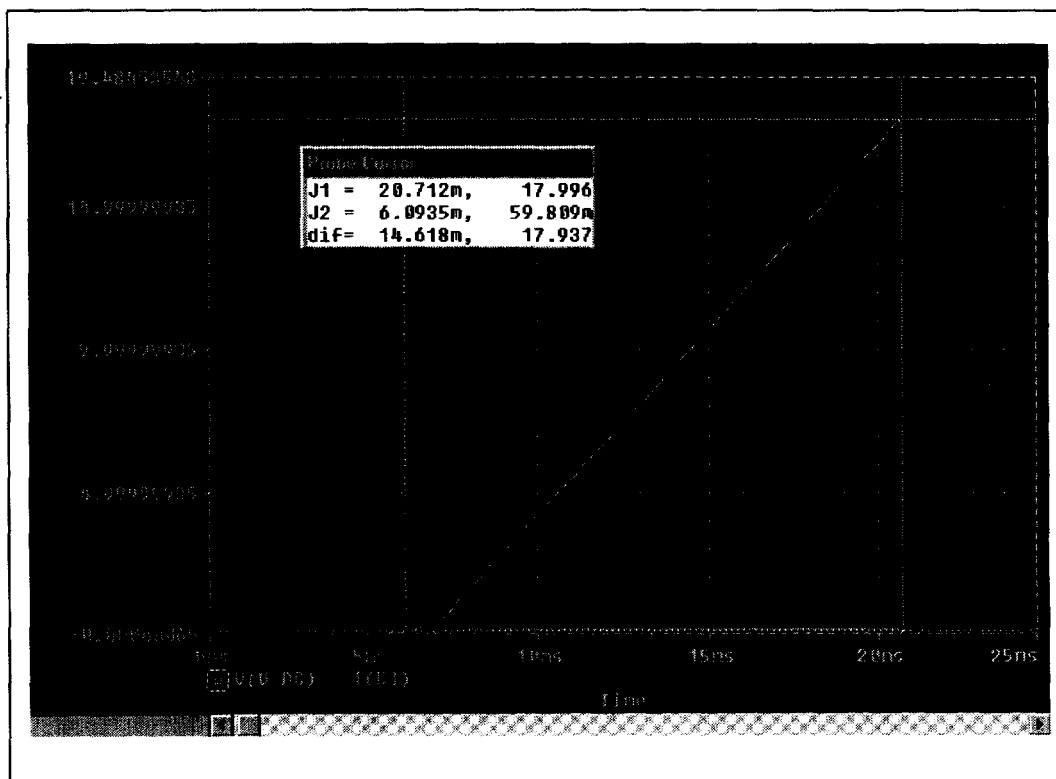
**Figure 8. Spice Simulation Using In Rush Protection**

**4.6.4.2. Under Voltage Lockout: Circuit Description**

The circuit shown in Figure 8 provides an under-voltage protection and locks out the applied voltage to the Intel Pentium II Processor Mobile Module to prevent an accidental turn-on at low voltage. The output of this circuit, pin 1 of the LM339 comparator, is an open-collector output. It is low when the applied voltage at PWR is less than 4.75V. This voltage can be calculated with the following equation with the voltage across D7 as 2.5V. (D7 is a 2.5-V reference generator.)

$$V\_uv\_lockout := Vref \left[ 1 + \frac{R17}{\left( \frac{R18 \cdot R25}{R18 + R25} \right)} \right]$$

$$V\_uv\_lockout = 4.757 \cdot volt$$

**4.6.4.3. Over Voltage Lockout: Circuit Description**

The Intel Pentium II Processor Mobile Module is specified to operate with a maximum input voltage of 21V. This circuit locks out the input voltage if it exceeds the maximum 21V. The output of this circuit, Pin 14 of the LM339 comparator, is an open-collector output. It is low when the applied voltage at PWR is more than 21V. This voltage can be calculated with the following equation:

$$V\_ov\_lockout := Vref \left(\frac{R26}{R26+R27}\right) \cdot \left(1 + \frac{R24}{R23}\right)$$

$$V\_ov\_lockout = 20.998 \, volt$$

#### 4.6.4.4. Over Current Protection: Circuit Description

Figure 8 shows that the circuit detects an over-current condition and cuts off the input voltage applied to the Intel Pentium II Processor Mobile Module. This circuit has two different current limit trip points. This takes into account the different maximum current drain by the Intel Mobile Module at different input voltages (i.e., whether the AC Adaptor is plugged in or not.) Assuming the AC Adaptor voltage is 18V and the battery is a 3x3 Li-Ion configuration with a minimum voltage of 7.5V, the maximum current for the above circuit can be calculated using the following expression:

With AC Adaptor:

$$I\_wAdaptor := \frac{Vref - Vbe\_Q1}{R14} \cdot \frac{R13}{R1}$$

$$I\_wAdaptor = 0.989 \bullet amp$$

$$I\_woAdaptor := \frac{Vref - Vbe\_Q1}{\left(\dfrac{R14R33}{R14+R33}\right)} \cdot \frac{R13}{R1}$$

$$I\_woAdaptor = 2.375 \bullet amp$$

### 4.7. Active Thermal Feedback

Table 22 identifies the address allocated for the System Management Bus (SMBus) thermal sensor used on the Intel Mobile Module.

**Table 22. Thermal Sensor SMBUS Address Table**

| Function | Fixed Address AD Bits (6:4) | Selectable Address AD Bits (3:0) |
|---|---|---|
| Thermal Sensor | 100 | 1110 |
| Reserved | 010 | 1010 |
| Reserved | 010 | 1011 |

NOTE:

The thermal sensor used is compliant with SMBus addressing. However, the register set and architecture on the Intel Pentium® II Processor Mobile Module are different from the thermal sensor used in previous generations of Intel Mobile Modules. After consulting your local Intel sales representative, refer to the data sheet of the digital thermal sensor for complete device programming details.

## 4.8. Power Management

### 4.8.1. The Mobile Pentium® II Processor Clock Control Architecture

The Mobile Pentium II processor clock control architecture (Figure 9) has been optimized for leading edge deep green desktop and mobile computer designs. The Auto Halt state provides a low power clock state that can be controlled through the software execution of the HLT instruction. The Quick Start state provides a very low power, low exit latency clock state that can be used for hardware controlled "idle" computer states. The Deep Sleep state provides an extremely low power state that can be used for "Power-on Suspend" computer states, which is an alternative to shutting off the processor's power. Compared to the Pentium processor exit latency of 1 msec, the exit latency of the Deep Sleep state has been reduced to 30 μsec in the Mobile Pentium II processor. The Stop Grant and Sleep states shown in Figure 9 are intended for use in

"Deep Green" desktop and server systems—not in mobile systems. Performing state transitions not shown in Figure 9 is neither recommended nor supported.

The clock control architecture consists of seven different clock states: Normal, Stop Grant, Auto Halt, Quick Start, HALT/Grant Snoop, Sleep and Deep Sleep states. The Stop Grant and Quick Start clock states are mutually exclusive, i.e., a strapping option on pin A15# chooses which state is entered when the STPCLK# signal is asserted. The Quick Start state is enabled by strapping the A15# pin to ground at Reset; otherwise, asserting the STPCLK# signal puts the processor into the Stop Grant state. The Stop Grant state has a higher power level than the Quick Start state and is designed for SMP platforms. The Quick Start state has a much lower power level, but it can only be used in uniprocessor platforms. Table 24 provides clock state characteristics (power numbers based on estimates for a Mobile Pentium II processor running at 266 MHz), which are described in detail in the following sections.

**Table 23. New Pins in the Mobile Pentium® II Processor**

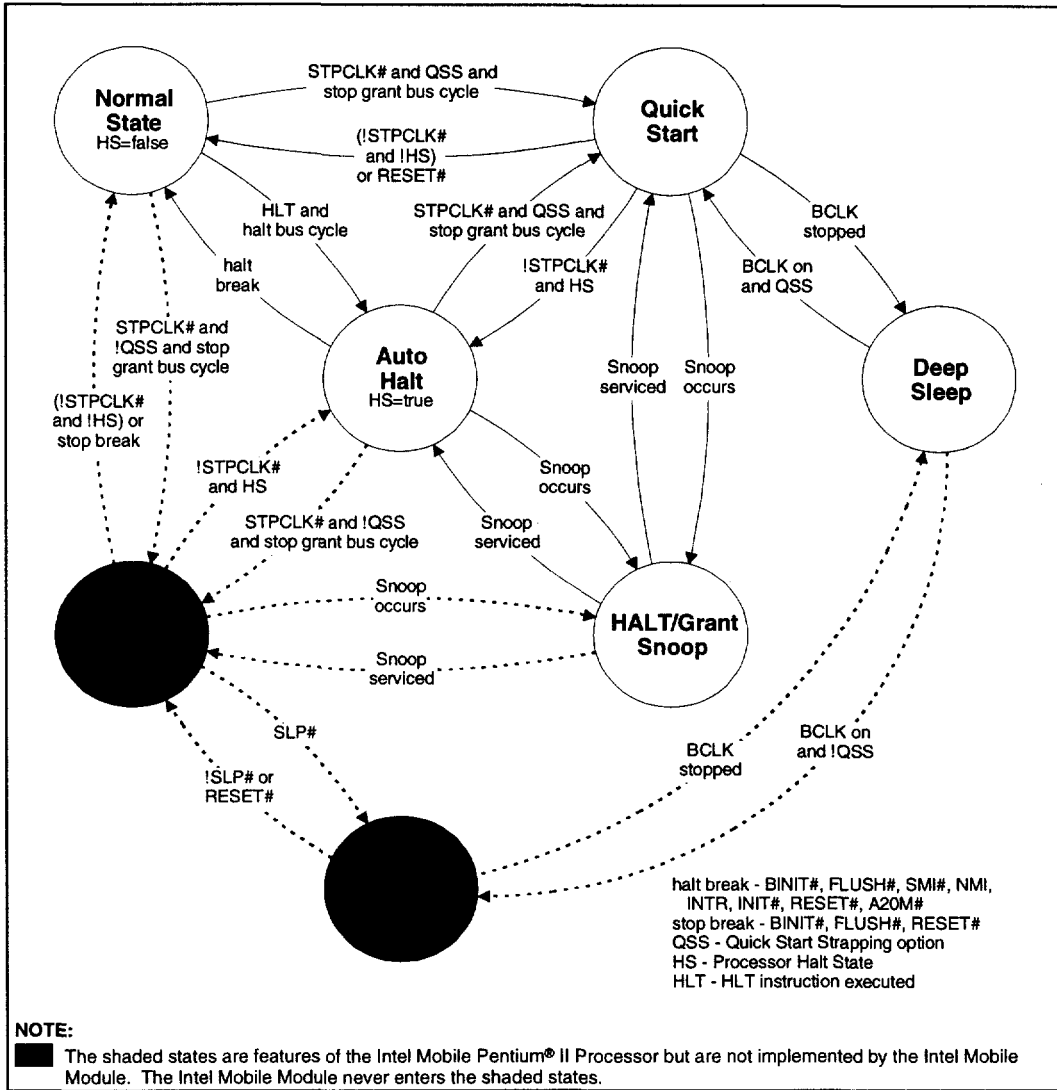| Pin Name | Type | Description |
|----------|------|-------------|
| SMBALERT# | O | Thermal sensor attention signal. |
| SMBCLK | I/O | SMBus clock signal. Refer to the *System Management Bus Specification* for descriptions and specifications of the three SMBus signals. |
| SMBDATA | I/O | SMBus data signal. Refer to the *System Management Bus Specification* for descriptions and specifications of the three SMBus signals. |

**Figure 9. Mobile Pentium® II Processor Clock Control States**

**Table 24. Mobile Pentium® II Processor Clock State Characteristics**

| Clock State | Exit Latency | Power | Snooping? | System Uses |
|---|---|---|---|---|
| Normal | N/A | Varies | Yes | Normal program execution |
| Auto Halt | Approximately 10 bus clocks | 1.2 W | Yes | S/W controlled entry idle mode |
| Stop Grant | 10 bus clocks | 1.2 W | Yes | H/W controlled entry/exit mobile throttling |
| Quick Start | Through snoop, to *HALT/Grant Snoop* state: immediate<br><br>Through STPCLK#, to *Normal* state: 10 bus clocks | 0.5 W | Yes | H/W controlled entry/exit mobile throttling |
| HALT/ Grant Snoop | A few bus clocks after the end of snoop activity. | Not specified | Yes | Supports snooping in the low power states |
| Sleep | To *Stop Grant* state 10 bus clocks | 0.5 W | No | H/W controlled entry/exit desktop idle mode support |
| Deep Sleep | 30 μsec | 100 mW | No | H/W controlled entry/exit mobile powered-on suspend support |

### 4.8.2. NORMAL STATE

The Normal state of the processor is the normal operating mode where the processor's internal clock is running and the processor is actively executing instructions.

### 4.8.3. AUTO HALT STATE

This is a low power mode entered by the processor through the execution of the HLT instruction. The power level of this mode is similar to the Stop Grant state. A transition to the Normal state is made by a halt break event (one of the following signals going active: NMI, INTR, BINIT#, INIT#, RESET#, FLUSH# or SMI#).

Asserting the STPCLK# signal while in the Auto Halt state will cause the processor to transition to the Stop Grant or Quick Start state, where a Stop Grant Acknowledge bus cycle will be issued. By deasserting STPCLK#, system logic can return the processor to the Auto Halt state without issuing a new Halt bus cycle.

The SMI# interrupt is recognized in the Auto Halt state. The return from the System Management Interrupt (SMI) handler can be to either the Normal state or the Auto Halt state. See the *Intel Architecture Software Developer's Manual, Volume III: System Programmer's Guide*, for more information. No Halt bus cycle is issued when returning to the Auto Halt state from SMM.

The FLUSH# signal is serviced in the Auto Halt state. After the on-chip and off-chip caches have been flushed, the processor will return to the Auto Halt state without issuing a Halt bus cycle. Transitions in the A20M# pin are recognized while in the Auto Halt state.

### 4.8.4. STOP GRANT STATE

The processor enters this mode with the assertion of the STPCLK# signal when it is configured for Stop Grant state (via the A15# strapping option). The processor is still able to respond to snoop requests and latch interrupts. Latched interrupts will be serviced when the processor returns to the Normal state. Only one occurrence of each interrupt event will be latched. A transition back to the Normal state can be made by the de-assertion of the STPCLK#

signal, or the occurrence of a stop break event (a BINIT#, FLUSH# or RESET# assertion).

While in the Stop Grant state, SMI#, INIT# and LINT[1:0] will be latched by the processor, and only serviced when the processor returns to the normal state. Only one occurrence of each event will be recognized upon return to the normal state.

The processor will return to the Stop Grant state after the completion of a BINIT# bus initialization unless STPCLK# has been de-asserted.

RESET# assertion will cause the processor to immediately initialize itself, but the processor will stay in the Stop Grant state after initialization until STPCLK# is deasserted.

If the FLUSH# signal is asserted, the processor will flush the on-chip and off-chip caches and return to the Stop Grant state. A transition to the Sleep state can be made by the assertion of the SLP# signal.

### 4.8.4.1.    Quick Start State

This is a mode entered by the processor with the assertion of the STPCLK# signal when it is configured for the Quick Start state (via the A15# strapping option). In the Quick Start state the processor is only capable of acting on snoop transactions generated by the system bus priority device. Because of its snooping behavior, Quick Start can only be used in a Uniprocessor (UP) configuration.

A transition to the Deep Sleep state can be made by stopping the clock input to the processor. A transition back to the Normal state (from the Quick Start state) is made only if the STPCLK# signal is deasserted.

While in this state the processor is limited in its ability to respond to input. It is incapable of latching any interrupt, servicing snoop transactions from symmetric bus masters or responding to FLUSH# or BINIT# assertions. While the processor is in the Quick Start state, it will not respond properly to any input signal other than STPCLK#, RESET# or BPRI#. If any other input signal changes, then the behavior of the processor will be unpredictable. No serial interrupt messages may begin or be in progress while the processor is in the Quick Start state. The thermal sensor will respond normally to SMBus transactions when the processor is in the Quick Start state.

RESET# assertion will cause the processor to immediately initialize itself, but the processor will stay in the Quick Start state after initialization until STPCLK# is deasserted.

Asserting the SLP# signal when the processor is configured for Quick Start will result in unpredictable behavior and is not recommended.

### 4.8.5.    HALT/GRANT SNOOP STATE

The Mobile Pentium II processor will respond to snoop transactions on the system bus while in the Auto Halt, Stop Grant or Quick Start state. When a snoop transaction is presented on the system bus the processor will enter the HALT/Grant Snoop state. The processor will remain in this state until the snoop on the system bus has been serviced and the system bus is quiet. After the snoop has been serviced, the processor will return to the previous Auto Halt, Stop Grant or Quick Start state. If the HALT/Grant Snoop state is entered from the Quick Start state, then the input signal restrictions of the Quick Start state still apply in the HALT/Grant Snoop state, except for those signal transitions that are required to perform the snoop.

### 4.8.6.    SLEEP STATE

The Sleep state is a very low power state in which the processor maintains its context and the phase-locked loop (PLL) maintains phase lock. The Sleep state can only be entered from the Stop Grant state. After entering the Stop Grant state, the SLP# signal can be asserted, causing the processor to enter the Sleep state. The SLP# pin is not recognized in the Normal or Auto Halt states.

The processor can be reset by the RESET# pin while in the Sleep state. If RESET# is driven active while the processor is in the Sleep state then SLP# and STPCLK# must immediately be driven inactive to ensure that the processor correctly executes the Reset sequence.

Input signals (other than RESET#) may not change while the processor is in the Sleep state or transitioning into or out of the Sleep state. Input signal changes at these times will cause unpredictable behavior. Thus, the processor is incapable of snooping or latching any events in the Sleep state. The thermal sensor will respond normally to SMBus transactions when the processor is in the Sleep state.

While in the Sleep state, the processor is capable of entering its lowest power state, the Deep Sleep state, by removing the processor's input clock. PICCLK may be removed in the Sleep state.

### 4.8.7.    DEEP SLEEP STATE

The Deep Sleep state is the lowest power mode the processor can enter while maintaining its context. The Deep Sleep state is entered by stopping the BCLK input to the processor, while it is in the Sleep or Quick Start state. For proper operation, the BCLK input should be stopped in the low state.

To re-enter either the Sleep or Quick Start state from the Deep Sleep state, the BCLK input must be restarted. The processor will return to the Sleep or Quick Start state, as appropriate, after 30 msec. PICCLK may be removed in the Deep Sleep state. PICCLK should be designed to turn on when BCLK turns on when transitioning out of the Deep Sleep state.

The input signal restrictions for the Deep Sleep state are the same as for the Sleep state, except that RESET# assertion will result in unpredictable behavior. The thermal sensor will respond normally to SMBus transactions when the processor is in the Deep Sleep state.

### 4.8.8.    CURRENTLY SUPPORTED CLOCK STATES

Table 25 shows the low-power clock states supported by the Pentium II processor family product line.

### 4.8.9.    OPERATING SYSTEM IMPLICATIONS OF THE QUICK START AND SLEEP STATES

There are a number of architectural features of the Mobile Pentium II processor that are not available when the Quick Start state is enabled or do not function in the Quick Start or Sleep state as they do in the Stop Grant state. These features are part of the APIC, time-stamp counter and performance monitor counters.

The local APIC timer does not behave properly when the processor is in the Quick Start or Sleep state. There is no guarantee that the local APIC timer will count down in the Quick Start or Sleep state. If the timer counts down to zero when the processor is in or about to enter the Quick Start or Sleep state, the processor's behavior will be unpredictable. Inter-Processor Interrupts (IPIs) should not be used in Mobile Pentium II processor systems. If software generates an IPI just before the processor enters the Quick Start or Sleep state, then a message on the APIC bus will be generated. This would violate the requirement that no input signals toggle in the Quick Start or Sleep state. Any software-generated IPI in a Mobile Pentium II processor system (uniprocessor system) will always result in an error.

**Table 25. Low-Power Clock States Supported by Processor**

| Processor | Clock State | | | | |
|---|---|---|---|---|---|
|  | Stop Grant | Auto Halt | Quick Start | Sleep | Deep Sleep |
| Pentium® Pro Processor | X | X | | | |
| Pentium II Processor | X | X | | X | X |
| Mobile Pentium II Processor | X | X | X | X | X |
| Pentium II Processor Mobile Module | | X | X | | X |

The time-stamp counter and the performance monitor counters are not guaranteed to count in the Quick Start or Sleep states. If software sets the APIC interrupt enable bit of either of the performance counters, then the resulting behavior will be unpredictable.

## 4.9. Typical POS/STR Power

The Intel Pentium II Processor Mobile Module (MMC-2) supports both power on suspend (POS) and suspend to RAM (STR) features. Typical power during these states are:

| States | MMC2 Power |
|--------|------------|
| POS | 910mW |
| STR | 3mW |

These are average values of measurement on several typical modules and are guidelines only.

## 5.0.    MECHANICAL REQUIREMENTS

## 5.1.    Module Dimensions

This section provides the physical dimensions for the Intel Mobile Module.

### 5.1.1.    BOARD AREA

Figure 10 shows the board dimensions and the connector orientation for the Intel Mobile Module. These dimensions are necessary to accommodate the next generation of Intel Mobile Processors and PCI Northbridge chipset controllers.
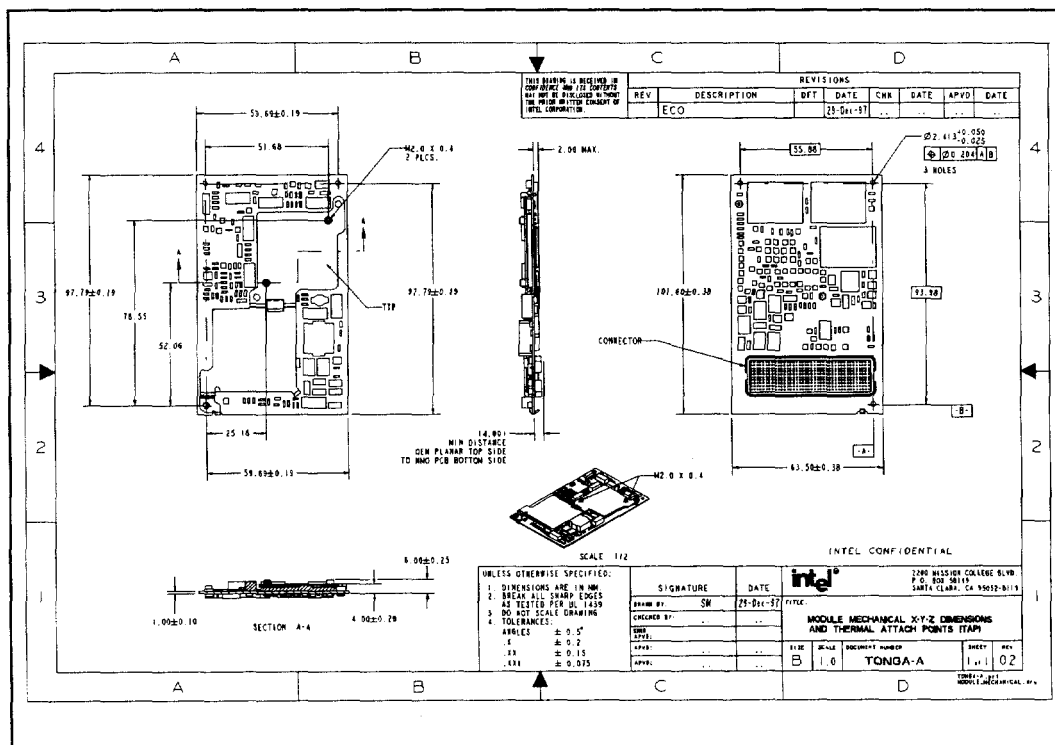


**Figure 10. Intel Mobile Module Board Dimensions with 400-Pin Connector Orientation**

**intel®**

### 5.1.2. MMC-2 PIN 1 LOCATION

Figure 11 shows the location of pin 1 of the 400pin MMC-2 connector as referenced to the adjacent mounting hole.



MODULE
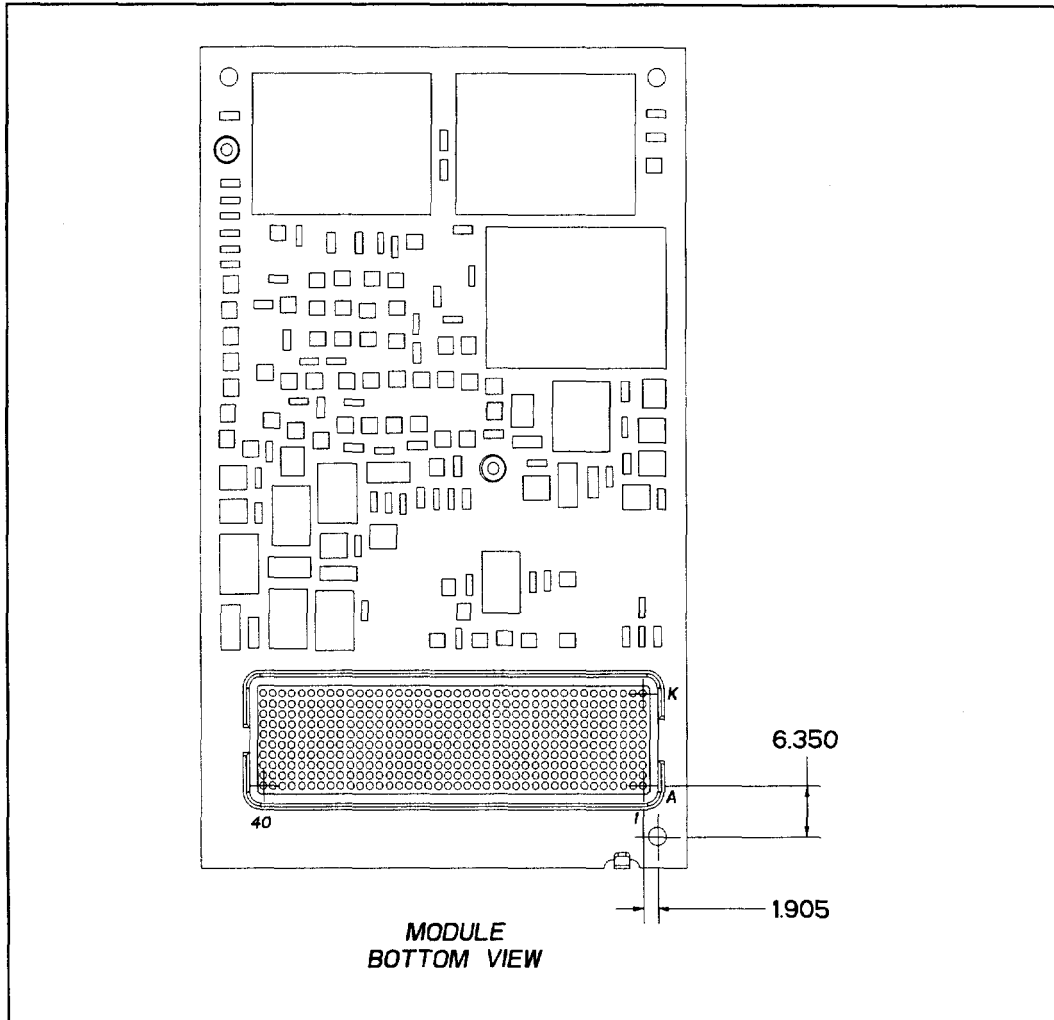BOTTOM VIEW

**Figure 11. Intel Mobile Module Board Dimensions with 400-Pin Connector—Pin 1 Orientation**

min: 0.90mm
max: 1.10mm
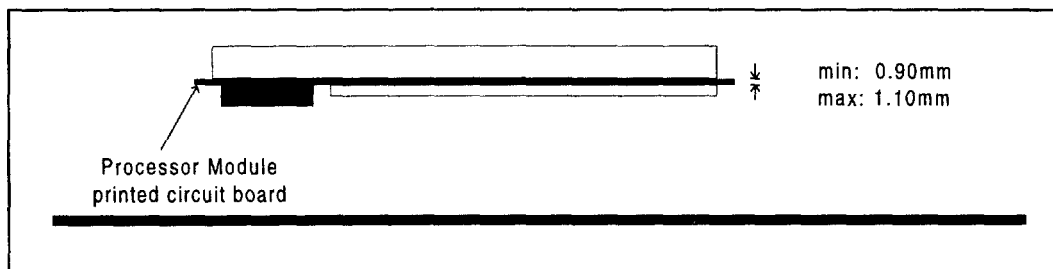
Processor Module
printed circuit board

**Figure 12. PCB Board Thickness**

### 5.1.3. PRINTED CIRCUIT BOARD THICKNESS

Figure 12 shows the Intel Mobile Module profile and the associated minimum and maximum thickness of the printed circuit board (PCB). The range of PCB thickness allows for different PCB technologies to be used with current and future modules.

**NOTE**

*The system manufacturer must ensure that the mechanical restraining method and/or system-level EMI contacts are able to support this range of PCB thickness, to ensure compatibility with future modules.*

### 5.1.4. HEIGHT RESTRICTIONS

Figure 13 shows the Intel Mobile Module mechanical stackup and associated component clearance requirements.

The system manufacturer establishes the board-to-board clearance between the Intel Mobile Module and the system electronics by selecting one of three possible mating connectors.

The mating connectors provide board-to-board clearances (distance underneath the Intel Mobile Module) of 4 mm, 6 mm or 8 mm. With these three options, the system manufacturer has reasonable flexibility in choosing components on the system electronics that are between the two boards. Information on these connectors can be obtained from your local Intel representative.
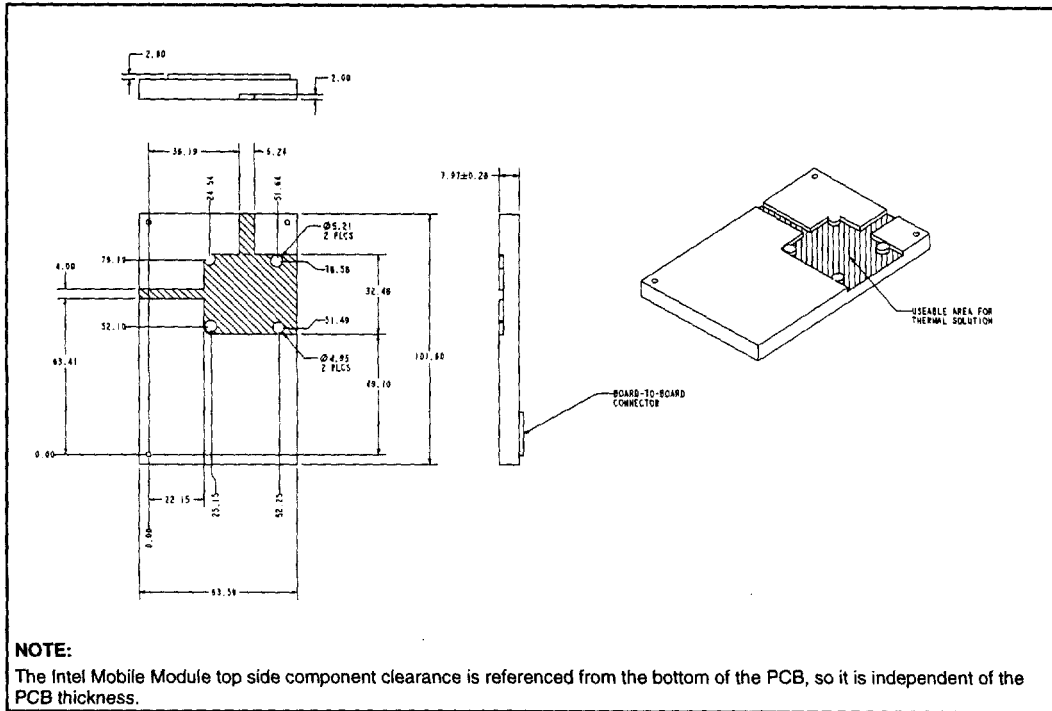
**NOTE:**
The Intel Mobile Module top side component clearance is referenced from the bottom of the PCB, so it is independent of the PCB thickness.

**Figure 13. Intel Mobile Module 3-D Mechanical Drawing**

## 5.2. Thermal Transfer Plate

The Intel Mobile Module provides a thermal transfer plate, or TTP, connected to the processor in a standard position called the thermal attach point (see Figure 14 and Figure 15 for exact dimensions). The thermal attach point is a fixed location relative to the mounting holes and other physical datum on the Intel Mobile Module. The system manufacturer can use both a heat pipe and a heat spreader plate in contact with the thermal attach point to transfer heat through the notebook system or a thermal solution of their choice. The TTP thermal resistance as measured between the processor core to the OEM interface (top of the TTP) is less than 1°C per Watt.

The thermal transfer plate is physically mounted to the Intel Mobile Module, and may be different from one generation of Intel Mobile Module to the next. The following figures detail the mechanical dimensions of the thermal transfer plate used on the Pentium II Processor Mobile Module, and the conceptual relationship between the circuit board thermal transfer plate, and thermal attach point.
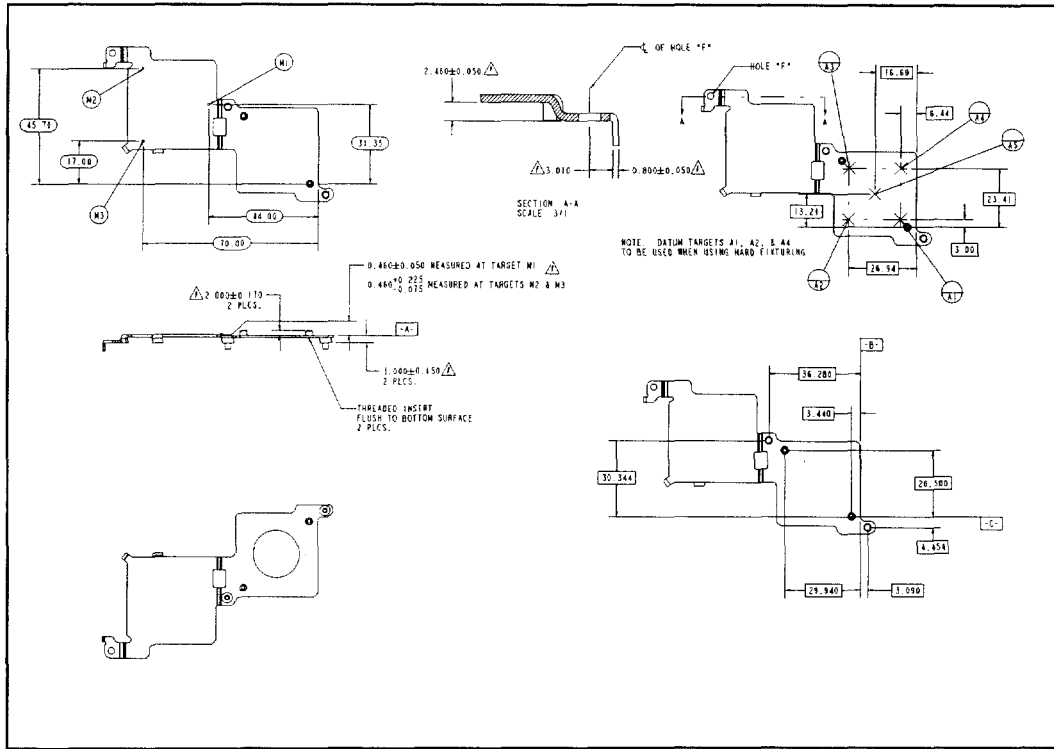
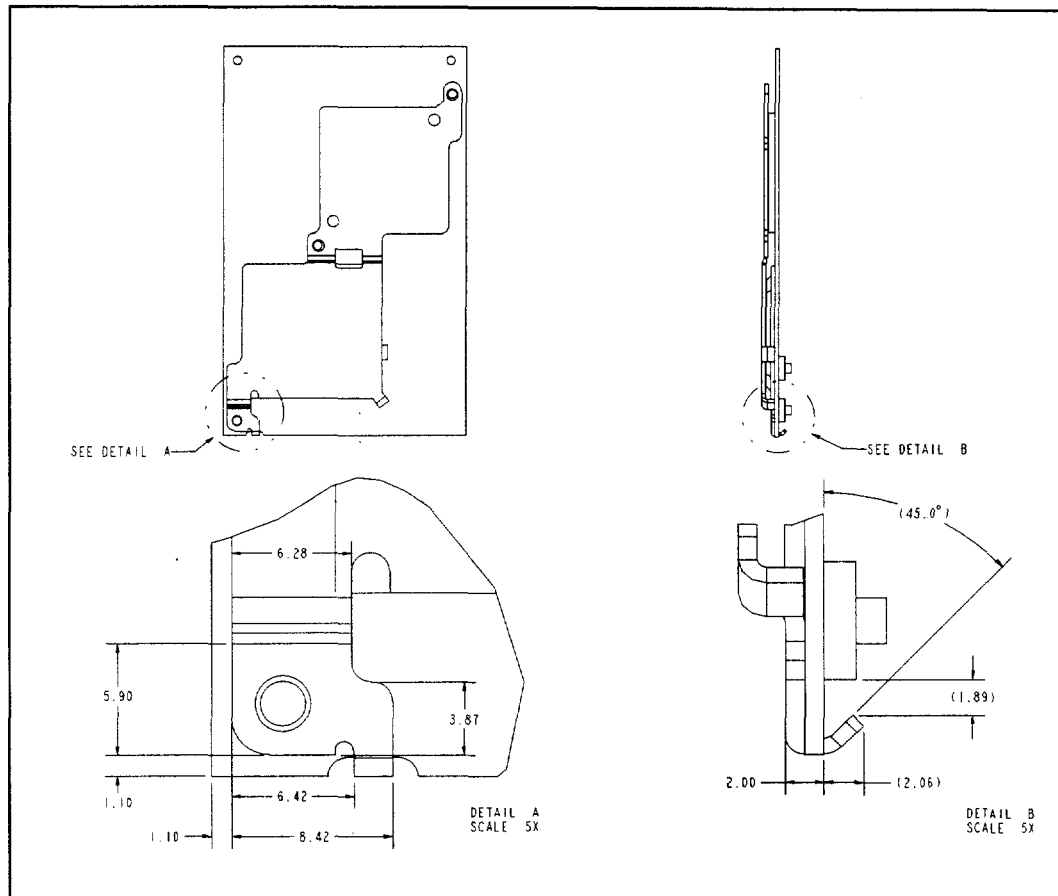**Figure 14. Intel Mobile Module Thermal Transfer Plate**

**Figure 15. Intel Mobile Module Thermal Transfer Plate**

## 5.3. Module Physical Support

Figure 16 shows the Intel Mobile Module standoff support hole patterns and the board edge clearance around the perimeter of the Mobile Module. These hole locations and board edge clearances will remain fixed for all Intel Mobile Modules. The hole patterns and board edge clearance lets the system manufacturer develop several methods for mechanically supporting the Intel Mobile Module within a particular notebook system.

### 5.3.1. MODULE MOUNTING REQUIREMENTS

Three mounting holes are available to the System OEM for securing the module to the system base or the system electronics. See Figure 10 for mounting hole locations. It is strongly recommended that the System OEM utilize mounting screws through all three of the mounting holes to ensure long term reliability of the mechanical and EMI integrity of the system.

To interface to the module's thermal transfer plate (TTP), it is recommended that the exact dimensions shown in Figure 14 for the OEM thermal interface block be used. These dimensions provide maximum contact area to the TTP while ensuring that no warpage of the TTP occurs. If warpage occurs due to the use of an improperly-designed interface, or over-tightening of assembly screws, the thermal resistance of the module could be adversely affected.

When attaching the mating block to the module TTP, material such as a thermal elastimer or thermal grease should be used. This material is designed to reduce the thermal resistance and should be placed between the TTP and the OEM mating block. This will improve the overall system thermal efficiency.

After the OEM has placed the mating thermal transfer plate, it should be secured with 2.0mm screws using a maximum torque of 1.5 - 2.0 Kg*cm (equivalent to 0.147 - .197 N*m). The thread length of the 2.00mm screws should be 2.25mm gageable thread (2.25 mm minimum to 2.80mm maximum).

The board edge clearance includes a 0.762 mm (0.030 in) width EMI containment ring around the perimeter of the module. This ring is on each layer of the module PCB and is grounded. On the surface of the module, the metal is exposed for EMI shielding purposes. The hole patterns placed on the module also have a plated surrounding ring and one can use a metal standoff to contact the ring for EMI shielding purposes. Figure 16 shows the dimensions of the EMI containment ring and the keepout area. No components are placed on the board in the keepout area.



**Standoff Holes and Board Edge Keepouts (top side)**

Hole detail, 3 places

3.81+/-0.19mm

USEABLE MOUNTING AREA SHOWN HERE
4.45mm diameter grounded ring available for mounting

2.413mm +0.050mm -0.025mm hole diameter

1.27+/-0.19mm board edge to EMI ring

0.762mm width of EMI containment ring

2.54+/-0.19mm keepout area
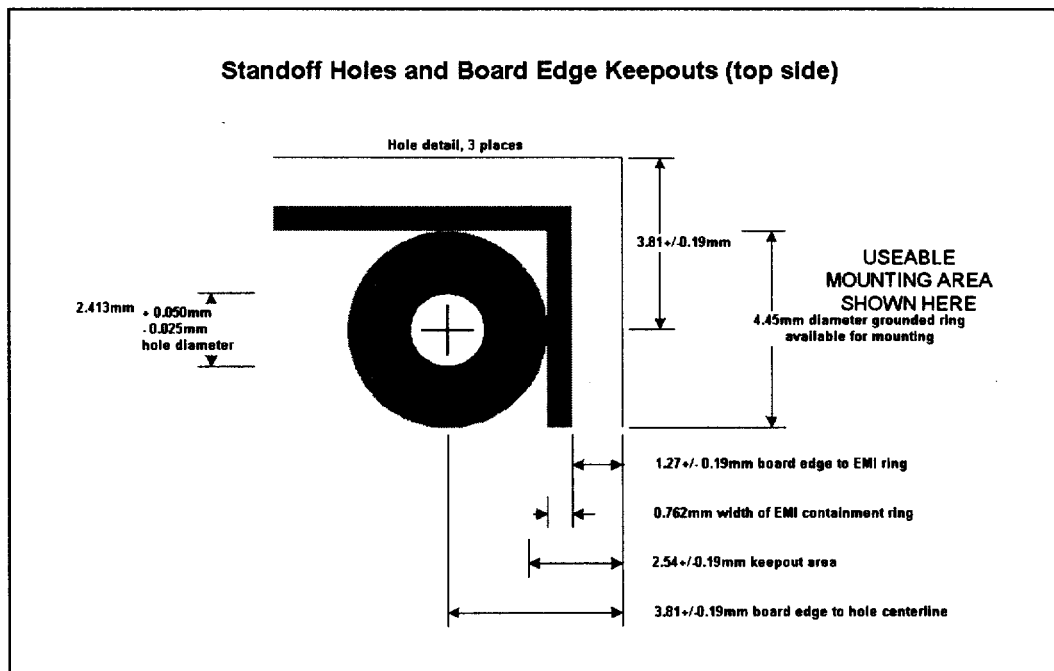
3.81+/-0.19mm board edge to hole centerline

**Figure 16. Standoff Holes, Board Edge Clearance and EMI Containment Ring**

Standoffs should be used to provide support for the installed module. The distance from the bottom of the module PCB to the top of the OEM system electronics board with the connectors mated is 4.0mm +0.16mm / -0.13mm, however the warpage of the baseboard can vary and should be calculated into the final dimensions of the standoffs used.

**5.3.1.1.** **Module Weight**

The weight of the Pentium II Processor Mobile Module is 48g +/- 2g.

## 6.0. THERMAL SPECIFICATIONS

**Table 26. Pentium® II Processor Mobile Module (MMC-2) Power Specifications**

| Symbol | Parameter | | Typ | Max[1] | Unit | Notes |
|---|---|---|---|---|---|---|
| $TDP^2_{MMC-2}$ | Thermal Design Power (MMC-2 module) | @ 300 MHz<br>@ 266 Mhz<br>@ 233 MHz | — | 13.9 | W | Module (core, northbridge, voltage regulator, & L2 cache) |

**NOTES:**

1. $TDP_{MAX}$ is a specification of the total power dissipation of the worst-case processor, worst-case Northbridge, worst-case L2 cache, and worst-case voltage regulator while executing a worst-case instruction mix under normal operating conditions at nominal voltages. Not 100% tested. Specified by design/characterization.

2. Please refer to the yellow cover document, *Mobile Pentium® II Processor and Pentium® II Processor Mobile Module Power Consumption,* rev 1.0, for detailed discription of thermal specification terms.

## 7.0. LABELING INFORMATION

The Pentium II Processor Mobile Module has two means of being tracked. The first means is by labeling information via the Product Tracking Code (PTC) and the other is by an OEM generated software utility.

## 7.1. Product Tracking Code

The Product Tracking Code label provides module information that is used by Intel to determine the assembly level of the module. The PTC label exists on the secondary side of the module and provides the following information:
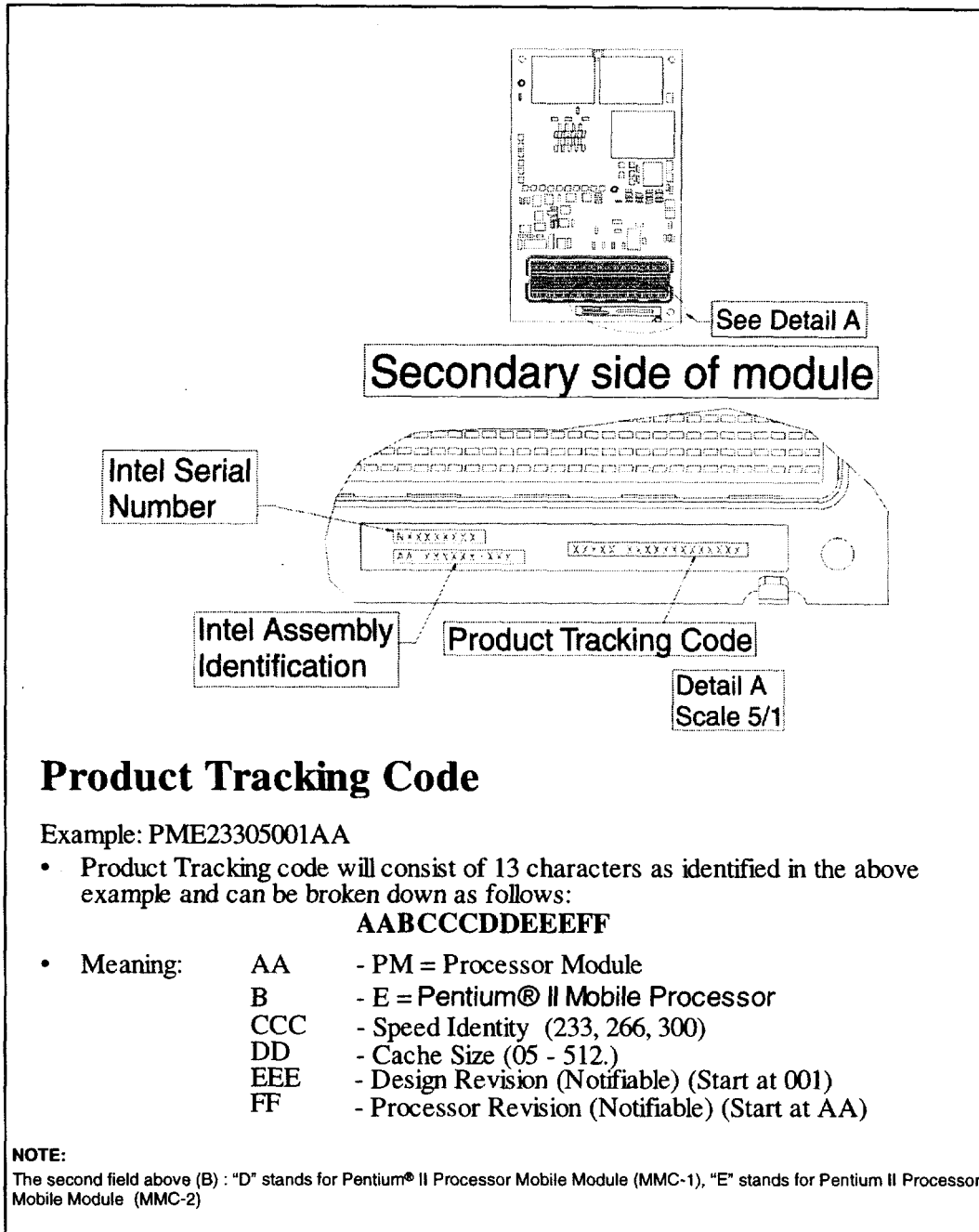
See Detail A

## Secondary side of module

Intel Serial Number

Intel Assembly Identification

Product Tracking Code

Detail A
Scale 5/1

## Product Tracking Code

Example: PME23305001AA

- Product Tracking code will consist of 13 characters as identified in the above example and can be broken down as follows:

**AABCCCDDEEEFF**

- Meaning:

| | | |
|---|---|---|
| AA | - PM = Processor Module | |
| B | - E = Pentium® II Mobile Processor | |
| CCC | - Speed Identity (233, 266, 300) | |
| DD | - Cache Size (05 - 512.) | |
| EEE | - Design Revision (Notifiable) (Start at 001) | |
| FF | - Processor Revision (Notifiable) (Start at AA) | |

**NOTE:**

The second field above (B) : "D" stands for Pentium® II Processor Mobile Module (MMC-1), "E" stands for Pentium II Processor Mobile Module (MMC-2)

**Figure 17. Intel Mobile Module Product Tracking Information**

### 7.1.1.  MODULE IDENTIFICATION BITS

Located on the Pentium II Processor Mobile Module are four strapping resistors used to determine the production level of the module. If connected and terminated properly, up to 16 unique module revision levels can be determined. Using a software utility generated by the OEM, these ID bits can be read along with the CPU and north bridge stepping IDs to provide a complete module manufacturing revision level. For current PTC and module ID bit information, please refer to the latest Pentium II Processor Mobile Module Product Change Notification letter which can be obtained from your local Intel sales representative.

## 8.0.  ENVIRONMENTAL STANDARDS

The environmental standards the Intel Pentium II Processor Mobile Module are defined in Table 27.

**Table 27. Environmental Standards**

| Parameter | Condition | Specification |
|-----------|-----------|---------------|
| Temperature | Non-Operating | -40°C to 85°C |
| Cycle | Operating | 0°C to 55°C |
| Humidity | Unbiased | 85% relative humidity @ 55 °C |
| Voltage | V_5 | +/- 4% |
|  | V_3S | +/- 4% |
|  | V_3 | +/- 4% |
| Shock | Non-Operating | Half Sine, 2G, 11msec |
|  | Unpackaged | Trapezoidal, 50G, 11msec |
|  | Packaged | Inclined Impact @5.7ft/s |
|  | Packaged | Half Sine, 2msec @36" Simulated Free Fall |
| Vibration | Unpackaged | 5Hz to 500Hz 2.2gRMS random |
|  | Packaged | 10Hz to 500Hz 1.0gRMS |
|  | Packaged | 11,800 impacts 2Hz to 5Hz (low frequency) |
| ESD | Human Body Model | 0 to 2kV (no detectable err) |