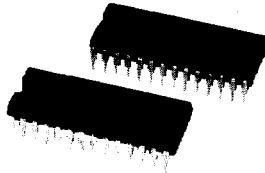


For Immediate Assistance, Contact Your Local Salesperson



PCM1760P/U
DF1760P/U

DEMO BOARD
AVAILABLE
See Appendix A

www.burr-brown.com/databook/PCM1760.html

Multi-Bit Enhanced Noise Shaping 20-Bit ANALOG-TO-DIGITAL CONVERSION SYSTEM

FEATURES

- **DUAL 20-BIT MONOLITHIC MODULATOR (PCM1760) AND MONOLITHIC DECIMATING DIGITAL FILTER (DF1760)**
- **HIGH PERFORMANCE:**
 - THD+N: -92dB typ, -90dB max
 - Dynamic Range: 108dB typ
 - SNR: 108dB min, 110dB typ
 - Channel Separation: 98dB typ, 94dB min
- **64X OVERSAMPLING**
- **CO-PHASE CONVERSION**
- **RUNS ON 256fs OR 384fs SYSTEM CLOCK**
- **VERSATILE INTERFACE CAPABILITY:**
 - 16-, 20-Bit Output
 - MSB First or LSB First Format
- **OPTIONAL FUNCTIONS:**
 - Offset Error Calibration
 - Overflow Detection
 - Power Down Mode (DF1760)
- **RUNS ON ±5V SUPPLIES (PCM1760) AND 5V SUPPLY (DF1760)**
- **COMPACT 28-PIN PACKAGES:**
 - 28-Pin DIP and SOIC

DESCRIPTION

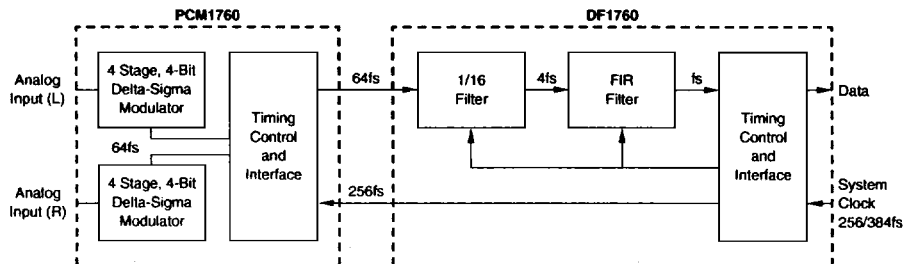
The PCM1760 and DF1760 combine for a low-cost, high-performance dual 20-bit, 48kHz sampling analog-to-digital conversion system which is specifically designed for dynamic applications.

The PCM1760/DF1760 pair form a 4-bit, 4th order, 64X oversampling analog-to-digital converter.

The PCM1760 is a delta-sigma modulator that uses a 4-bit quantizer within the modulation loop to achieve very high dynamic range.

The DF1760 is a high-performance decimating digital filter. The DF1760 accepts 4-bit 64fs data from the PCM1760 and decimates to 20-bit 1fs data.

The FIR filter of the DF1760 has pass-band ripple of less than ± 0.001 dB and greater than 100dB of the reject band attenuation.



International Airport Industrial Park • Mailing Address: PO Box 11400, Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd., Tucson, AZ 85706 • Tel: (520) 746-1111 • Twx: 910-852-1111
Internet: <http://www.burr-brown.com/> • FAXLine: (800) 548-6133 (US/Canada Only) • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 599-1510 • Immediate Product Info: (800) 548-6132

Or, Call Customer Service at 1-800-548-6132 (USA Only)

SPECIFICATIONS

ELECTRICAL

At $T_A = +25^\circ\text{C}$, $\pm V_{CC} = \pm 5\text{V}$, $+V_{DD} = +5\text{V}$, $f_s = 48\text{kHz}$ and ext. components = $\pm 2\%$, unless otherwise noted.

PARAMETER	CONDITIONS	PCM1760/DF1760			UNITS
		MIN	TYP	MAX	
RESOLUTION		20			Bits
ANALOG INPUT					
Input Range	$R_{IN1} = 2.2\text{k}\Omega$		± 2.5		Vp-p
Input Impedance	$R_{IN1} = 2.2\text{k}\Omega$		R_{IN1}		Ω
SAMPLING FREQUENCY					
Cover Range of fs	Integrator Constants: Application ⁽¹⁾	30	48	50	kHz
ACCURACY					
Gain Error	$V_{IN} = 0$ at 20s After Power-On 0°C to $+70^\circ\text{C}$		± 0.5	± 1.0	dB
Gain Mismatch				± 0.5	dB
Bipolar Zero Error				± 0.4	% FSR ⁽²⁾
Gain Drift		0°C to $+70^\circ\text{C}$		± 100	ppm/°C
Bipolar Zero Drift		0°C to $+70^\circ\text{C}$		± 20	ppm/°C
DYNAMIC CHARACTERISTICS⁽⁴⁾					
THD+N/(0dBFS)	P, U P-L, U-L	$f_{IN} = 1\text{kHz}$	-92 -90	-90 -88	dB
THD+N/(-20dBFS)	P, U P-L, U-L	$f_{IN} = 1\text{kHz}$	-76 -76	-70 -70	dB
THD+N/(-60dBFS)	P, U P-L, U-L	$f_{IN} = 1\text{kHz}$	-44 -44	-42 -42	dB
Dynamic Range	P, U P-L, U-L	$f_{IN} = 1\text{kHz}$, $V_{IN} = -60\text{dBFS}$, A Filter	104 104	108 108	dB
SNR	P, U P-L, U-L	$V_{IN} = 0$, A Filter	108 106	110 110	dB
Frequency Response		$f_{IN} = 20\text{kHz}$		± 0.1	dB
Channel Separation		$f_{IN} = 1\text{kHz}$, A Filter	94	98	dB
DIGITAL FILTER					
Over Sample Rate				64	fs
Ripple in Band		0 - 0.04535fs			dB
Stopband Attenuation -1		0.5465fs - 63.4535fs	-94		dB
Stopband Attenuation -2		0.5465fs - 3.4535fs	-100		dB
LOGIC INPUTS AND OUTPUTS					
Logic Family Input			TTL Level Compatible CMOS		
Frequency (System Clock 1)		256fs		12.288	MHz
Frequency (System Clock 2)		384fs		18.432	MHz
Duty Cycle (System Clock 1)		256fs	40	50	%
Duty Cycle (System Clock 2)		384fs	45	50	%
Data Clock Input			32	48	fs
Logic Family Output				CMOS	
Data Clock Output				64	fs
Data Coding				Two's Complement	
Data Bit Length			16	20	Bits
Data Format				Selectable	
Output Data Delay		$f_s = 48\text{kHz}$		1.5	ms
POWER SUPPLY REQUIREMENTS					
Supply Voltage					
$\pm V_{CC}$	PCM1760	± 4.75	± 5.0	± 5.25	V
$\pm V_{DD}$	DF1760	± 4.75	± 5.0	± 5.25	V
$+V_{DD}$	PCM1760	4.75	5.0	5.25	V
Supply Current					
$+I_{CC}$	PCM1760		24	36	mA
$-I_{CC}$	PCM1760		-30	-45	mA
$+I_{DD}$	PCM1760		12	18	mA
$-I_{DD}$	PCM1760		-8	-12	mA
$+I_{DD-1}$	DF1760, Normal Mode		40	55	mA
$+I_{DD-2}$	DF1760, Power-Down Mode		4	6.6	mA
Power Consumption	PCM1760		370	500	mW
	DF1760, Normal Mode		200	275	mW
	DF1760, Power-Down Mode		20	33	mW
TEMPERATURE RANGE					
Operating	PCM1760/DF1760	0	+25	+70	$^\circ\text{C}$
Storage	PCM1760/DF1760	-50		+125	$^\circ\text{C}$

NOTES: (1) Integrator Constants are determined by the external components shown in the block diagram. (2) FSR means Full Scale Range, digital output code is from 90000H to 70000H, FSR = 5.0V. (3) Use 20-bit DAC, 20kHz LPF, 400Hz HPF, average response. (4) Average response using a 20-bit reconstruction DAC with 20kHz low-pass filter and 400Hz high-pass filter.

For Immediate Assistance, Contact Your Local Salesperson

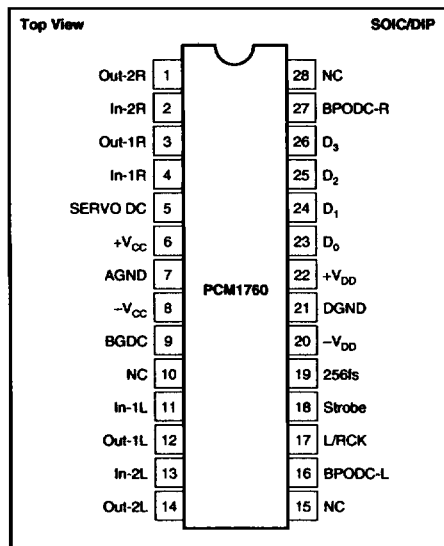
ABSOLUTE MAXIMUM RATINGS—PCM1760

Supply Voltage	±8V
Voltage Mismatch	0.1V
Analog Input	±V _{CC}
Digital Input	+V _{DD} +0.3V GND -0.3V
Power Dissipation/P	580mW
Power Dissipation/U	550mW
Lead Temperature/P (soldering, 10s)	260°C
Lead Temperature/U (soldering, 10s)	235°C
Operating Temperature	0°C to +70°C
Storage Temperature	-50°C to +125°C

ABSOLUTE MAXIMUM RATINGS—DF1760

Supply Voltage	7.0V
Voltage Mismatch	0.1V
Digital Input	+V _{DD} +0.5V V _{SS} -0.5V
Input Current	±20mA
Power Dissipation/P	480mW
Power Dissipation/U	440mW
Lead Temperature/P (soldering, 10s)	260°C
Lead Temperature/U (soldering, 10s, reflow)	235°C
Operating Temperature	0°C to +70°C
Storage Temperature	-50°C to +125°C

PIN CONFIGURATION—PCM1760



PIN ASSIGNMENTS—PCM1760

PIN	I/O ⁽¹⁾	NAME	DESCRIPTION
1	O	Out-2R	Right Channel Second Integrator Output
2	I	In-2R	Right Channel Second Integrator Input
3	O	Out-1R	Right Channel First Integrator Output
4	I	In-1R	Right Channel First Integrator Input
5	-	SERVO DC	Servo Amp Decoupling Capacitor
6	-	+V _{CC}	+5V Analog Supply Voltage
7	-	AGND	Analog Common
8	-	-V _{CC}	-5V Analog Supply Voltage
9	-	BGDC	Band Gap Reference Decoupling Capacitor
10	-	NC	No Connection
11	I	In-1L	Left Channel First Integrator Input
12	O	Out-1L	Left Channel First Integrator Output
13	I	In-2L	Left Channel Second Integrator Input
14	O	Out-2L	Left Channel Second Integrator Output
15	-	NC	No Connection
16	-	BPODC-L	Left Channel Bipolar Offset Decoupling Capacitor
17	O	L/RCK	LR Clock Output (64fs)
18	O	Strobe	Data Strobe Output (128fs)
19	I	256fs	256fs Clock Input
20	-	-V _{DD}	-5V Digital Supply Voltage
21	-	DGND	Digital Common
22	-	+V _{DD}	+5V Digital Supply Voltage
23	O	D ₀	D ₀ Data Output (LSB)
24	O	D ₁	D ₁ Data Output
25	O	D ₂	D ₂ Data Output
26	O	D ₃	D ₃ Data Output (MSB)
27	-	BPODC-R	Right Channel Bipolar Offset Decoupling Capacitor
28	-	NC	No Connection

NOTE: (1) O = Output terminal; I = Input terminal.

PACKAGE INFORMATION

PRODUCT	PACKAGE	PACKAGE DRAWING NUMBER ⁽¹⁾
PCM1760P	28-Pin PDIP	215
PCM1760U	28-Pin SOIC	217
PCM1760P-L	28-Pin PDIP	215
PCM1760U-L	28-Pin SOIC	217
DF1760P	28-Pin PDIP	215
DF1760U	28-Pin SOIC	341

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

ORDERING INFORMATION

PRODUCT	PACKAGE	THD ±N (fs)	SNR
PCM1760P	PDIP	-90dB	108dB
PCM1760U	SOIC	-90dB	108dB
PCM1760P-L	PDIP	-88dB	106dB
PCM1760U-L	SOIC	-88dB	106dB
DF1760P	PDIP	NA	NA
DF1760U	SOIC	NA	NA

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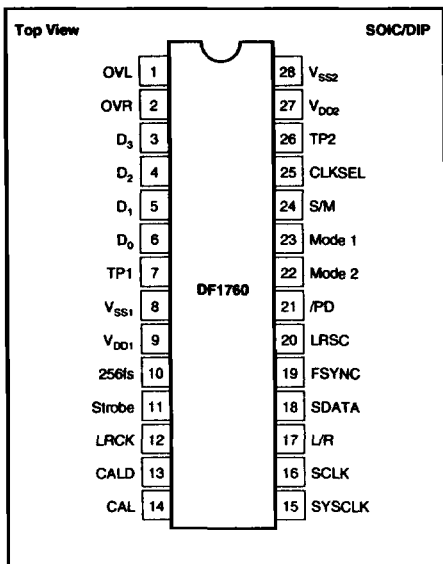
ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

Or, Call Customer Service at 1-800-548-6132 (USA Only)

PIN CONFIGURATION—DF1760

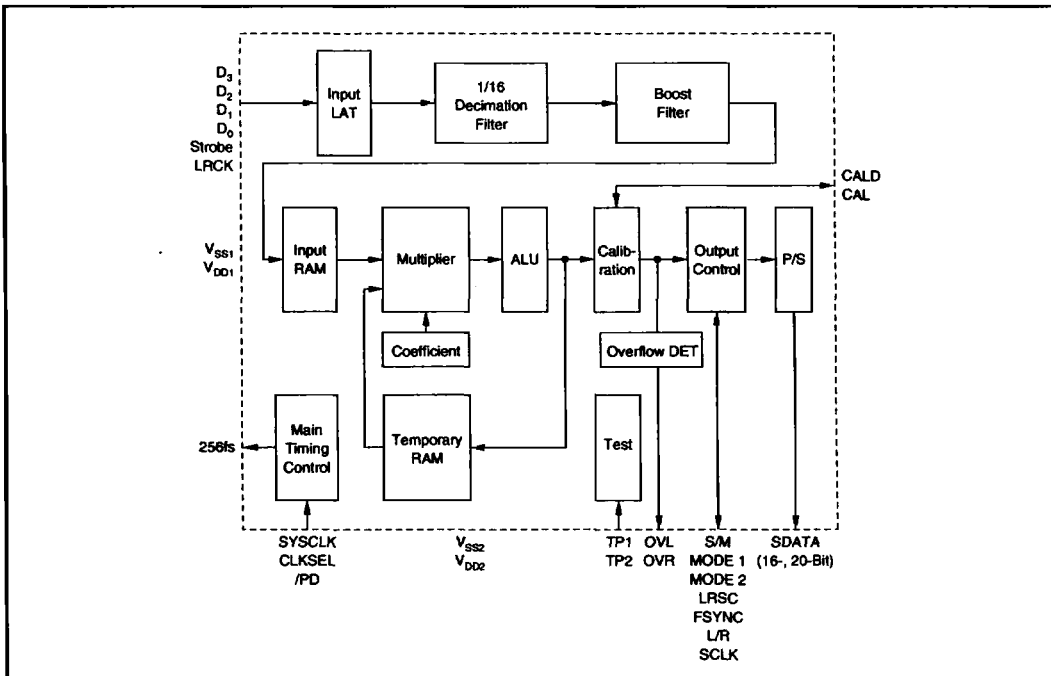


PIN ASSIGNMENTS—DF1760

PIN	I/O ⁽¹⁾	NAME	DESCRIPTION
1	O	OVL	Left Channel Overflow Output (Active High)
2	O	OVR	Right Channel Overflow Output (Active High)
3	I	D ₃	D3 Data Input (MSB)
4	I	D ₂	D2 Data Input
5	I	D ₁	D1 Data Input
6	I	D ₀	D0 Data Input (LSB)
7	-	TP1	Test Pin (No Connection)
8	-	V _{SS1}	Common Channel 1
9	-	V _{DD1}	+5V Channel 1
10	O	256fs	256fs Clock Output
11	I	Strobe	Data Strobe Clock Input (128fs)
12	I	LRCK	LR Clock Input
13	I↑	CALD	Calibration Function Enable (Active Low)
14	O	CAL	Calibration Output (High During Calibration)
15	I	SYSCLK	System Clock Input (256fs or 384fs)
16	I↑/O	SCLK	Data Clock
17	I↑/O	L/R	LR Channel Phase Clock
18	O	SDATA	Serial Data Output (1fs)
19	I↑/O	FSYNC	Frame Clock (2fs)
20	I↑	LRSC	Phase Control of LR Channel Phase Clock
21	I↑	/PD	Power Down Mode Enable Input (Active Low)
22	I↑	Mode2	Output Format Selection Input 2
23	I↑	Mode1	Output Format Selection Input 1
24	I↑	S/M	Slave/Master Mode Selection Input (High Makes Slave Mode)
25	I↑	CLKSEL	System Clock Selection Input (High Makes 256fs)
26	-	TP2	Test Pin (No Connection)
27	-	V _{DD2}	+5V Channel 2
28	-	V _{SS2}	Common Channel 2

NOTE: (1) O = Output terminal; I = Input terminal.

BLOCK DIAGRAM OF DF1760



PCM1760/DF1760 8.1 DIGITAL AUDIO PRODUCTS—A/D