SDC3UV6482-(67/84/100/125)T-S

24MByte (3M x 64) CMOS Synchronous DRAM Module

General Description

The SDC3UV6482-(67/84/100/125)T-S is a high performance, 24-megabtye synchronous, dynamic RAM module organized as 3M words by 64 bits, in a 168-pin, dual-in-line memory module (DIMM) package.

The module utilizes eight Fujitsu MB81117822A-(67/84/100/125)FN CMOS 2Mx8 and four Fujitsu MB811171622A-(67/84/100/125)FN CMOS 1Mx16 synchronous dynamic RAMs in surface mount package (TSOP) on an epoxy laminated substrate. Each device is accompanied by a decoupling capacitor for improved noise immunity.

A 256 Byte Serial EEPROM contains the module configuration information.

Features

- High Density 24MByte
- Cycle Time: 8ns (125MHz), 10ns (100MHz), 12ns (84MHz), 15ns (67MHz)
- Low Power: Active 5.0W (125MHz), 4.6W (100MHz), 4.3W (84MHz), 4.0W (67MHz)
- LVTTL-compatible inputs and outputs
- Separate power and ground planes to improve noise immunity
- Single power supply of 3.3V±0.3V
- Height: 1.150 inch

ABSOLUTE MAXIMUM RATINGS

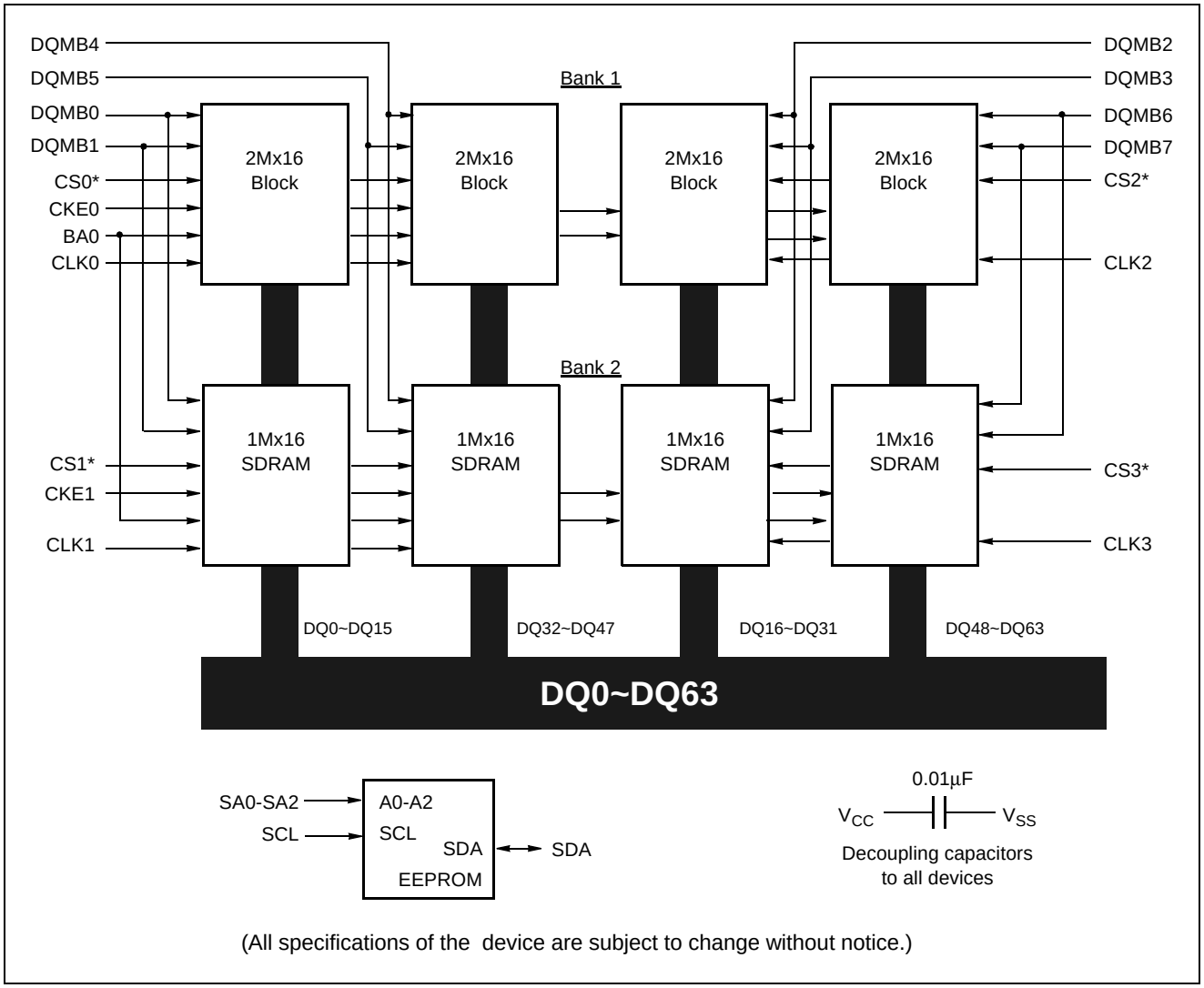
Item	Symbol	Ratings	Unit
Voltage on any pin relative to V_{SS}	V_T	-0.5 to +4.6	V
Power Dissipation	P_T	15.6	W
Operating Temperature	T_{opr}	0 to +70	°C
Storage Temperate	T_{stg}	-55 to +125	°C
Short Circuit Output Current	I_{OS}	±50	mA

RECOMMENDED DC OPERATING CONDITIONS

(T_A = 0 to +70 °C)

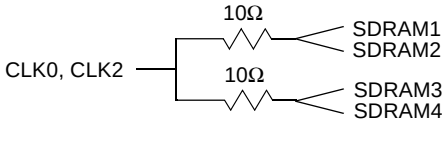
Symbol	Parameter	Min	Typ	Max	Unit
V_{CC}	Supply Voltage	3.0	3.3	3.6	V
V_{SS}	Ground	0	0	0	V
V_{IH}	Input High voltage	2.0	-	V_{CC}+0.5	V
V_{IL}	Input Low voltage	-0.5	-	0.8	V

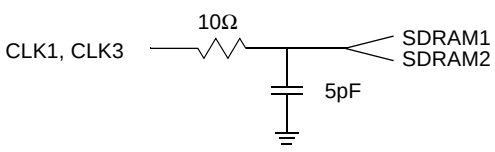
Functional Diagram



(All specifications of the device are subject to change without notice.)

Notes:
1. CKE has a 10K ohm pull-up to Vcc.
2. Data and CLKs are terminated using 10 ohm series resistors.
3. Each 2Mx16 block comprises of two 2Mx8 devices
4. DQMs vs. Data I/Os
   DQMB0 controls DQ0~DQ7
   DQMB1 controls DQ8~DQ15,C0~C7
   DQMB2 controls DQ16~DQ23
   DQMB3 controls DQ24~DQ31
   DQMB4 controls DQ32~DQ39
   DQMB5 controls DQ40~DQ47
   DQMB6 controls DQ48~DQ55
   DQMB7 controls DQ56~DQ63
5. Clock Wiring





Pin Name

A0~A10/AP	Addresses	CS0*~CS3*	Chip Select
BA0	Bank Select Address	WE*	Write Enable
DQ0~DQ63	Data Inputs/Outputs	SA0~SA2	Decode Input
CLK0~CLK3	Clock Inputs	SCL	Serial Clock
RAS*	Row Address Strobes	SDA	Serial Data Input/Output
CAS*	Column Address Strobes	V_{CC}	Power Supply
CKE0, CKE1	Clock Enables	V_{SS}	Ground
DQMB0-DQMB7	DQ Mask Enables	NC	No Connection

Pin No.	Pin Designation	Pin No.	Pin Designation	Pin No.	Pin Designation	Pin No.	Pin Designation
1	V_{SS}	43	V_{SS}	85	V_{SS}	127	V_{SS}
2	DQ0	44	NC	86	DQ32	128	CKE0
3	DQ1	45	CS2*	87	DQ33	129	CS3*
4	DQ2	46	DQMB2	88	DQ34	130	DQMB6
5	DQ3	47	DQMB3	89	DQ35	131	DQMB7
6	V_{CC}	48	NC	90	V_{CC}	132	NC
7	DQ4	49	V_{CC}	91	DQ36	133	V_{CC}
8	DQ5	50	NC	92	DQ37	134	NC
9	DQ6	51	NC	93	DQ38	135	NC
10	DQ7	52	NC	94	DQ39	136	NC
11	DQ8	53	NC	95	DQ40	137	NC
12	V_{SS}	54	V_{SS}	96	V_{SS}	138	V_{SS}
13	DQ9	55	DQ16	97	DQ41	139	DQ48
14	DQ10	56	DQ17	98	DQ42	140	DQ49
15	DQ11	57	DQ18	99	DQ43	141	DQ50
16	DQ12	58	DQ19	100	DQ44	142	DQ51
17	DQ13	59	V_{CC}	101	DQ45	143	V_{CC}
18	V_{CC}	60	DQ20	102	V_{CC}	144	DQ52
19	DQ14	61	NC	103	DQ46	145	NC
20	DQ15	62	NC	104	DQ47	146	NC
21	NC	63	CKE1	105	NC	147	NC
22	NC	64	V_{SS}	106	NC	148	V_{SS}
23	V_{SS}	65	DQ21	107	V_{SS}	149	DQ53
24	NC	66	DQ22	108	NC	150	DQ54
25	NC	67	DQ23	109	NC	151	DQ55
26	V_{CC}	68	V_{SS}	110	V_{CC}	152	V_{SS}
27	WE*	69	DQ24	111	CAS*	153	DQ56
28	DQMB0	70	DQ25	112	DQMB4	154	DQ57
29	DQMB1	71	DQ26	113	DQMB5	155	DQ58
30	CS0*	72	DQ27	114	CS1*	156	DQ59
31	NC	73	V_{CC}	115	RAS*	157	V_{CC}
32	V_{SS}	74	DQ28	116	V_{SS}	158	DQ60
33	A0	75	DQ29	117	A1	159	DQ61
34	A2	76	DQ30	118	A3	160	DQ62
35	A4	77	DQ31	119	A5	161	DQ63
36	A6	78	V_{SS}	120	A7	162	V_{SS}
37	A8	79	CLK2	121	A9	163	CLK3
38	A10 / AP (Note)	80	NC	122	BA0	164	NC
39	NC	81	NC	123	NC	165	SA0
40	V_{CC}	82	SDA	124	V_{CC}	166	SA1
41	V_{CC}	83	SCL	125	CLK1	167	SA2
42	CLK0	84	V_{CC}	126	NC	168	V_{CC}

Note: A10 / AP initiates Auto-precharge

SERIAL PD INFORMATION

		Function Supported				Hex Value			
Byte#	**Function Described**	**125 Mhz**	**100 Mhz**	**84 Mhz**	**67 Mhz**	**125 Mhz**	**100 Mhz**	**84 Mhz**	**67 Mhz**
0	# Bytes Written into serial memory at module mfr	128 bytes				80h			
1	Total # bytes of SPD memory device	256 bytes				08h			
2	Fundamental memory type	SDRAM				04h			
3	# Row Address on this assembly	11,11				BBh			
4	# Column Addresses on this assembly	8,9				89h			
5	# Module Banks on this assembly	2				02h			
6	Data Width of this assembly	64 bits				40h			
7	Data Width of this assembly (continued)					00h			
8	Voltage interface standard of this assembly	LVTTL				01h			
9	SDRAM cycle time at CL=3 (tCLK)	8ns	10ns	12ns	15ns	80h	A0h	C0h	F0h
10	SDRAM Access from Clock at CL=3 (tAC)	7.5ns	8.5ns	8.5ns	9.0ns	75h	85h	85h	90h
11	DIMM configuration type	Non-Parity				00h			
12	Refresh Rate/Type	S/R, Normal 15.6 ms				80h			
13	SDRAM Width Primary DRAM	x8,x16				88h			
14	ECC SDRAM Data Width	N/A				00h			
15	Min. clock delay, Back to Back Random Column Addresses (ICCD)	1CLK				01h			
16	Burst Length Supported	1, 2, 4, 8 & Full				8Fh			
17	# Banks on each SDRAM device	2				02h			
18	CAS# Latency	2, 3				06h			
19	CS# Latency	0				01h			
20	Write Latency	0				01h			
21	SDRAM Module Attribute	Non-Buffered/Registered				00h			
22	SDRAM Device Attribute	Vcc, B/R, S/W, P/A, A/P				0Eh			
23	Min Clock cycle Time at CL=2 (tCLK)	12ns	15ns	17ns	20ns	C0h	F0h	20h	50h
24	Max. Data Access Time from clock at CL=2 (tAC)	9.0ns	9.0ns	9.0ns	10ns	90h	90h	90h	A0h
25	Min Clock cycle Time at CL=1 (tCLK)	N/A				FFh			
26	Max. Data Access Time from clock at CL=1 (tAC)	N/A				FFh			
27	Min. Row Precharge Time (tRP)	27ns	30ns	35ns	40ns	1Bh	1Eh	23h	28h
28	Min. Row Active Delay (tRRD)	24ns	30ns	30ns	30ns	18h	1Eh	1Eh	1Eh
29	Min. RAS to CAS Delay (tRCD)	24ns	30ns	30ns	30ns	18h	1Eh	1Eh	1Eh
30	Min. RAS Pulse Width (tRAS)	48ns	60ns	65ns	70ns	30h	3Ch	41h	46h
31	Module Bank Density	16MB, 8MB				3Ch			
32-61	Superset Information					FFh			
62	SPD Revision	Rev. 1				01h			
63	Checksum for bytes 0-62								

SERIAL PD INFORMATION (CONTINUED)

		Function Supported				Hex Value			
Byte#	**Function Described**	**125 Mhz**	**100 Mhz**	**84 Mhz**	**67 Mhz**	**125 Mhz**	**100 Mhz**	**84 Mhz**	**67 Mhz**
64	Manufacturers JEDEC ID code per JEP-106E	Continuation code				7Fh			
65	Manufacturers JEDEC ID code per JEP-106E	SMART's ID				94h			
66-71	Manufacturers JEDEC ID code per JEP-106E	None				FFh			
72	Manufacturing location	Mfr Specific Data							
73	Manufacturer's Part Number	S				53h			
74	Manufacturer's Part Number	D				44h			
75	Manufacturer's Part Number	C				43h			
76	Manufacturer's Part Number	3				33h			
77	Manufacturer's Part Number	U				55h			
78	Manufacturer's Part Number	V				56h			
79	Manufacturer's Part Number	6				36h			
80	Manufacturer's Part Number	4				34h			
81	Manufacturer's Part Number	8				38h			
82	Manufacturer's Part Number	2				32h			
83	Manufacturer's Part Number	1	1	8	6	31h	31h	38h	36h
84	Manufacturer's Part Number	2	0	4	7	32h	30h	34h	37h
85	Manufacturer's Part Number	5	0	T	T	35h	30h	54h	54h
86	Manufacturer's Part Number	T	T	S	S	54h	54h	53h	53h
87	Manufacturer's Part Number	S	S	None	None	53h	53h	FFh	FFh
88	Manufacturer's Part Number	None				FFh			
89	Manufacturer's Part Number	None				FFh			
90	Manufacturer's Part Number	None				FFh			
91	Revision Code	Mfr Specific Data				Mfr Specific Data			
92	Revision Code	None				FFh			
93	Manufacturing Date	DATE				DATE			
94	Manufacturing Date	DATE				DATE			
95-98	Assembly Serial Number	Serial Number				S.No.			
99	Manufacturer Specific Data	S				53h			
100	Manufacturer Specific Data	M				4Dh			
101	Manufacturer Specific Data	A				41h			
102	Manufacturer Specific Data	R				52h			
103	Manufacturer Specific Data	T				54h			
104	Manufacturer Specific Data	M				4Dh			
105	Manufacturer Specific Data	o				6Fh			
106	Manufacturer Specific Data	d				64h			
107	Manufacturer Specific Data	u				75h			
108	Manufacturer Specific Data	l				6Ch			
109	Manufacturer Specific Data	a				61h			
110	Manufacturer Specific Data	r				72h			
111	Manufacturer Specific Data	T				54h			
112	Manufacturer Specific Data	e				65h			
113	Manufacturer Specific Data	c				63h			
114	Manufacturer Specific Data	h				68h			
115	Manufacturer Specific Data	n				6Eh			
116	Manufacturer Specific Data	o				6Fh			
117	Manufacturer Specific Data	l				6Ch			
118	Manufacturer Specific Data	o				6Fh			
119	Manufacturer Specific Data	g				67h			
120	Manufacturer Specific Data	i				69h			
121	Manufacturer Specific Data	e				65h			
122	Manufacturer Specific Data	s				73h			
123	Manufacturer Specific Data	None				FFh			
124	Manufacturer Specific Data	None				FFh			
125	Manufacturer Specific Data	None				FFh			
126 (*)	INTEL specification frequency	66 Mhz				66h			
127 (*)	INTEL specification CAS# Latency Support	2,3				06h			
128-255	Open for CPQ Use for Read & Write	None				FFh			

(*) INTEL specification extension: These bytes are required for compatibility with previously released systems.

DC CHARACTERISTICS

(V_{CC} = 3.3V±0.3V, V_{SS} = 0V, T_A = 0 to +70 °C)

Parameter	Symbol	Test Condition	125		100		84		67		Unit	Note
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
Operating Current	I_{CC1}	No Burst, t_{CK} = min. t_{RC} = min.	-	920	-	880	-	840	-	800	mA	1, 2
		No Burst, t_{CK} = min., t_{RC} = min. All Banks Active	-	1320	-	1240	-	1160	-	1080	mA	1, 2
Precharge Standby Current	I_{CC2}	CKE -V_{IL}, t_{CK} = min. All Banks Idle	-	24	-	24	-	24	-	24	mA	1, 2
		CKE = V_{IH}, t_{CK} = min. All Banks Idle	-	360	-	360	-	360	-	360	mA	1.2
Active Standby Current	I_{CC3}	CKE = V_{IL}, t_{CK} = min. Any Bank Active	-	360	-	360	-	360	-	360	mA	1, 2
		CKE = V_{IH}, t_{CK} = min. Any Bank Active	-	600	-	600	-	600	-	600	mA	1, 2
Burst Mode Current	I_{CC4}	t_{CK} = min.	-	1400	-	1280	-	1200	-	1120	mA	1, 2
Refresh Current	I_{CC5}	t_{CK} = min., t_{RC} = min., t_{RRD} = min. Auto Refresh	-	1160	-	1080	-	1000	-	920	mA	1, 2
Self Refresh Current	I_{CC6}	CKE - V_{IL}	-	24	-	24	-	24	-	24	mA	1, 2
Input Leakage	I_{LI}	0V ≤ V_{in} ≤ V_{CC}	-120	120	-120	120	-120	120	-120	120	µA	
Output Leakage Current	I_{LO}	0V ≤ V_{out} ≤ V_{CC} D_{out} = Disable	-20	20	-20	20	-20	20	-20	20	µA	
Output High Voltage	V_{OH}	High I_{out} = -2mA	2.4	-	2.4	-	2.4	-	2.4	-	V	
Output Low Voltage	V_{OL}	Low I_{out} = 2 mA	-	0.4	-	0.4	-	0.4	-	0.4	V	

†CL = CAS* Latency

Notes: 1. I_{CC} depends on output load condition when the device is selected I_{CC} (max.) is specified at the output open condition.

2. An initial pulse of 200µs is required after power-up followed by a minimum of eight Auto-Refresh-Cycles.

CAPACITANCE

(TA =+25°C, VCC = 3.3V±0.3V)

Parameter	Symbol	Max.	Unit	Note
Input Capacitance (Address, WE*, CKE, RAS*, CAS*)	C_{I1}	53	pF	1
Input Capacitance (DQMBs)	C_{I2}	17	pF	1
Input Capacitance (CS0*,CS2*,CLK0,CLK2)	C_{I3}	21	pF	1
Input Capacitance (CLK1,CLK3,CS1*,CS3*)	C_{I4}	13	pF	1
Input/Output Capacitance (DQ0~DQ63)	$C_{I/O}$	19	pF	1, 2

Notes: 1. Capacitance is measured with Boonton Meter or effective capacitance method.

2. CAS* - V_{IH} to disable D_{out}.

AC CHARACTERISTICS

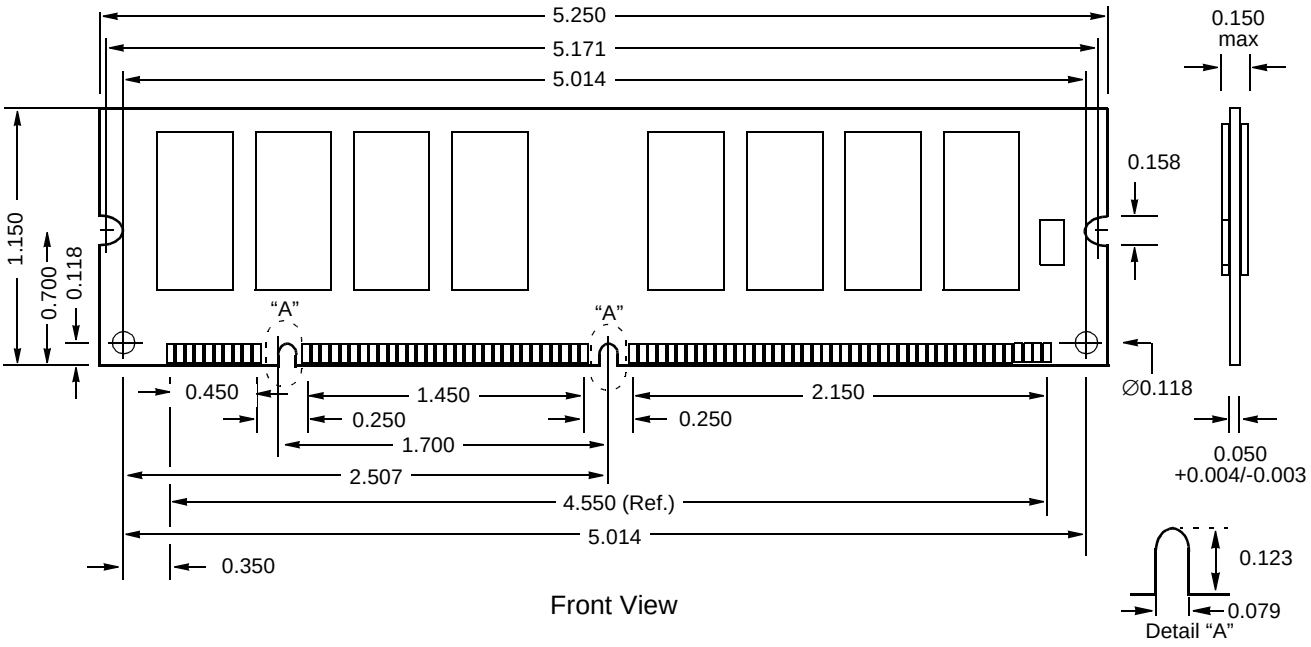
(TA = 0 to +70°C, V_{CC} = 3.3V±0.3V, V_{SS} = 0V)

Parameter		Symbol	Unit	125		100		84		67		Notes
Clock Period	CL=3	t_{CLK}	ns	8	-	10	-	12	-	15	-	1, 2, 3, 6
	CL=2			12	-	15	-	17	-	20	-	
Transition Time		t_T	ns	0.5	2	0.5	2	0.5	2	0.5	2	1, 2, 3
Clock High Time		t_{CH}	ns	3.5	-	4	-	4	-	4	-	1, 2, 3
Clock Low Time		t_{CL}	ns	3.5	-	4	-	4	-	4	-	1, 2, 3
CS Setup Time		t_{SC}	ns	3.0	-	3.0	-	3.0	-	3.0	-	1, 2, 3
CS Hold Time		t_{HC}	ns	1.0	-	1.0	-	1.0	-	1.0	-	1, 2, 3
Input Setup Time		t_{SI}	ns	3.0	-	3.0	-	3.0	-	3.0	-	1, 2, 3
Input Hold Time		t_{HI}	ns	1.0	-	1.0	-	1.0	-	1.0	-	1, 2, 3
Output Valid from Clock	CL=3	t_{AC}	ns	-	7.5	-	8.5	-	8.5	-	9.0	1, 2, 3
	CL=2			-	9		9	-	9	-	10	
Output In Low-Z		t_{OLZ}	ns	2	-	3	-	3	-	3	-	1, 2, 3
Output in High-Z		t_{OHZ}	ns	2	-	3	-	3	-	3	-	1, 2, 3, 4
Output Hold Time		t_{OH}	ns	2	-	3	-	3	-	3	-	1, 2, 3
Time between Refresh		t_{REF}	ms	-	32.8	-	32.8	-	32.8	-	32.8	1, 2, 3
RAS Cycle Time		t_{RC}	ns	75	-	90	-	100	-	110	2	1, 2, 3, 5
RAS Access Time		t_{RAC}	ns	-	45	-	54	-	56	-	60	1, 2, 3
CAS Access Time		t_{CAC}	ns	-	21	-	24	-	26	-	30	1, 2, 3
RAS Precharge Time		t_{RP}	ns	27	-	30	-	35	-	40	-	1, 2, 3
RAS Active Time		t_{RAS}	ns	48	10000	60	10000	65	-	70	10000	1, 2, 3
RAS to CAS Delay Time		t_{RCD}	ns	24	-	30	-	30	-	30	-	1, 2, 3
Write Recovery Time		t_{WR}	ns	8	-	10	-	12	-	15	-	1, 2, 3
Write to Precharge Lead Time		t_{RWL}	ns	8	-	10	-	12	-	15	-	1, 2, 3
RAS to RAS Delay Time		t_{RRD}	ns	24	-	30	-	30	-	30	-	1, 2, 3
Power-down Exit Time		t_{PDE}	ns	3	-	3	-	4	-	5	-	1, 2, 3
CKE to Clock Disable		l_{CKE}	cycle	1		1		1		1		
DQM to Output in High-Z		l_{DQZ}	cycle	2		2		2		2		
DQM to Input Data Delay		l_{DQD}	cycle	0		0		0		0		
Last Output to Write Command Delay		l_{OWD}	cycle	2		2		2		2		
Write Command to Input Data Delay		l_{DWD}	cycle	0		0		0		0		
Precharge to Output in High-Z Delay	CL=3	l_{ROH}	cycle	3		3		3		3		
	CL=2			2		2		2		2		
Mode Register Access to Bank Active (min.)		l_{MRD}	cycle	2		2		2		2		
CAS to CAS Delay		l_{CCD}	cycle	1		1		1		1		
CAS Bank Delay		l_{CBD}	cycle	1		1		1		1		

Notes:
1. An initial pulse of at least 200µs is required after power-up followed by a minimum of eight auto refresh cycles.
2. AC characteristics assume t_T = 1ns and 50pF capacitive load. If t_T is longer than 1ms, reference level for measuring time of input signal is V_{IH} (min.) and V_{IL} (max.).
3. 1.4V is the reference level for measuring timing of input signals.
4. t_{HZ} and t_{OH} defines the time at which the outputs achieve ±200mV.
5. Actual clock output of t_{RC} will be sum clock of t_{RAS} and t_{RP}.
6. 20ns is not supported in SPD.

Physical Dimensions

168-pin (84x2) DIMM



Front View

Notes: 1. All dimensions are in inches.
2. Pin 85 is behind pin 1 on the back side.

Ordering Information

S D C 3 U V 64 8 2 _ _ - 100 T - _ S

(1) (2) (3) (4) (5) (6) (7) (8) (8a) (9) (10) (11) (12) (13) (14)

(1) **Memory Type**
S : SDRAM
G : SGRAM

(2) **Module Shape**
S : SIMM
D : DIMM
O : Small Outline DIMM

(3) **Module Pin Count**
A : 72-pin
B : 144-pin
C : 168-pin
D : 200-pin

(4) **Word Depth**
1 : 1M
2 : 2M
4 : 4M
8 : 8M
256 : 256K
512 : 512K

(5) **Buffer Type**
B : Buffered
U : Unbuffered

(6) **Operating Voltage & Power Consumption**
V : 3.3V & Standard Power
L : 3.3V & Low Power

(7) **Data Width**
(ex. 64=x64, 72=x72 etc.)

(8) **Device Configuration**
4 : x4
8 : x8
1 : x16
3 : x32

(8a) **Refresh**
2 : 2krf
4 : 4krf

(9) **Interface Level**
Blank : LVTTL
S : SSTL

(10) **Module Revision / Applied "Standard" *1**
Blank : Rev. 0
A : Rev. 1
B : Rev. 2 (etc.)

*1 When DRAM device or PCB is revised, the revision is changed

(11) **Clock Frequency**
67 : 67Mhz
84 : 84Mhz
100 : 100Mhz
125 : 125Mhz

(12) **Package of Component**
J : SOJ
T : TSOP

(13) **Private Brand Name *2**
Blank : Common Products
G : FMG Brand

*2 This column is applicable to custom modules, NOT applicable to JEDEC standard commodity products

(14) **Assembly & Test Site**
S : Smart Modular Technologies

FUJITSU LIMITED

For further information please contact:

Japan

FUJITSU LIMITED
Memory Marketing Dept.
4-1-1, Kamikodanaka Nakahara-ku,
Kawasaki 211-88, Japan
Tel: +81-44-754-3767
Fax: +81-44-754-3343

Internet: http://www.fujitsu.co.jp/

North and South America

FUJITSU MICROELECTRONICS, INC.
3545 North First Street
San Jose, CA 95134-1804, USA.
Tel: +1-408-922-9000
Fax: +1-408-922-9179

Customer Response Center (Mon-Fri: 7am-5pm (PST))
Tel: +1-800-866-8608
Fax: +1-408-922-9179

Internet: http://www.fujitsumicro.com/

Europe

FUJITSU MIKROELEKTRONIK GmbH
Am Siebenstein 6-10
63303 Dreieich–Buchschlag
Germany
Tel: +49-6103-690-0
Fax: +49-6103-690-122

Internet: http://www.fujitsu-ede.com/

Asia

FUJITSU MICROELECTRONICS ASIA PTE LIMITED
#05-08, 151 Lorong Chuan
NewTechPark
Singapore 556741
Tel: +65-281-0770
Fax: +65-281-0220

Internet: http://www.fsl.com.sg/

MP-DRAMM-DS-20539-7/97