10-bit bus transceiver (3-State)

74ABT861

FEATURES

- Provides high performance bus interface buffering for wide data/address paths or buses carrying parity
- Buffered control inputs for light loading, or increased fan-in as required with MOS microprocessors
- Output capability: +64mA/–32mA
- Latch-up protection exceeds 500mA per Jedec Std 17
- ESD protection exceeds 2000 V per MIL STD 883 Method 3015 and 200 V per Machine Model
- Power-up 3-State
- Inputs are disabled during 3-State mode

DESCRIPTION

The 74ABT861 bus transceiver provides high performance bus interface buffering for wide data/address paths of buses carrying parity.

The 74ABT861 10-bit bus transceiver has NOR-ed transmit and receive output enables for maximum control flexibility.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25°C; GND = 0V	TYPICAL	UNIT
t_{PLH} t_{PHL}	Propagation delay An to Bn or Bn to An	C_L = 50pF; V_{CC} = 5V	3.4	ns
C_{IN}	Input capacitance	V_I = 0V or V_{CC}	4	pF
$C_{I/O}$	I/O capacitance	Outputs disabled; V_O = 0V or V_{CC}	7	pF
I_{CCZ}	Total supply current	Outputs disabled; V_{CC} =5.5V	500	nA

ORDERING INFORMATION

| PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	DWG NUMBER
24-Pin Plastic DIP	–40°C to +85°C	74ABT861 N	74ABT861 N	SOT222-1
24-Pin plastic SO	–40°C to +85°C	74ABT861 D	74ABT861 D	SOT137-1
24-Pin Plastic SSOP Type II	–40°C to +85°C	74ABT861 DB	74ABT861 DB	SOT340-1
24-Pin Plastic TSSOP Type I	–40°C to +85°C	74ABT861 PW	74ABT861PW DH	SOT355-1

PIN CONFIGURATION

$\overline{OEBA}$ [1]	[24] V_{CC}
A0 [2]	[23] B0
A1 [3]	[22] B1
A2 [4]	[21] B2
A3 [5]	[20] B3
A4 [6]	[19] B4
A5 [7] TOP VIEW	[18] B5
A6 [8]	[17] B6
A7 [9]	[16] B7
A8 [10]	[15] B8
A9 [11]	[14] B9
GND [12]	[13] $\overline{OEAB}$

SA00278
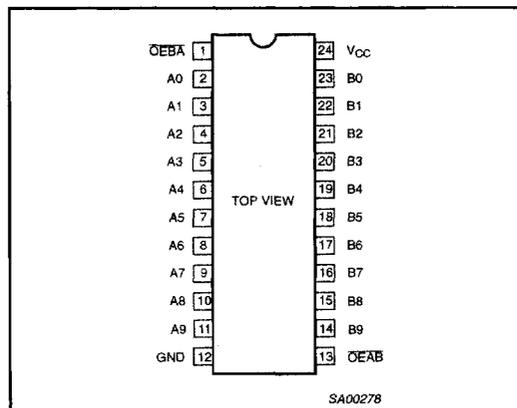
PIN DESCRIPTION

PIN NUMBER	SYMBOL	FUNCTION
13	$\overline{OEAB}$	A side to B side output enable input (active-Low)
2, 3, 4, 5, 6, 7, 8, 9, 10, 11	A0-A9	Data inputs/outputs (A side)
23, 22, 21, 20, 19, 18, 17, 16, 15, 14	B0-B9	Data inputs/outputs (B side)
1	$\overline{OEBA}$	B side to A side output enable input (active-Low)
12	GND	Ground (0V)
24	V_{CC}	Positive supply voltage

10-bit bus transceiver (3-State)

LOGIC SYMBOL

SA00279
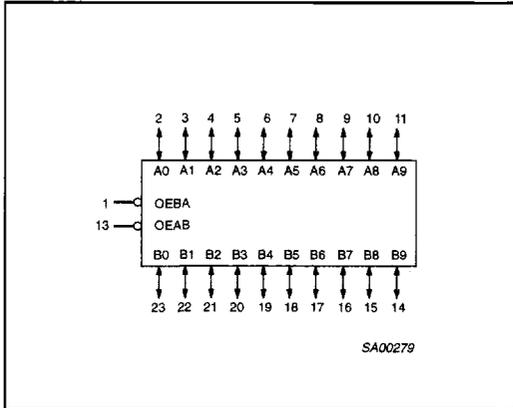
LOGIC SYMBOL (IEEE/IEC)

SA00280

LOGIC DIAGRAM

SA00281
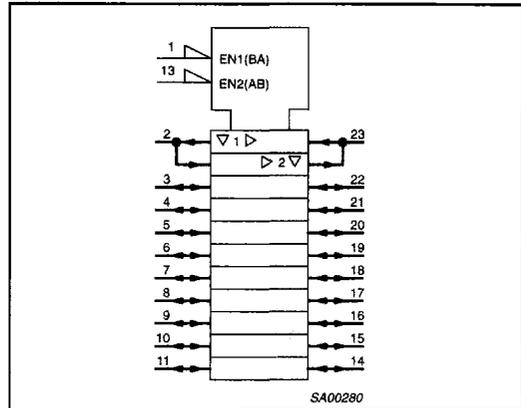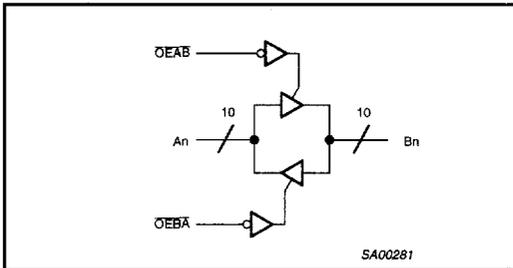
FUNCTION TABLE

INPUTS		OPERATING
$\overline{\text{OEAB}}$	$\overline{\text{OEBA}}$	MODE
L	H	A data to B bus
H	L	B data to A bus
H	H	Z

H = High voltage level
L = Low voltage level
X = Don't care
Z = High impedance "off" state

ABSOLUTE MAXIMUM RATINGS[1, 2]

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		−0.5 to +7.0	V
I_{IK}	DC input diode current	$V_I < 0$	−18	mA
V_I	DC input voltage[3]		−1.2 to +7.0	V
I_{OK}	DC output diode current	$V_O < 0$	−50	mA
V_{OUT}	DC output voltage[3]	output in Off or High state	−0.5 to +5.5	V
I_{OUT}	DC output current	output in Low state	128	mA
T_{stg}	Storage temperature range		−65 to 150	°C

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150°C.
3. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

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RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS		UNIT
		Min	Max	
V_{CC}	DC supply voltage	4.5	5.5	V
V_I	Input voltage	0	V_{CC}	V
V_{IH}	High-level input voltage	2.0		V
V_{IL}	Low-level input voltage		0.8	V
I_{OH}	High-level output current		−32	mA
I_{OL}	Low-level output current		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	0	5	ns/V
T_{amb}	Operating free-air temperature range	−40	+85	°C

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER		TEST CONDITIONS	LIMITS					UNIT
				T_{amb} = +25°C			T_{amb} = −40°C to +85°C		
				Min	Typ	Max	Min	Max	
V_{IK}	Input clamp voltage		V_{CC} = 4.5V; I_{IK} = −18mA		−0.9	−1.2		−1.2	V
V_{OH}	High-level output voltage		V_{CC} = 4.5V; I_{OH} = −3mA; V_I = V_{IL} or V_{IH}	2.5	3.5		2.5		V
			V_{CC} = 5.0V; I_{OH} = −3mA; V_I = V_{IL} or V_{IH}	3.0	4.0		3.0		V
			V_{CC} = 4.5V; I_{OH} = −32mA; V_I = V_{IL} or V_{IH}	2.0	2.6		2.0		V
V_{OL}	Low-level output voltage		V_{CC} = 4.5V; I_{OL} = 64mA; V_I = V_{IL} or V_{IH}		0.42	0.55		0.55	V
I_I	Input leakage current	Control pins	V_{CC} = 5.5V; V_I = GND or 5.5V		±0.01	±1.0		±1.0	μA
		Data pins	V_{CC} = 5.5V; V_I = GND or 5.5V		±5.0	±100		±100	μA
I_{OFF}	Power-off leakage current		V_{CC} = 0.0V; V_O or V_I ≤ 4.5V		±5.0	±100		±100	μA
$I_{PU/PD}$	Power-up/down 3-State output current[3]		V_{CC} = 2.1V; V_O = 0.5V; V_I = GND or V_{CC}; V_{OE} = V_{CC}		±5.0	±50		±50	μA
$I_{IH} + I_{OZH}$	3-State output High current		V_{CC} = 5.5V; V_O = 2.7V; V_I = V_{IL} or V_{IH}		5.0	50		50	μA
$I_{IL} + I_{OZL}$	3-State output Low current		V_{CC} = 5.5V; V_O = 0.5V; V_I = V_{IL} or V_{IH}		−5.0	−50		−50	μA
I_{CEX}	Output high leakage current		V_{CC} = 5.5V; V_O = 5.5V; V_I = GND or V_{CC}		5.0	50		50	μA
I_O	Output current[1]		V_{CC} = 5.5V; V_O = 2.5V	−50	−100	−180	−50	−180	mA
I_{CCH}	Quiescent supply current		V_{CC} = 5.5V; Outputs High, V_I = GND or V_{CC}		0.5	250		250	μA
I_{CCL}			V_{CC} = 5.5V; Outputs Low, V_I = GND or V_{CC}		25	38		38	mA
I_{CCZ}			V_{CC} = 5.5V; Outputs 3-State; V_I = GND or V_{CC}		0.5	50		50	μA
ΔI_{CC}	Additional supply current per input pin[2]		Outputs enabled, one input at 3.4V, other inputs at V_{CC} or GND; V_{CC} = 5.5V		0.5	1.5		1.5	mA
			Outputs 3-State, one data input at 3.4V, other inputs at V_{CC} or GND; V_{CC} = 5.5V		0.01	50		50	μA
			Outputs 3-State, one enable input at 3.4V, other inputs at V_{CC} or GND; V_{CC} = 5.5V		0.5	1.5		1.5	mA

NOTES:
1. Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
2. This is the increase in supply current for each input at 3.4V.
3. This parameter is valid for any V_{CC} between 0V and 2.1V with a transition time of up to 10msec. For V_{CC} = 2.1V to V_{CC} = 5V ± 10%, a transition time of up to 100μsec is permitted.

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74ABT861

AC CHARACTERISTICS

GND = 0V, t_R = t_F = 2.5ns, C_L = 50pF, R_L = 500Ω

SYMBOL	PARAMETER	WAVEFORM	LIMITS					UNIT
			T_{amb} = +25°C V_{CC} = +5.0V			T_{amb} = -40 to +85°C V_{CC} = +5.0V ±0.5V		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay An to Bn or Bn to An	1	1.1 1.0	3.4 3.2	4.9 4.9	1.1 1.0	5.2 5.2	ns
t_{PZH} t_{PZL}	Output enable time to High and Low level	2	1.2 2.4	3.5 4.6	5.0 6.0	1.2 2.4	5.9 6.9	ns
t_{PHZ} t_{PLZ}	Output disable time from High and Low level	2	3.1 3.7	5.3 5.3	6.5 6.6	3.1 3.7	7.5 7.1	ns

AC WAVEFORMS

V_M = 1.5V, V_{IN} = GND to 3.0V
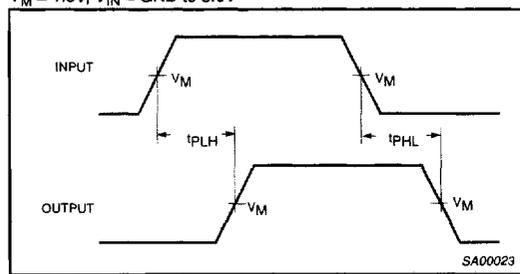
Waveform 1. Input to Output Propagation Delays
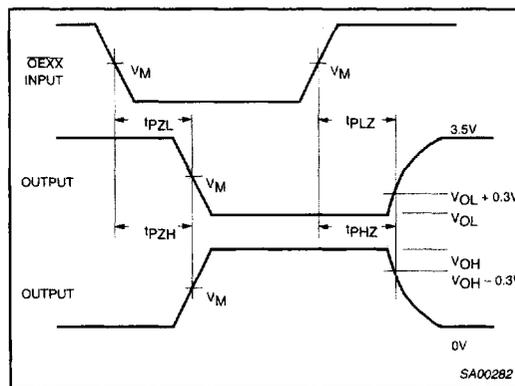

Waveform 2. 3-State Output Enable and Disable Times

# 10-bit bus transceiver (3-State)

TEST CIRCUIT AND WAVEFORM
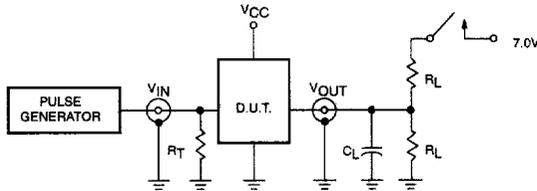
Test Circuit for 3-State Outputs

Input Pulse Definition

$V_M = 1.5V$

SWITCH POSITION

TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.
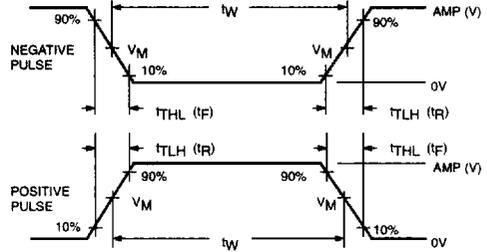
FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_R	t_F
74ABT	3.0V	1MHz	500ns	2.5ns	2.5ns

SA00012