

# LH534500A

CMOS 4M (512K × 8/256K × 16)  
Mask-Programmable ROM

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## FEATURES

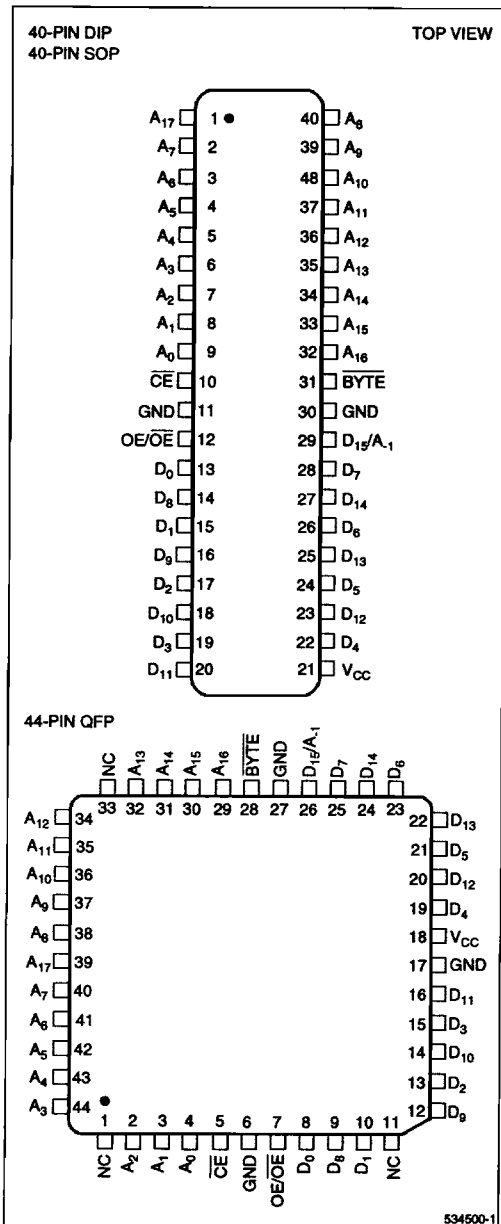
- Memory organization selection:
  - 524,288 × 8 bit (byte mode)
  - 262,144 × 16 bit (word mode)
- $\overline{\text{BYTE}}$  input pin selects bit configuration
- Access time: 150 ns (MAX.)
- Low-power consumption:
  - Operating: 275 mW (MAX.)
  - Standby: 550  $\mu$ W (MAX.)
- Static operation (Internal sync. system)
- TTL compatible I/O
- Three-state outputs
- Single +5 V power supply

- Packages:
  - 40-pin, 600-mil DIP
  - 40-pin, 525-mil SOP
  - 48-pin, 12 × 18 mm<sup>2</sup> TSOP (Type I)
  - 44-pin, 14 × 14 mm<sup>2</sup> QFP
- ×16 word-wide pinout

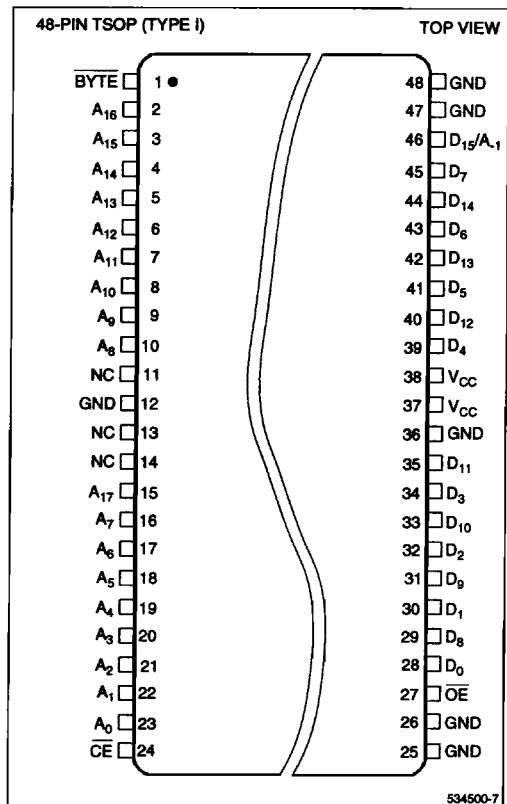
## DESCRIPTION

The LH534500A is a 4M bit mask-programmable ROM with two programmable memory organizations of byte and word modes. It is fabricated using silicon-gate CMOS process technology.

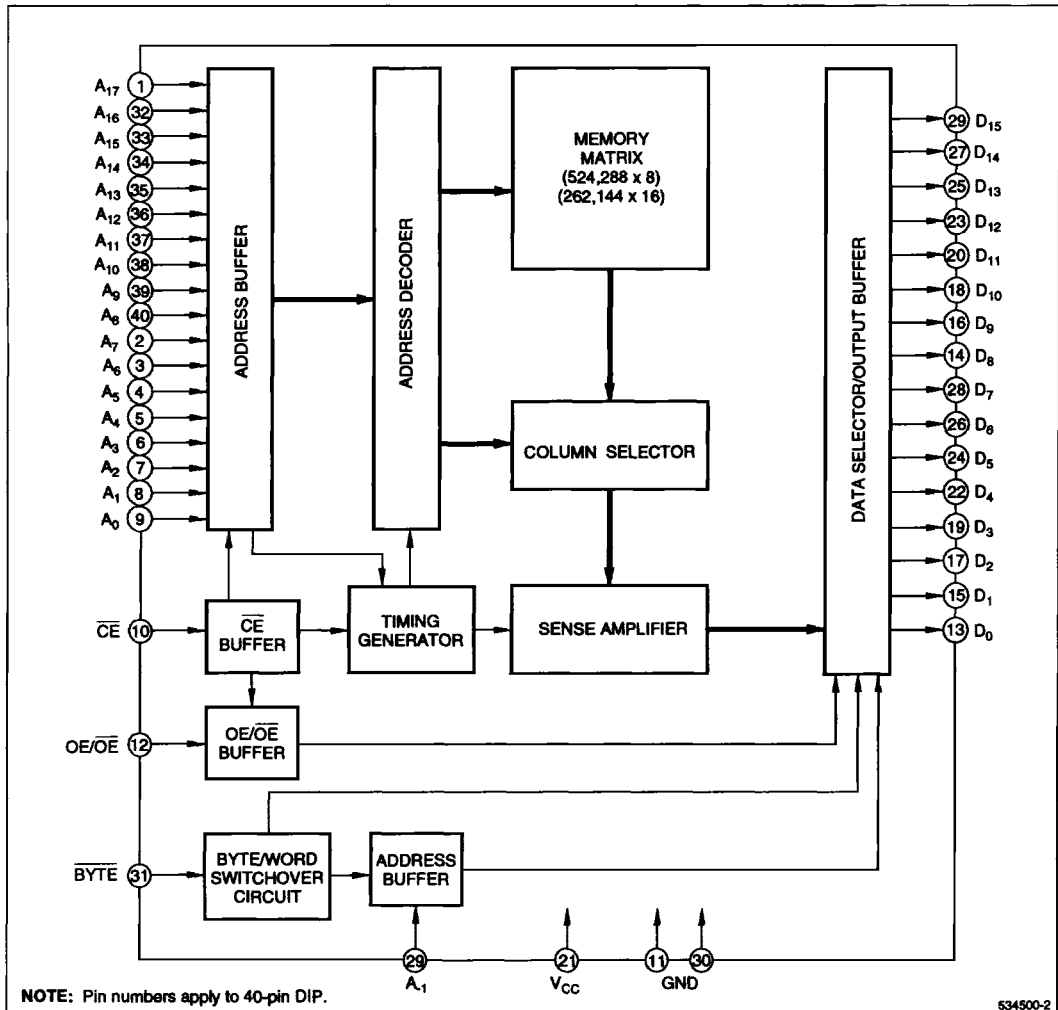
**PIN CONNECTIONS**



**Figure 1. Pin Connections for DIP, SOP, and QFP Packages**



**Figure 2. Pin Connections for TSOP Package**



534500-2

Figure 3. LH534500A Block Diagram

**PIN DESCRIPTION**

SIGNAL	PIN NAME	NOTE
A <sub>1</sub>	Address input	1
A <sub>0</sub> - A <sub>17</sub>	Address input	
D <sub>0</sub> - D <sub>15</sub>	Data output	
CE	Chip Enable input	

SIGNAL	PIN NAME	NOTE
OE/OE	Chip Enable input	2
BYTE	Byte/word mode switch	
V <sub>CC</sub>	Power supply (+5 V)	
GND	Ground	

**NOTES:**

1. D<sub>15</sub>/A<sub>1</sub> pin becomes LSB address input (A<sub>1</sub>) when the bit configuration is set in byte mode, and data output (D<sub>15</sub>) when in word mode. BYTE input pin selects bit configuration.
2. Active level of OE/OE is mask-programmable.

## TRUTH TABLE

$\overline{CE}$	OE/ $\overline{OE}$	BYTE	A <sub>1</sub>	MODE	D <sub>0</sub> - D <sub>7</sub>	D <sub>8</sub> - D <sub>15</sub>	SUPPLY CURRENT
H	X	X	X	Non selected	High-Z		Standby (I <sub>SB</sub> )
L	L/H	X	X	Non selected	High-Z		Operating (I <sub>CC</sub> )
L	H/L	H	Inhibit	Word	D <sub>0</sub> - D <sub>7</sub>	D <sub>8</sub> - D <sub>15</sub>	Operating (I <sub>CC</sub> )
L	H/L	L	L	Byte	D <sub>0</sub> - D <sub>7</sub>	High-Z	Operating (I <sub>CC</sub> )
L	H/L	L	H	Byte	D <sub>8</sub> - D <sub>15</sub>	High-Z	Operating (I <sub>CC</sub> )

## NOTE:

X = High or Low

The input state of BYTE must not be changed during operation. The BYTE pin must be set to either High or Low.

## ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	RATING	UNIT	NOTE
Supply voltage	V <sub>CC</sub>	-0.3 to +7.0	V	1
Input voltage	V <sub>IN</sub>	-0.3 to V <sub>CC</sub> +0.3	V	
Output voltage	V <sub>OUT</sub>	-0.3 to V <sub>CC</sub> +0.3	V	
Operating temperature	T <sub>opr</sub>	0 to +70	°C	
Storage temperature	T <sub>stg</sub>	-55 to +150	°C	

## NOTE:

1. The maximum applicable voltage on any pin with respect to GND

RECOMMENDED OPERATING CONDITIONS (T<sub>A</sub> = 0 to +70°C)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Supply voltage	V <sub>CC</sub>	4.5	5.0	5.5	V

DC CHARACTERISTICS (V<sub>CC</sub> = 5 V ±10%, T<sub>A</sub> = 0 to +70°C)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT	NOTE
Input 'Low' voltage	V <sub>IL</sub>		-0.3		0.8	V	
Input 'High' voltage	V <sub>IH</sub>		2.2		V <sub>CC</sub> +0.3	V	
Output 'Low' voltage	V <sub>OL</sub>	I <sub>OL</sub> = 2.0 mA			0.4	V	
Output 'High' voltage	V <sub>OH</sub>	I <sub>OH</sub> = -400 μA	2.4			V	
Input leakage current	I <sub>LI</sub>	V <sub>IN</sub> = 0 V to V <sub>CC</sub>			10	μA	
Output leakage current	I <sub>LO</sub>	V <sub>OUT</sub> = 0 V to V <sub>CC</sub>			10	μA	1
Operating current	I <sub>CC1</sub>	t <sub>RC</sub> = 150 ns			50	mA	2
	I <sub>CC2</sub>	t <sub>RC</sub> = 1 μs			45		
	I <sub>CC3</sub>	t <sub>RC</sub> = 150 ns			45	mA	3
	I <sub>CC4</sub>	t <sub>RC</sub> = 1 μs			40		
Standby current	I <sub>SB1</sub>	$\overline{CE} = V_{IH}$			5	mA	
	I <sub>SB2</sub>	$\overline{CE} = V_{CC} - 0.2 V$			100		

## NOTES:

- OE = V<sub>IL</sub>,  $\overline{CE}/\overline{OE} = V_{IH}$
- V<sub>IN</sub> = V<sub>IH</sub>/V<sub>IL</sub>,  $\overline{CE} = V_{IL}$ , outputs open
- V<sub>IN</sub> = (V<sub>CC</sub> - 0.2 V) or 0.2 V,  $\overline{CE} = 0.2 V$ , outputs open

**AC CHARACTERISTICS ( $V_{CC} = 5 V \pm 10\%$ ,  $T_A = 0$  to  $+70^\circ C$ )**

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	NOTE
Read cycle time	$t_{RC}$	150			ns	
Address access time	$t_{AA}$			150	ns	
Chip enable access time	$t_{ACE}$			150	ns	
Output enable delay time	$t_{OE}$			70	ns	
Output hold time	$t_{OH}$	5			ns	
CE to output in High-Z	$t_{CHZ}$			70	ns	1
OE to output in High-Z	$t_{OHZ}$			70	ns	

**NOTE:**

1. This is the time required for the outputs to become high-impedance.

**AC TEST CONDITIONS**

PARAMETER	RATING
Input voltage amplitude	0.6 V to 2.4 V
Input rise/fall time	10 ns
Input reference level	1.5 V
Output reference level	0.8 V and 2.2 V
Output load condition	1TTL +100 pF

**CAPACITANCE ( $V_{CC} = 5 V \pm 10\%$ ,  $f = 1$  MHz,  $T_A = 25^\circ C$ )**

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Input capacitance	$C_{IN}$			10	pF
Output capacitance	$C_{OUT}$			10	pF

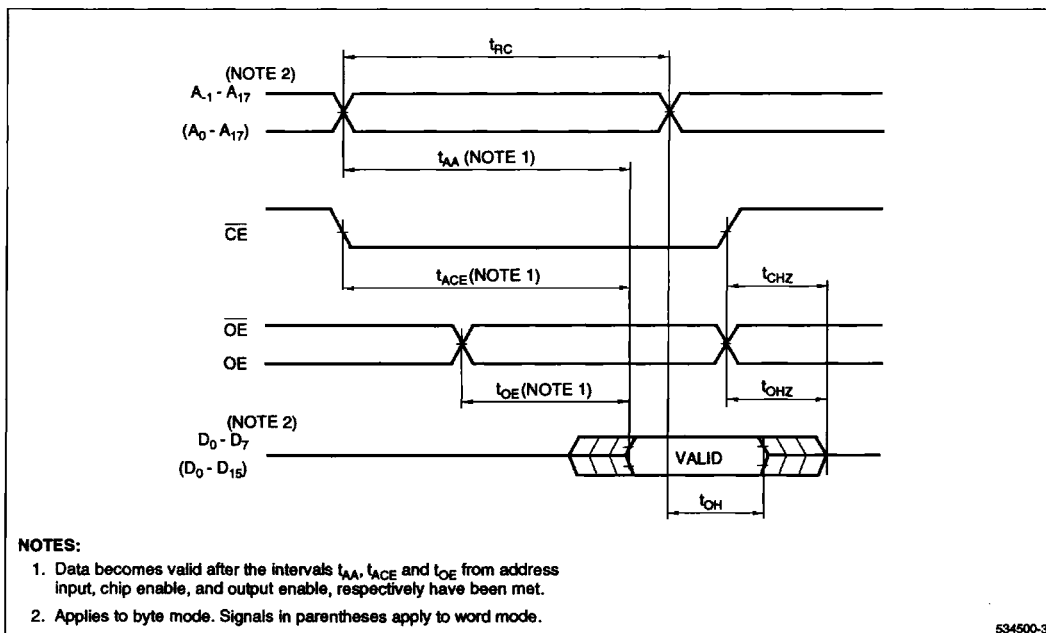


Figure 4. Timing Diagram

**ORDERING INFORMATION**

