SALI-25C Device
Six ATM Line Interface at 25 Mbit/s
TXC-07625

DATA SHEET

FEATURES

- Transmission Convergence
  - meets ATM Forum specifications
  - maps ATM cells to six 25.6 Mbit/s payloads
  - NRZI/NRZ and 5B/4B conversions
  - scrambling, cell delineation and rate adaptation
  - HEC generate/check with bad cell discard
  - transmit GFC insertion for Xon/Xoff
- Line Interface
  - six independent lines each with data and clock
  - line rate at 32 Mbaud +/- 100ppm
  - detects received illegal 5B codes
  - direct interface to 25 Mbit/s 5 volt transceivers
  - idle signal generation on the line side
  - single transmit clock input for all six line signals
  - 8 kHz timing marker output
- 8-bit 33 MHz or UTOPIA Level 1 and 2 Interface
  - single cell available cell level control
  - 3 cells per line FIFO in the receive direction
  - 2 cells per line FIFO in the transmit direction
  - optional 4 priority queues per line sharing 2048 or 4096-cell external SRAM buffer for transmit
- Discarded, received and transmitted cell counts
- External memory (SRAM) interface
- External transceiver and LED controls
- Intel/Motorola processor interface with interrupts
- Test Access Port (IEEE 1149.1 boundary scan)
- Single +3.3 V, ±5% power supply, 0.6W max.
- 208-pin plastic quad flat package

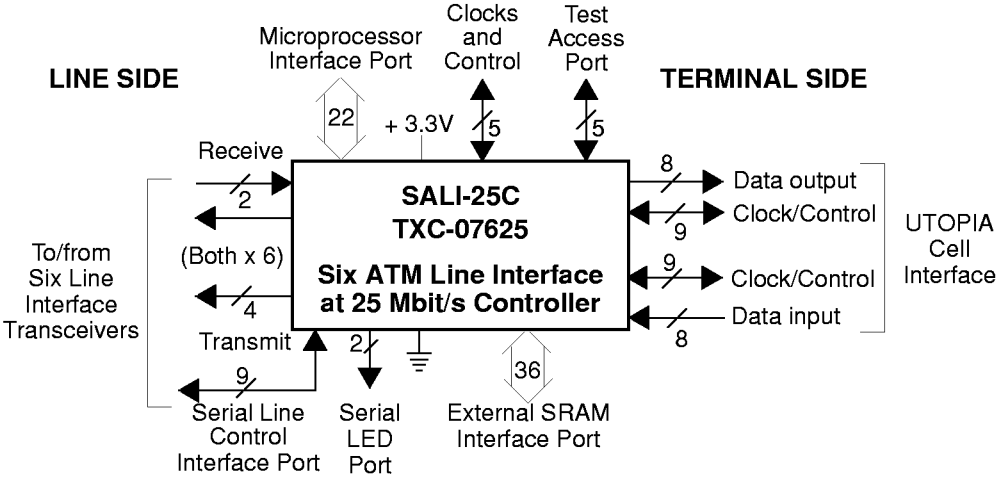
DESCRIPTION

The SALI-25C VLSI device is a controller for six 25.6 Mbit/s ATM Line Interfaces, with a common 8-bit parallel transmit and receive UTOPIA interface on the terminal side. It performs the transmission convergence function of six independent 25.6 Mbit/s bit-serial line signals used for connection to private UNIs, and the terminal side interface employs single cell I/O signals.

The device is designed to interface directly on the line side with PMD devices such as the TranSwitch ALI-25T ATM Line Interface 25 Mbit/s Transceiver (part number TXC-07225-BCPL). It performs NRZI/NRZ conversion, data deserialization, 5B/4B decoding, descrambling, cell delineation, and idle byte discard in the receive direction, and the inverse processes in the transmit direction. The SALI-25C provides an 8-bit 33 MHz multi-PHY UTOPIA cell interface with ATM layer devices. The SALI-25C also provides a special UTOPIA mode for interfacing with the TranSwitch CUBIT or CUBIT-*Pro* *CellBus* Bus Switch VLSI device (TXC-05801 or TXC-05802).

APPLICATIONS

- PC and Work-station Network Interface Adaptors
- ATM Concentrators
- ATM Hubs
- Local and Campus ATM Switches
- ATM Access Switches



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* Please note that TranSwitch provides documentation for all of its products. Customers who are using a TranSwitch Product, or planning to do so, should register with the TranSwitch Marketing Department to receive relevant updated and supplemental documentation as it is issued. They should also contact the Applications Engineering Department to ensure that they are provided with the latest available information about the product, especially before undertaking development of new designs incorporating the product.

LIST OF FIGURES

REFERENCES

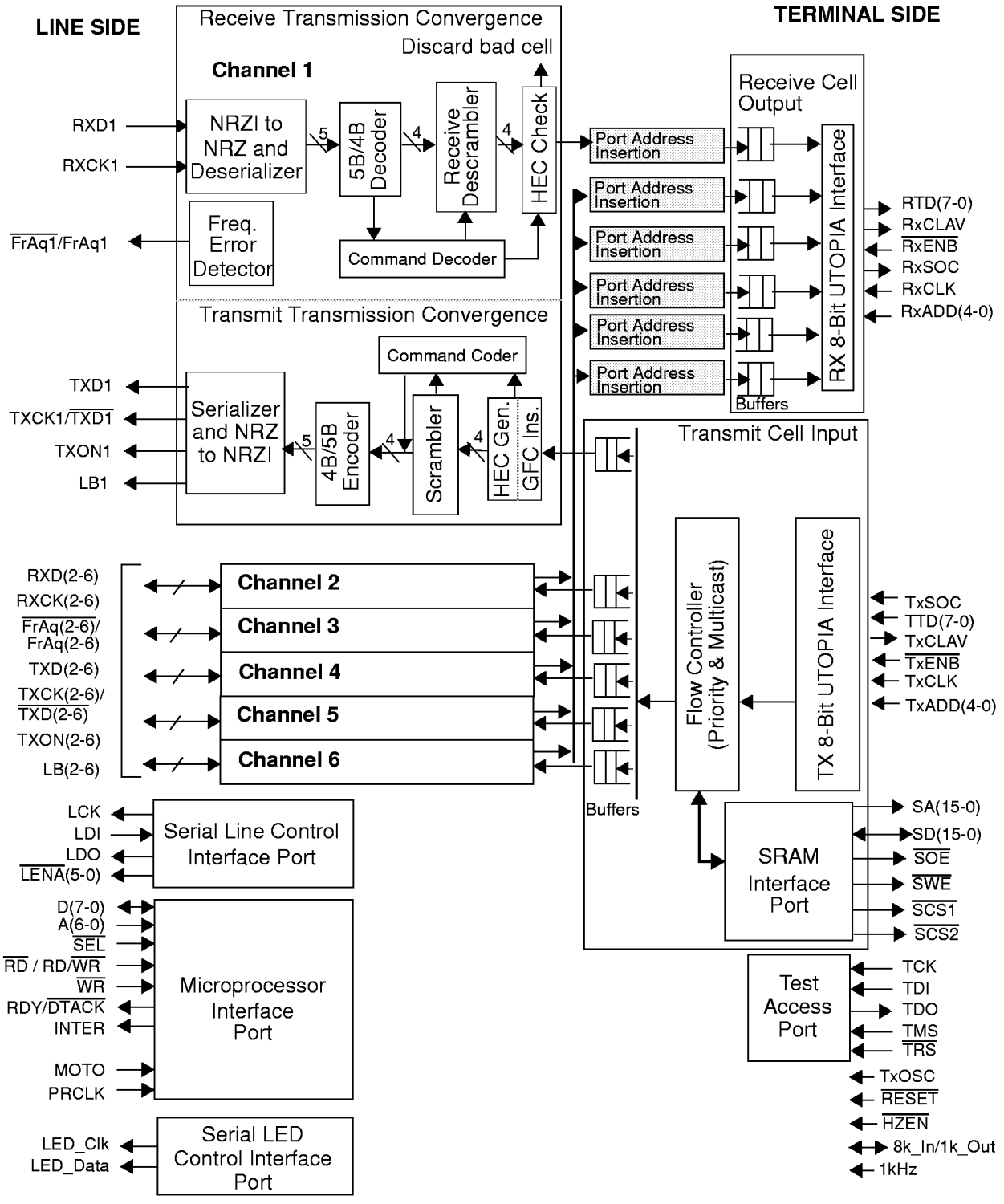
Copies of the following reference documents may be obtained from the issuing organizations, which are listed in the Standards Documentation Sources section:

Physical Interface Specification for 25.6 Mbit/s Over Twisted Pair Cable, af-phy-0040.000 Letter Ballot, ATM Forum Technical Committee, 6/95.

UTOPIA, an ATM-PHY Interface Specification, Level 2 V1.0, af-phy-0039.000, ATM Forum Technical Committee, 6/95.

BISDN User-Network Interface - Physical Layer Specification, ITU-T Recommendation I.432

BLOCK DIAGRAM



Note: The variable n is used throughout this document to represent a channel/line number (n = 1-6).

Figure 1. SALI-25C TXC-07625 Block Diagram

BLOCK DIAGRAM DESCRIPTION

RECEIVE DIRECTION

A block diagram of the SALI-25C is shown in Figure 1. On the line side, the Receive data path for channel n (where n = 1-6) takes in serial data at 32 Mbit/s from the ALI-25T or equivalent line transceiver, converts the data from NRZI format to NRZ format (if enabled), and then deserializes it into a parallel 5-bit symbol. The 5-bit symbols are then decoded into a 4-bit nibble of scrambled data and unscrambled control codes. The control nibbles are sent to the command decoder while the data nibbles are send to the descrambler. The receive descrambler converts the scrambled nibble into data. The data nibbles are converted into bytes and stored in a 3-cell buffer after the cell HEC byte is verified and the port address is inserted, if selected. Data is then extracted from the terminal side receive output by an ATM layer device (such as the TranSwitch CUBIT). Throughout the receive data path, the information contained in the control or command symbol-pair is used by the various functional blocks to maintain proper operation and data flow.

Receive Transmission Convergence

NRZI to NRZ Format Conversion and Deserializer

The serial data input signal RXDn can be sampled on the rising or falling edge of the input clock RXCKn, as determined by the common control bit FALL. If it is in NRZI format, the received data is converted to NRZ format before being deserialized to 5-bit parallel data symbols. The NRZI to NRZ conversion is bypassed if control bit NRZ is set to 1 for receipt of NRZ data input. The 5-bit symbol X (00010) is used for symbol alignment and recognition of sequential symbol-pairs containing commands. The aligned 5-bit data is sent to the 5B/4B decoder block, which decodes it to 4-bit nibbles. The clocking for this section is provided by the line interface transceiver.

Frequency Error Detector

The frequency error detector has as inputs the local oscillator (TxOSC) and the recovered receive clock from the line interface transceiver phase-locked loop (RXCKn). This circuit detects the frequency difference between TxOSC, which is used for transmission, and RXCKn, which is used for reception. When a frequency error is detected, it triggers the FREQEn interrupt, if enabled, and the "frequency acquisition" pin ($\overline{\text{FrAqn}}$/FrAqn) is asserted (low if control bit INVFRAQ = 0, high if INVFRAQ = 1) for at least 72 microseconds (please see the Memory Map and Memory Map Descriptions sections for details of control bits and other register bits). The $\overline{\text{FrAqn}}$/FrAqn pin is used to initialize the transceiver device, such as the TranSwitch ALI-25T. The frequency error detector will detect a frequency deviation of $(1.2 \pm 0.4)\%$ or more. The response time from no transition on the receive clock to assertion of the $\overline{\text{FrAqn}}$/FrAqn output signal is less than 0.2 microseconds. Repeated FREQEn interrupts can be used as an indicator of loss-of-signal from the associated line.

5B/4B Decoder Block

The 5B/4B Decoder block converts the 5-bit symbols to scrambled nibble data according to the following table:

5B Symbol	00000	00001	00010	00011	00100	00101	00110	00111	01000	01001	01010
4B Data	Illegal	Illegal	X	Illegal	Illegal	Illegal	Illegal	0100	Illegal	0001	0010
5B Symbol	01011	01100	01101	01110	01111	10000	10001	10010	10011	10100	10101
4B Data	0011	Illegal	0101	0110	0111	Illegal	Illegal	1000	Illegal	illegal	0000
5B Symbol	10110	10111	11000	11001	11010	11011	11100	11101	11110	11111	
4B Data	Illegal	1100	Illegal	1001	1010	1011	Illegal	1101	1110	1111	

The fifteen 5-bit symbols that have no 4-bit decoded equivalent should not occur, and are classified as "illegal". The symbol that represents X is unique, and is used as the first (marker) symbol of a 2-symbol command. Upon its recognition, the decoder detects that the next symbol will be the second symbol of the command symbol-pair. Of the 17 possible commands (XX, X0,...,XF), only three are defined, as follows:

- XX = Start of cell with scrambler / descrambler initialized
- X4 = Start of cell without scrambler / descrambler initialized
- X8 = 8 kHz timing pulse marker (this command is ignored)
- Xi, where i = 0, 1, 2, 3, 5, 6, 7, 9, A, B, C, D, E, and F, are undefined commands and are ignored without affecting the normal operation of the SALI-25C.

The descrambled data derived from a received illegal 5B code is replaced with the previously descrambled legal code at all times including the idle period. The descrambler continues to run during the received illegal code cycle. The received illegal 5B code also triggers the 5BCODEn interrupt, if enabled.

Repeated 5BCODEn interrupts can be used as an indicator of loss-of-data from the associated line.

Descrambler/Scrambler

The descrambler takes the 4-bit nibbles and descrambles them in exactly the inverse of the manner in which they were scrambled in the transmit side of the SALI-25C. The scrambler and descrambler are each comprised of a 10-bit pseudo-random number generator (PRNG) based on the polynomial $x^{10} + x^7 + 1$. The PRNG logic diagram is shown in Figure 2 below:

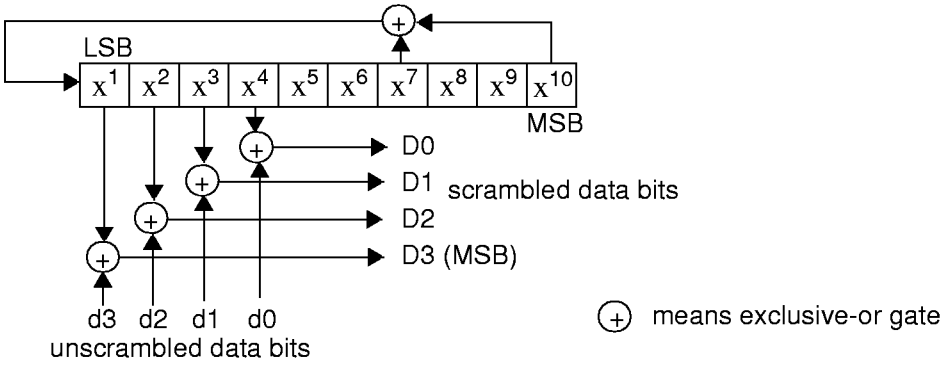


Figure 2. PRNG Logic Diagram

Both the scrambler and descrambler are reset to their initial states when the XX command is detected. The three types of command bytes are not scrambled prior to transmission, so they are not descrambled by the receive descrambler.

The PRNG is clocked 4 times after each nibble regardless of whether the command byte, valid data or idle data is being transmitted. The PRNG is reset to its initial state (3FFH) upon every detection of the XX command, regardless of whether the XX nibbles are byte-aligned. The first nibble that follows is exclusive or-gated with the initial F(Hex) of the scrambler sequence in bits x^4-x^1, unless it is part of a command byte.

Cell Header Error Checking and Bad Cell Discard

After descrambling, the header CRC of each received cell is checked for correctness. This is achieved by calculation of a CRC-8 over the first four bytes of each cell and the modulo-2 addition of a 01010101 sequence (the COSET polynomial), and then comparing the resulting value to the received HEC value (the fifth byte) in the cell. If the HEC check fails, or if fewer than 53 bytes are received, the cell is discarded as a bad cell; otherwise, the cell is sent to the port address insertion block and then stored in the 3-cell buffer to be sent as output on the UTOPIA receive terminal interface. A cell that is discarded due to HEC check failure triggers the corresponding RHECEn interrupt, if enabled, and increments the corresponding 24-bit roll-over discarded bad HEC cell counter. Short cells that are discarded would neither cause an interrupt nor increment the discarded cell counter.

Port Address Insertion

Port address is inserted inband in the cell header if the SALI-25C is in single-PHY UTOPIA mode. The 3 or 4 LSBs of the 5-bit port address in configuration register ADDn(4-0) are inserted in the 4-bit GFC field if control bits RINBAND = 00, in the HEC 7:4 bits if RINBAND = 01, in the VPI 7:5 bits if RINBAND = 10, or in the VPI 4:2 bits if RINBAND = 11, as shown in Figure 3.

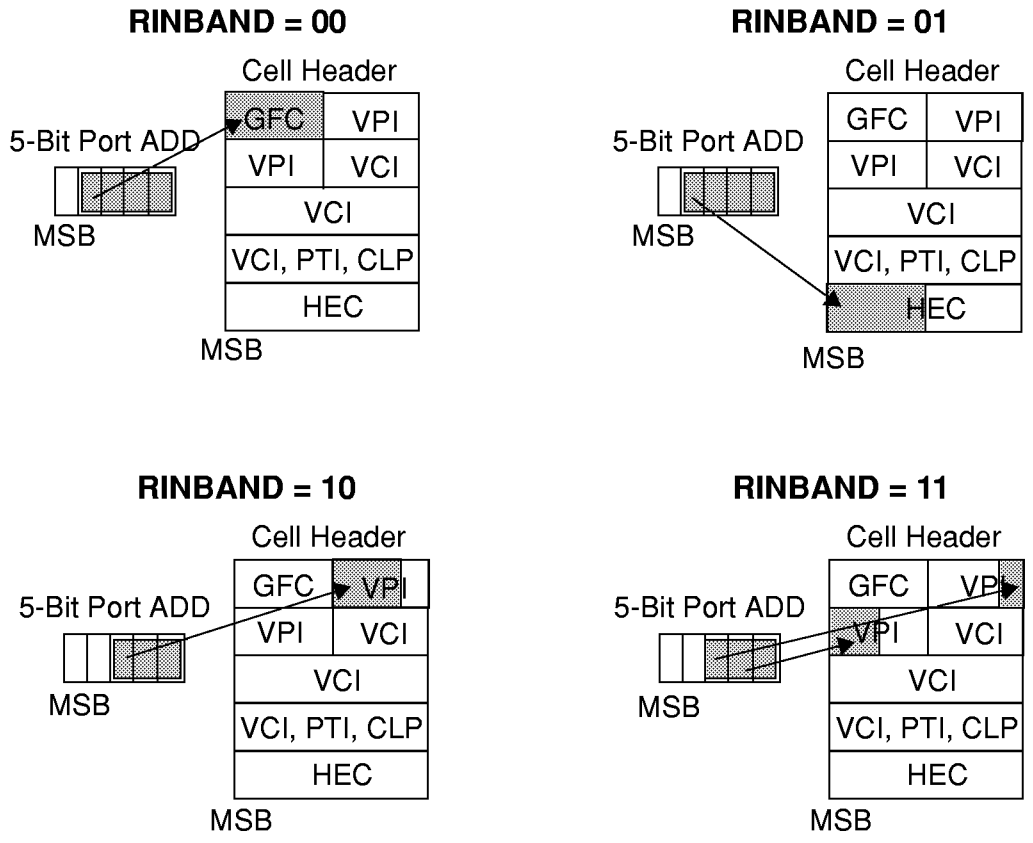


Figure 3. RX Line to UTOPIA Port Address Insertion

Receive Cell Output Block

The Receive Cell Output Block (RCOB) supports a fully ATM Forum-compliant 8-bit single-PHY or multi-PHY UTOPIA interface on the cell input/output terminal side interface, depending on the state of control bit U1. There is a 3-cell FIFO buffer for each line. A receive line buffer full (RBFULn) interrupt, if enabled, is generated to alert the user when the third cell buffer is being filled with a cell having a correct HEC. This will allow the user a minimum of 0.0146 milliseconds to perform flow control and stop the line input before the 3-cell buffer overflows. The RBFULn status is exited when two empty cell spaces become available. When a cell is ready in the buffer, this block coordinates the transfer of the ATM cell to the ATM layer device and performs all the necessary handshaking to transfer the data between the chips. Only cells which have a correct HEC before the port address insertion block, and the correct 53-byte count, are transferred out of the receive interface. There is no HEC regeneration in the receive direction.

In the single-PHY UTOPIA mode, cells are serviced on a first-come, first-served basis. In the multi-PHY UTOPIA mode, cell transfer is controlled by the ATM layer.

TRANSMIT DIRECTION

The ATM terminal passes cells from the UTOPIA interface to the Transmit Cell Input block to be stored in the appropriate channel's cell buffer at its output. A new HEC byte is generated for each cell before scrambling and conversion to symbols by the 4B/5B encoder. The 5-bit symbols are then serialized and converted to NRZI format (if enabled) before they are sent as bit-serial output on the line interface. In addition, flow control and frame synchronization are also supported. Flow control is achieved by setting the GFC nibble to the proper XON/XOFF value before HEC generation, and the 8 kHz frame synchronization symbol is sent out when it is required.

Transmit Cell Input

Fully ATM Forum-compliant 8-bit single-PHY or multi-PHY UTOPIA cell input interfaces are supported. There is a 4-cell buffer at the UTOPIA interface for decoupling the cell input rate from the internal rate.

UTOPIA Interface

The UTOPIA interface can be set to operate in either single- or multi-PHY mode. The UTOPIA interface can work with either single or priority queueing, and unicasting or multicasting. The assertion of the TxCLAV output pin is dependent on the number of queues serviced by the TxCLAV signal and the value of control bit DROPCELL. Further detail is provided below.

The UTOPIA interface keeps track of the received cell byte count. Received short cells are dropped. Received long cells are transmitted with the extra bytes dropped.

Unicast/Multicast for Single-PHY UTOPIA

Both unicast and multicast operations are supported in the single-PHY UTOPIA mode. For unicast operation, control bit MCAST must be set to 0. For multicast, MCAST must be set to 1. The ID of the port selected is carried inband using one of the following three methods:

- Uses inband port ID: TINBAND=010 selects this method. In this method, bits VPI 7:5 are used to compare with the 3 LSBs of the stored port ID in register ADDn, i.e., bits ADDn(2-0), as shown in Figure 4. The cell is directed to the channel with matching ADDn(2-0). An unmatched cell is discarded and the ROTOn alarm is triggered. Multicast and priority queuing are not supported.

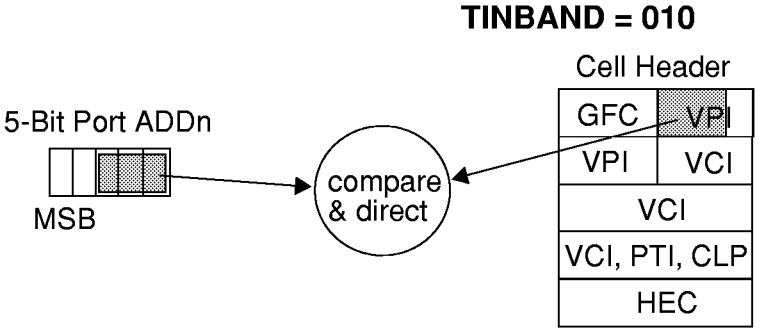


Figure 4. TX Using Inband Port ID

- Uses inband multiport indicator: TINBAND=001, 011 or 100 selects this method. In this method, the ports receiving the cell to be transmitted onto the line are indicated in the multiport indicator, which is a 6-bit port map located in the cell header, as shown in Figure 5. The presence of a 1 in the 6-bit port map indicates that the corresponding port is selected. The 6-bit port map is configured in descending order, with the MSB mapped to port 6. The ports selected for multicasting are indicated only by bits in the 6-bit port map.

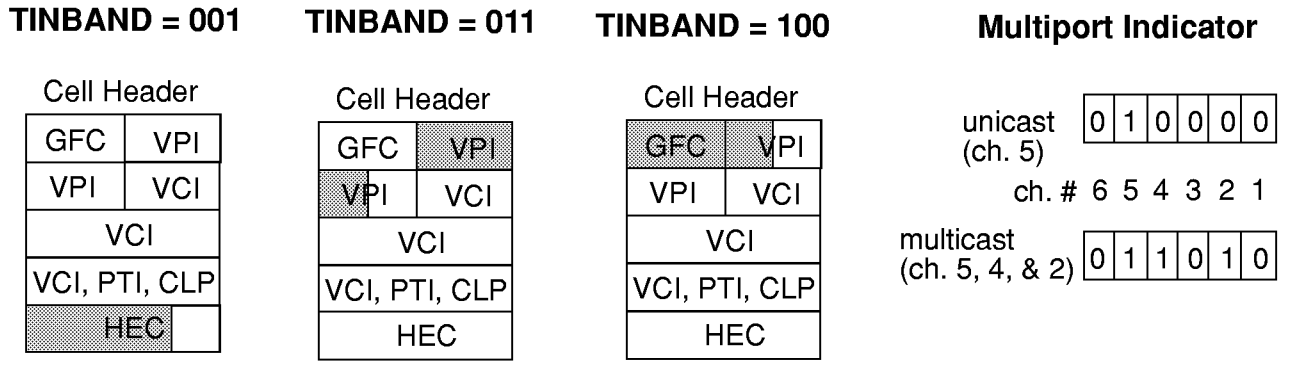


Figure 5. TX Using Inband Multiport Indicator

- Uses inband session indicator: TINBAND=000 selects this method. This method uses 55-byte mode with a 6-bit inband index carried by the MS tag byte that points to an internal multicast indicator, as shown in Figure 6. This method supports 64 active multicast or unicast transmit sessions simultaneously and is intended for use directly with the TranSwitch CUBIT VLSI device.

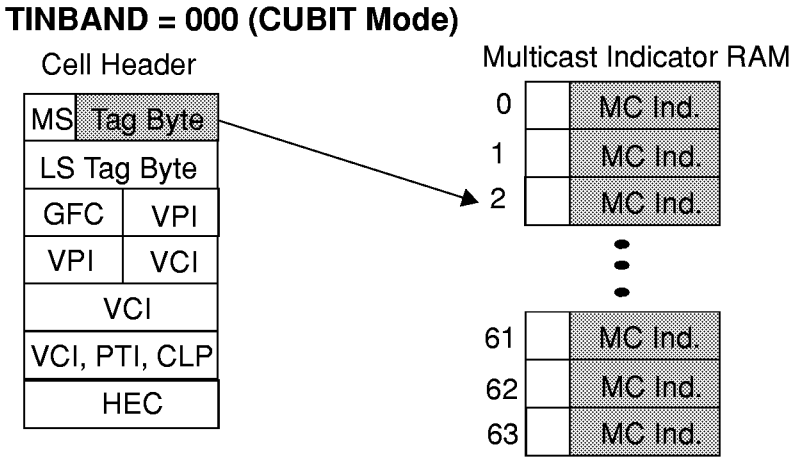


Figure 6. TX Using Inband Session Indicator

Unicast/Multicast for Multi-PHY UTOPIA

Both unicast and multicast operation are supported in the multicast mode. For unicast operation, control bit MCAST must be set to 0, and the port selection is governed only by the input pins TXADD(4-0). The inband multicast indicator is not used. For multicast operation, control bit MCAST must be set to 1, and the port selection is based on both the input pins TXADD(4-0) and the inband multiport indicator, as described above for the single-PHY mode, i.e., via a 6-bit port map indicated by TINBAND = 001, 011 or 100 (TINBAND = 000 or 010 are not supported). Cells admitted must have the TXADD(4-0) inputs matching the port address stored in registers ADDn and also the same port bit set in the inband multiport indicator. Other ports can also be set in the inband multiport indicator. In addition, the port addresses set in the ADDn registers have to be different from one another, i.e., two ports cannot have the same address.

Delay Sensitive (CBR) Traffic Support

Support for CBR traffic is through the use of an external SRAM cell buffer and the queueing of the received cells in pre-determined priority order for transmission onto the line. Setting control bit 4Q=1 allows the user to prioritize up to 4 queues per channel of different priority levels. Priority information is carried in the two bits of the cell header selected by the control bits TINBAND, as shown in Figure 7. For these two priority bits, 00 represents the highest priority and 11 represents the lowest priority. In addition, the user is required to set the minimum number of cell buffer blocks (4 cells per block) used in external SRAM for each priority by specifying registers MINLPij where ij indicates priority 00 to 11. MINLPij can be set to a value from 0 to 14. The number of cell buffer blocks reserved per channel is MINLPij + 1, i.e., if MINLP00 = 0, the external SRAM buffer used for the highest priority per channel is 1 block or 4 cells. Therefore, the range of cell space that can be reserved per channel for any priority is from 4 to 60 cells, in steps of 4, as shown in the table below. This cell buffer setting will provide a guaranteed initial space allocation for cells of the associated priority. In addition, LINKRES must be set to the value LINKRES = 3 x [MINLP00 + MINLP01 + MINLP10 + MINLP11].

4Q = 1, 4K = 0 or 1			
Priority	Register		Cell Space reserved per channel
	Name	Range	
Highest ↓ Lowest	MINLP00	0 - 14	4 - 60
	MINLP01	0 - 14	4 - 60
	MINLP10	0 - 14	4 - 60
	MINLP11	0 - 14	4 - 60
--	LINKRES	0 - 168	16 - 240

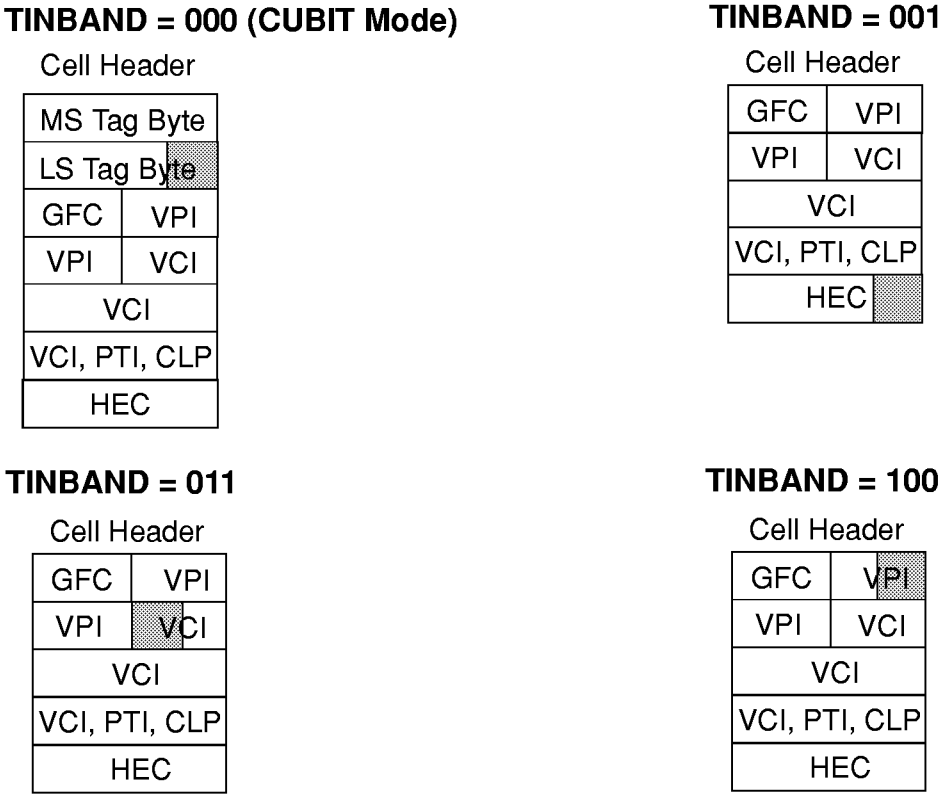


Figure 7. Inband Priority Indicator

If priority queueing is not used (4Q=0), MINLP11 and MINLP10 are used as byte MINLP. The 6 LSBs of MINLP set the minimum cell buffer size for all 6 channel queues. LINKRES should be set to 3 x MINLP in this case. For 4K=0 or 1, MINLP can be set to a value from 0 to 63, corresponding to reserving 1 to 64 blocks (4 to 256 cells) of buffer per channel, as shown in the table below.

4Q = 0, 4K = 0 or 1			
Priority	Register		Cell Space reserved per channel
	Name	Range	
None	MINLP	0 - 63	4 - 256
--	LINKRES	0 - 189	4 - 256

The queue size, once specified, is fixed and can be changed only after chip reset (software or hardware).

If priority queueing is selected (4Q=1), cells in the highest priority non-empty queue are output until the queue is empty, before a cell from the next priority non-empty queue is sent. The last valid byte is repeatedly sent out when all the queues used for this port are empty.

The following table summarizes the use of the TINBAND control bits for inband port address and priority communications:

CONTROL BITS **TINBAND**	**Bits Used to Carry the Multi-port Indicator, Index, or Port Address**	**Bits Used For Priority Indication**
000	6 LSBs of the most significant tag byte as an index to the multi-port indicator	2 LSBs of the least significant tag byte
001	HEC 7:2 is the 6-bit multi-port indicator	HEC 1:0
010**	VPI* 7:5 bits carry the 3 LSBs of the port ID (Multicast and 4-priority queue not allowed)	only single queue allowed
011	VPI* 7:2 is the 6-bit multi-port indicator	VCI 15:14
100	4 GFC bits and VPI* 7:6 contain the multi-port indicator	VPI* 5:4
others	not used	not used

* The VPI bits (2, 3, 4 or 6 bits) and the VCI bits used are reset to zeros before being sent as output to the line. The GFC bits are always replaced with 0000 if XOFFn=0, or the 4-bit value of the XCODE field in register 03H if XOFFn = 1.
** TINBAND = 010 should only be used for unicast and single-PHY.

The different UTOPIA interface modes and features that are available if TINBAND is set to 000, 001, 011 or 100 are summarized below:

Mode				Control Bits				
Ext. SRAM	**UTOPIA**	**Cast**	**Queues**	**XRAM**	**U1**	**MCAST**	**4Q**	**DROPCELL**
No	Single-PHY	Uni	1	0	1	0	0	0/1
		Multi	1	0	1	1	0	0/1
	Multi-PHY	Uni	1	0	0	0	0	0
		Multi	1	0	0	1	0	0
Yes	Multi-PHY	Uni	1	1	0	0	0	0
			4	1	0	0	1	0/1
		Multi	1	1	0	1	0	0
			4	1	0	1	1	0/1
	Single-PHY	Uni	1	1	1	0	0	0/1
			4	1	1	0	1	0/1
		Multi	1	1	1	1	0	0
			4	1	1	1	1	0/1

If TINBAND is set to 010, multicast and priority queueing are not supported and only the following modes are supported:

Mode				Control Bits				
Ext. SRAM	**UTOPIA**	**Cast**	**Queues**	**XRAM**	**U1**	**MCAST**	**4Q**	**DROPCELL**
No	Single-PHY	Uni	1	0	1	0	0	0/1
Yes	Single-PHY	Uni	1	1	1	0	0	0/1

Transmit Cell Buffers and SRAM

There are six internal 2-cell buffers in the Transmit Cell Input block, which are used to send output cells to the lines at about 3.2 MByte/s per line. Each of the 2-cell buffers accepts cells either from the 4-cell UTOPIA buffer or from the external cell buffers (if these are used). Priority queueing is not supported if external cell buffers are not used, and the control bit 4Q is ignored.

Control bit XRAM must be set to 1 to indicate that external SRAM is used in the transmit path for all six lines. Control bit 4K must be set to 1 to indicate that two SRAMs are used and 4K must be set to 0 to indicate that one SRAM is used. In this mode the transmitted cell is first stored in the external SRAM before it is transferred to the internal cell buffers. Each cell is stored in a 32-word page. The write and read operations to the SRAM are controlled by linked lists. For priority queueing operation there are 25 linked lists, composed of 4 linked lists per line and a free buffer linked list. For single queue operation there are 7 linked lists, composed of 1 linked list per line and a free buffer linked list. The free buffer linked list contains all the cell spaces that are freed up after a stored cell is read out.

If only one SRAM device is used it should be a 64k x 16 SRAM. The $\overline{SCS1}$ output should be tied directly to the SRAM's Chip enable pin $\overline{CE}$ and $\overline{SCS2}$ is not used, as shown in Figure 8 below:

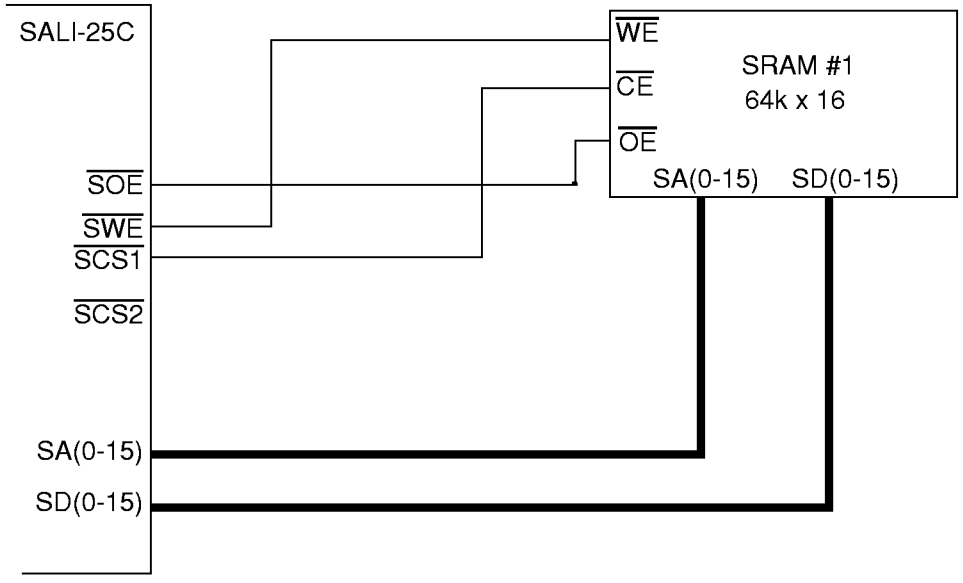


Figure 8. Interfacing with one 64k x 16 SRAM

If two SRAM devices are used, they should be 128k x 8 SRAMs. The $\overline{SCS1}$ output is used as address pin A16 after being latched by an Integrated Device Technology, Inc. (Tel. 408-727-6116) 74FCT573 or equivalent device. The $\overline{SCS2}$ output is not used, and the two SRAM chip enable pins $\overline{CE}$ should be grounded. The interfacing is shown in Figure 9 below. This dual SRAM configuration is preferred to the single SRAM configuration.

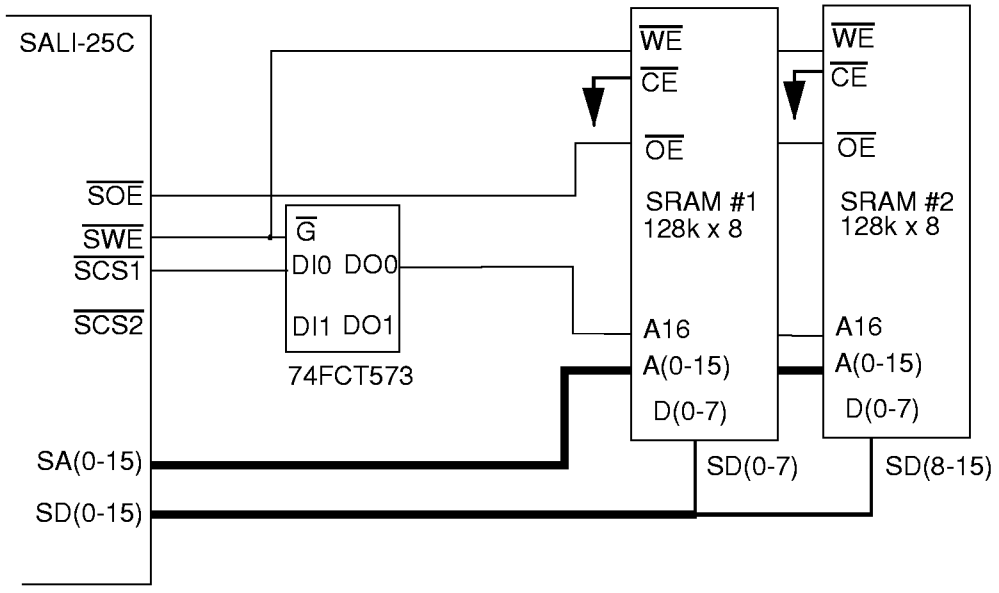


Figure 9. Interfacing with two 128k x 8 SRAMs

Suitable SRAM devices are available from several vendors. The devices selected must satisfy the timing requirements shown in Figure 21. Inquiries related to 64k x 16 devices may be directed to vendors of Micron, NEC and Samsung products. Inquiries related to 128k x 8 devices may be directed to vendors of IDT, Micron, Motorola, NEC, Samsung and Toshiba products.

Cell Inlet Burst Rate

The cell inlet burst rate depends on whether there is external SRAM and the number of channels to which the incoming cell is multicasted. If external SRAM is not used (register bit XRAM=0) the UTOPIA interface stops transferring cells if there are a total of 2 cells destined to any one port in the combined 2-cell transmit buffer and the 4-cell UTOPIA FIFO.

If external SRAM is used (XRAM=1), input cells are first buffered in the 4-cell UTOPIA FIFO and then transferred to the external SRAM. The difference between the cell rate coming from the UTOPIA interface and the rate at which cells are written to the external SRAM will fill the 4-cell UTOPIA FIFO; this will stop the UTOPIA interface and limit the burst size. The multi-PHY UTOPIA interface stops if an input cell is destined for a full queue in SRAM or if the 4-cell UTOPIA FIFO is full. The single-PHY UTOPIA interface stops if any queue in SRAM is full or if the 4-cell UTOPIA FIFO is full.The following table shows some representative cell burst sizes for different UTOPIA speeds:

# Ch. Multicasted	UTOPIA Rate					
	16 MHz	20 MHz	25 MHz	29 MHz	32 MHz	33 MHz
1	Burst continuously until the external buffer is full				22 cells	17 cells
2	22 cells	8 cells	6 cells	5 cells	5 cells	5 cells
3	6 cells	5 cells	5 cells	4 cells	4 cells	4 cells
4	5 cells	4 cells	4 cells	4 cells	4 cells	4 cells
5	4 cells	4 cells	4 cells	4 cells	4 cells	4 cells
6	4 cells	4 cells	4 cells	4 cells	4 cells	4 cells

TxCLAV Generation

The generation of the TxCLAV output signal depends on the states of the control bits DROPCELL, XRAM, U1, MCAST and on the various cell buffer or queue conditions. Cells received from the UTOPIA interface can be dropped, and the DROPCn interrupt is triggered (if enabled) when DROPCELL is set to 1 and there is no line buffer (internal or external) available for cell transfer from the UTOPIA buffer.

Effect of TXENn on Cell Buffers

In order to provide maximum UTOPIA buffer efficiency in all configurations, the incoming cell is only written into the 4-cell UTOPIA cell buffer if at least one of the designated channels is enabled, e.g., if a cell is multicasted to channels 1 and 3, the cell will be written to the cell buffer only if one or both of TXEN1 and TXEN3 are set to 1. The ROTO1 interrupt would be triggered if TXEN1=0 and the ROTO3 interrupt would be triggered if TXEN3=0.

In addition, TXENn has to be 1 in all configurations before a cell is transferred from the 4-cell UTOPIA cell buffer to the channel n internal buffer (if XRAM=0) or to the external channel n SRAM buffer (if XRAM=1).

Transmit Transmission Convergence

The blocks comprising the Transmit Transmission Convergence function accept byte data from the cell buffer, calculate and add the CRC header, scramble the 53-byte ATM data, add the proper command codes, perform 4B/5B encoding, serialize the symbols, and convert the NRZ serial data to NRZI (if NRZ=0) format before sending it to the line interface for transmission. If the line is idle without any cell pending in the buffer, the last data byte of the last cell is sent as output repeatedly until a new cell arrives.

HEC Generation

The HEC generator calculates and overwrites the HEC byte of a cell received in the 53-byte format. According to standard, the HEC is modified before transmission by the addition, modulo-2, of a 01010101 sequence (the COSET polynomial). The leading "0" bit is added to the first outgoing HEC bit, and the trailing "1" bit is added to the final outgoing HEC bit. On reception, the same 01010101 sequence is added to the received HEC bits before checking. The double addition of the 01010101 pattern, first at the generator, then at the decoder, has no net effect on the HEC process. The purpose of the pattern addition is to increase the probability of state transitions between adjacent bits in the HEC byte.

Cell Scrambling

The Transmit Scrambler accepts 4-bit nibbles from the HEC generator block and converts them into 4 bits of pseudo-random data. All 53 bytes in an ATM cell are scrambled.

Command Coder

The command coder generates three types of command codes:

- XX, a symbol-pair to indicate start-of-cell with scrambler reset. This command is sent before the first byte of an ATM cell.
- X4, a symbol-pair to indicate start-of-cell without scrambler reset. This command is sent before the first byte of an ATM cell.
- X8, a symbol-pair to indicate an 8 kHz synchronization event. This command is sent immediately after receiving the 8 kHz pulse on a symbol-pair boundary.

The scrambler reset command is sent out every 125 microseconds, or on the first cell transmitted after an idle period of more than 125 microseconds. The SALI-25C uses either an internally generated 8 kHz clock (derived from TxOSC/4000) or an external 8 kHz clock to insert the scrambler reset command. There will not be any command code sent out during an extended idle period. The last byte of the last cell sent out is sent repeatedly during the idle period.

The 8 kHz clock can be sourced externally via the 8k_In/1k_Out pin or generated internally, by setting the control bit EXT8K to 1 or 0, respectively. The 8 kHz marker output on the Tx lines is enabled by setting the 8KEN control bit to 1.

Note: If control bit EXT8K is set to 1 (i.e., the external 8 kHz clock option is selected) and no external 8 kHz clock is provided via the 8k_In/1k_Out pin, then no scrambler reset command will be generated, and synchronization problems may occur.

4B/5B Encoder

The 4B/5B Encoder block takes the input nibbles from the scrambler and converts them into 5-bit symbols. The most important reason for this encoding is to guarantee sufficient data transitions for reliable clock recovery. The second reason is to help identify uniquely the command symbols generated by the Transmit Transmission Convergence block. These nibbles are encoded into non-data 5-bit symbols. This allows the receiver to recognize when a symbol-pair (i.e., the current and the previous 5-bit symbols) are control information and are not a part of the ATM cell itself.

Serializer and NRZ to NRZI Formatter

The serializer takes the 5-bit symbols from the 4B/5B Encoder and converts them into serial data. The serial data is sent out in NRZ format or further converted into NRZI format before transmission. The transmit clock frequency of 32 MHz is determined by the clock provided at the TxOSC input pin. TXDn is clocked out on the falling edge of the corresponding TXCKn clock that is derived from TxOSC input.

Transmit Line Output Control

Control bit TXENn provides individual transmit line output control. In all situations, setting TXENn to 0 holds the TXDn pin low and the TXCKn pin low if control bit NTDAT is set to 0, and holds the TXDn pin low and the $\overline{\text{TXDn}}$ pin high if NTDAT is set to 1. This function is useful in stopping the individual line transmitter without setting the transmitter to the standby (TXONn de-asserted) mode. If TXENn is set to 0 during operation, the corresponding buffer for that line will be flushed.

Flow Control

A simple XON/XOFF flow control mechanism is implemented to facilitate flow control on the line. An XOFFn bit is provided for each channel, to set the GFC nibble being sent out on the transmit line n. XOFFn = 1 sets the GFC nibble to use the value stored in XCODE, and 0 sets it to 0000. The GFC nibble is always replaced just before HEC calculation is performed. The GFC nibble can be used with the RBFULn alarm to regulate the traffic flow from the line.

MICROPROCESSOR INTERFACE

The microprocessor interface of the SALI-25C is designed to operate with a microprocessor clock input PRCLK (8.25-28 MHz), a 7-bit address input bus A(6-0), and a bidirectional 8-bit data bus D(7-0). It can be configured, by setting input pin MOTO, to be compatible with either Motorola or Intel type microprocessors.

Interrupt

The microprocessor interrupt pin INTER may be asserted on occurrence of any one or more of the following alarms or events:

- 6 alarm conditions each per port (DROPCn, ROTOn, 5BCODEn, RBFULn, RHECEn and FREQEn)
- 6 common port events (CHERRn).

There are three register bits associated with each of these events that may be enabled to cause an interrupt: the interrupt mask bit (read/write), the status bit (read-only), and the event bit (read-only, latched to 1 when set). Each event bit can be enabled to cause an interrupt by setting the corresponding interrupt mask bit to 0. The status bit is pulsed or set to 1 during the occurrence of the alarm condition and is set to 0 at other times. The pulsed status bits (DROCPn and ROTOn) are only used to set the corresponding event bits; they are not to be monitored by the user. The status bits (5BCODEn, RHECEn, RBFULn, and FREQEn) that are set on a condition can be used to monitor on-going conditions. The setting of the event bit is user-selected to be positive edge or negative edge triggered by the corresponding status bit. The event bits can only be cleared on read by the microprocessor. The relationships of the status and event indicator bits to the alarm condition are shown in Figure 10 below:

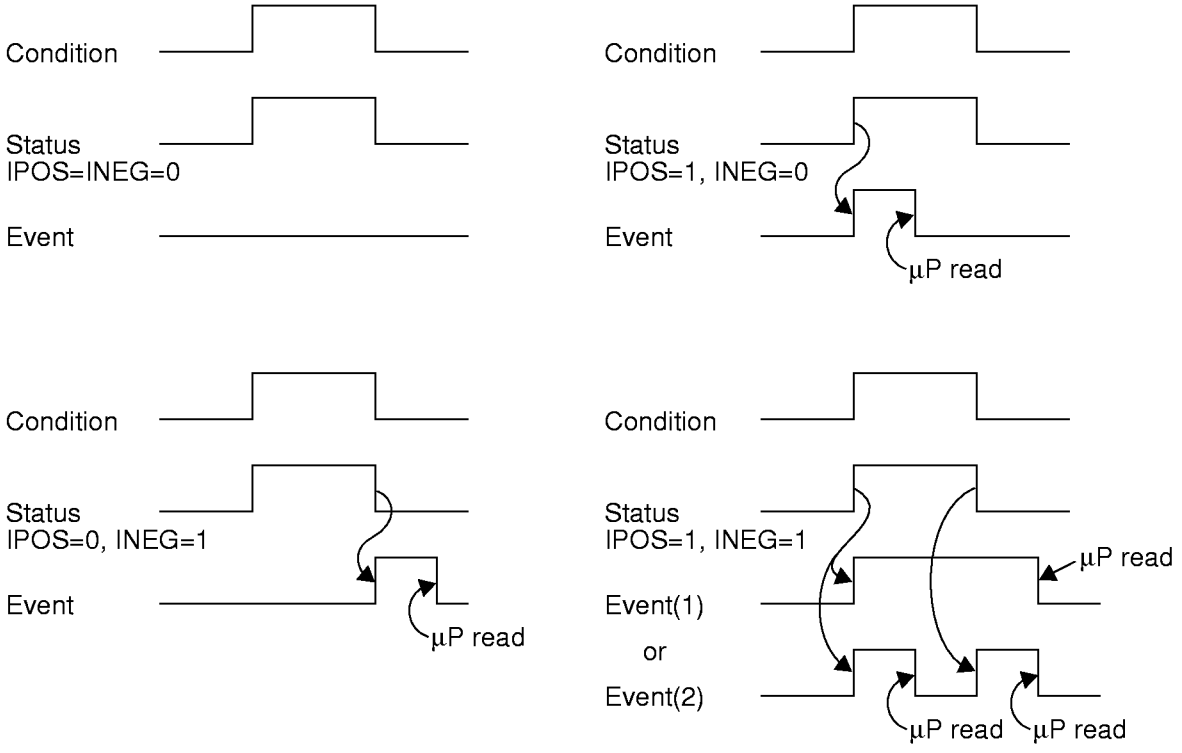


Figure 10. Relationships of the Status and Event Indicator Bits to the Alarm Condition

There is a common channel event polling register at address 30H (read-only). It contains separate single bits for each channel. Each of these bits is set to 1 while any associated event is latched to 1. The common channel register cannot be enabled to cause an interrupt, but may be used in alarm polling management schemes.

Cell Counters

There are three 24-bit roll-over counters for each port: a discarded cell counter, a received cell counter, and a transmitted cell counter. The discarded cell counter counts all the received cells that are discarded due to invalid HEC. The received cell counter counts all the full length cells (53 bytes) that have valid HEC. The transmitted cell counter counts all the cells that are completely sent as output, i.e., when the 53rd byte of the cell is transferred out of the line buffer. If any channel (n) is disabled by setting TXENn=0, the corresponding transmitted cell counter could be high by 1.

On power-up, these counters are in random states and have to be initialized to 000000H by writing to the counter locations through the microprocessor. Software reset would not change the counter values. Writing to a counter is achieved by loading the 24-bit count to registers 5DH-5FH first, and then writing register 5CH with a 0 in control bit CRW and the desired counter address in CADD(4-0). Reading is achieved by first writing register 5CH with a 1 in CRW and the desired counter address in CADD(4-0), and then reading the 24-bit count from the registers 5DH-5FH.

Multicast Indicators

There are 64 internal RAM addresses used to support up to 64 different multicast sessions when TINBAND is set to 000 for working with a CUBIT device. **These registers have to be configured by writing to the RAM addresses. The read and write operations of these registers are the same as described above for the cell counters except that these RAM locations can only be verified by reading the location twice, immediately after it has been written, and disregarding the result of the first read operation.**

EXTERNAL DEVICE CONTROLS

Serial Line Control Interface Port

The 9-pin Serial Line Control Interface Port is composed of six serial line enable output pins, a clock output pin, and data input and output pins. The six serial line enable pins allow control and communications to six external line transceiver devices through the registers in the SALI-25C.

To write to an external device, the 16-bit data word is first written into line data word LD(15-0) in registers 15H and 16H. Then a 0 is written into control bit LRW (register 11H, bit 7) together with the 15 line address bits LRA(14-0) in registers 11H and 12H. Upon writing the line number LN(2-0) to register 10H, the $\overline{\text{LENAm}}$ pin (m is set by the line number LN(2-0) of register 10H) is first asserted low and then the 32 bits (in the order of LRW, LRA14, LRA13, ..., LRA0, LD15, ..., LD0) are output on pin LDO on the falling edge of LCK. The $\overline{\text{LENAm}}$ pin is deasserted after the output of the 32nd bit.

To read from an external device, a 1 is written into control bit LRW (register 11H, bit 7) together with the 15 line address bits LRA(14-0) in registers 11H and 12H. Upon writing the line number LN(2-0) to register 10H, the $\overline{\text{LENAm}}$ pin (m is set by the line number LN(2-0) of register 10H) is first asserted low and then the 16 bits (in the order of LRW, LRA14, LRA13, ..., LRA0) are output on pin LDO on the falling edge of LCK. Input data bits LS15 to LS0 are latched on the rising edge of the 17th to 32nd LCK clock pulses after $\overline{\text{LENAm}}$ is asserted. The $\overline{\text{LENAm}}$ pin is deasserted after the output of the 32nd LCK clock. Input line data word LS(15-0) in registers 13H and 14H can be read once the line status bit LSTATUS (register 17H, bit 0) is set to 0, indicating the completion of the read operation.

Transmitter Control

Six output pins, TXONn, are provided to turn on and off individual transmitters in external line transceiver devices. Each of these pins can be forced low by setting control bit FTOFFn to 1. Control bit INVTXO inverts the output polarity of all these TXONn pins when it is set to 1. FTOFFn = 1 also forces the TXCKn and TXDn pins to low.

Loopback Control

Six output pins, LBn, are provided to set external line transceivers into their Loopback mode. These pins can be set to low by setting control bit FLBn to 0 or to high by setting FLBn to 1.

Serial LED Control Interface Port

The two output pins of the Serial LED Interface Port, LED_Clk and LED_Data, are provided to control six LED drivers through two external shift registers such as those contained in 74F164 devices, as shown in Figure 11. A burst of 16 clocks and data is output on the LED_Clk and LED_Data pins once every millisecond, as shown in Figure 22. The clocks on LED_Clk are used to shift the data on LED_Data out to the Qn outputs of the external shift registers. The LED_Clk frequency, 2.06 MHz to 7.00 MHz, is derived from the microprocessor clock PRCLK. LED_Data, which is a serial signal of 12 data bits and 4 zeros, is output on the falling edge of the LED_Clk.

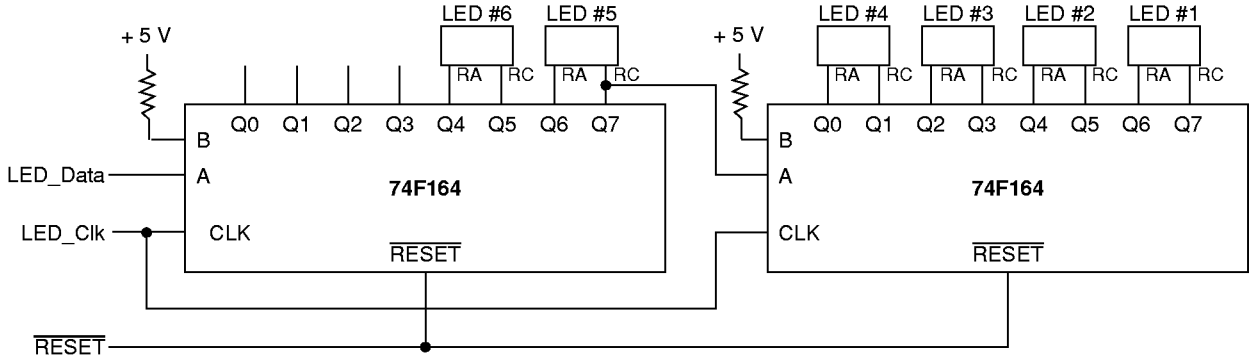


Figure 11. LED Drivers Circuit

The 12 data bits are arranged as six sets of RA and RC bits for the 6 LEDs. Each pair of RA and RC bits is set by 3 control bits LEDnC(2-0), where n indicates the line number, as shown in the table below:

LEDnC(2-0)	RA	RC	Condition and LED Color
000 (default)	0	1	Received or transmitted a cell on the port line. Port will output this data for a minimum 50 ms (green).
	0	0	No Tx or Rx cell (LED off).
001	0	1	Set by microprocessor (green).
010	1	0	Set by microprocessor (red).
011	RA = D & RC = $\overline{D}$ oscillating at 1 kHz		Set by microprocessor (yellow).
111	RA = D & RC = $\overline{D}$ oscillating at 1 kHz and turned on/off at 3 Hz		Set by microprocessor (yellow, flashing at 3 Hz).
other	0	0	Set by microprocessor (LED off).

The default setting for each port is LEDnC(2-0) = 000. In this setting the outputs of RA and RC are dependent on the cell traffic on the port. Every cell received or transmitted will trigger a retriggerable 50 ± 1 milliseconds[1] period where RA is set to 0 and RC is set to 1, which is latched in the 74F164 to drive the LED to green. Both RA and RC are reset to 0s if there is no cell traffic for 50 milliseconds.

Other RA and RC outputs are directly controlled by the microprocessor. Setting LEDnC(2-0) = 011 makes RA the inverse of RC, and both bits invert once every 1 millisecond. Inverting the opposite values of RA and RC at 1 millisecond intervals turns on the LED to oscillating green and red to generate yellow. LEDnC(2-0) = 111 is LEDnC(2-0) = 011 gated at 3 ± 0.05 Hz[1], which is yellow flashing at 3 ± 0.05 Hz[1].

Note 1: The period is based on the actual input frequency on pin 105 (1 kHz).

INTERFACING WITH CUBIT AND ALI-25T

Note: This subsection was written for an earlier Edition of the Data Sheet. The ALI-25T device has since been discontinued by our supplier and the CUBIT device is not now recommended for use in new designs. However, similar functionality may be implemented by using another 25 Mbit/s transceiver, such as the six-port Novacom NOV25PMD6, and the CUBIT-Pro (TXC-05802B) successor to the CUBIT. Please refer to the documentation for these devices (see Web sites www.novacom.com and www.transwitch.com).

The SALI-25C can be interfaced to six ALI-25T "B" version transceiver devices (part number TXC-07225-BCPL) with the interconnection and memory configurations shown in Figure 12 and Table 1.

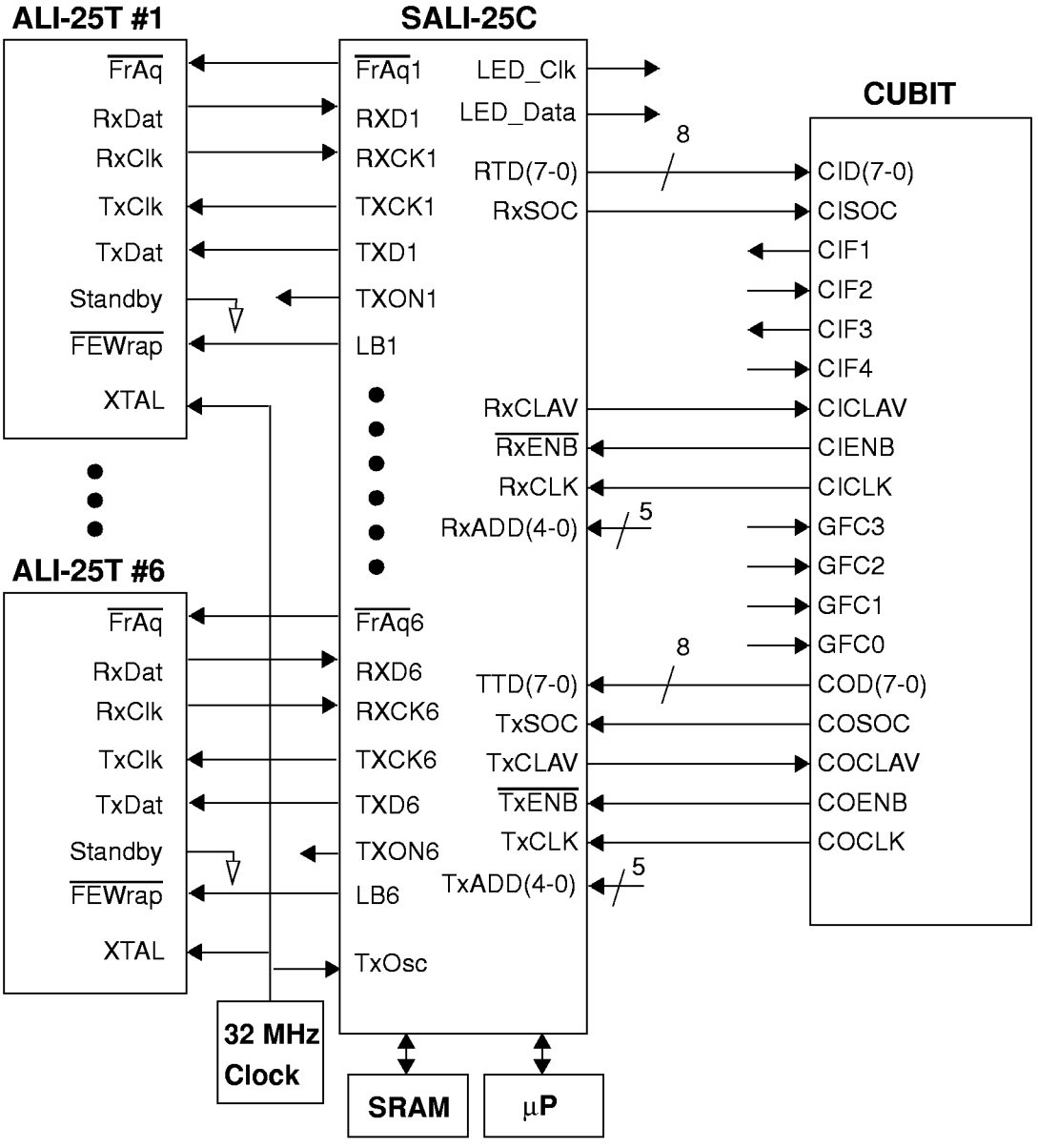


Figure 12. Interconnection for SALI-25C, ALI-25T and CUBIT

When interfacing to a CUBIT device (Figure 12), the CUBIT should be set to NNI mode and the SALI-25C should be set to use external SRAM (control bit XRAM set to 1) and single-PHY UTOPIA (control bits set to U1 = 1, RINBAND = 00, TINBAND = 000). The input signals on the TXADD(4-0) and RXADD(4-0) pins are ignored. There are 53 bytes/cell transferred from the SALI-25C to the CUBIT, and 55 bytes/cell transferred from the CUBIT to the SALI-25C, over the UTOPIA interface. The two extra bytes sent from the CUBIT are tag bytes. The six LSBs of the MS (first) tag byte carry an index, which is used by the SALI-25C to fetch the multi-port indicator. The priority queue code is carried in the two LSBs of the LS (second) tag byte. The SALI-25C examines the tag bytes to determine which ports and queue codes are used. The tag bytes are discarded after processing.

Table 1: SALI-25C Memory Configuration for Interfacing with CUBIT and ALI-25T

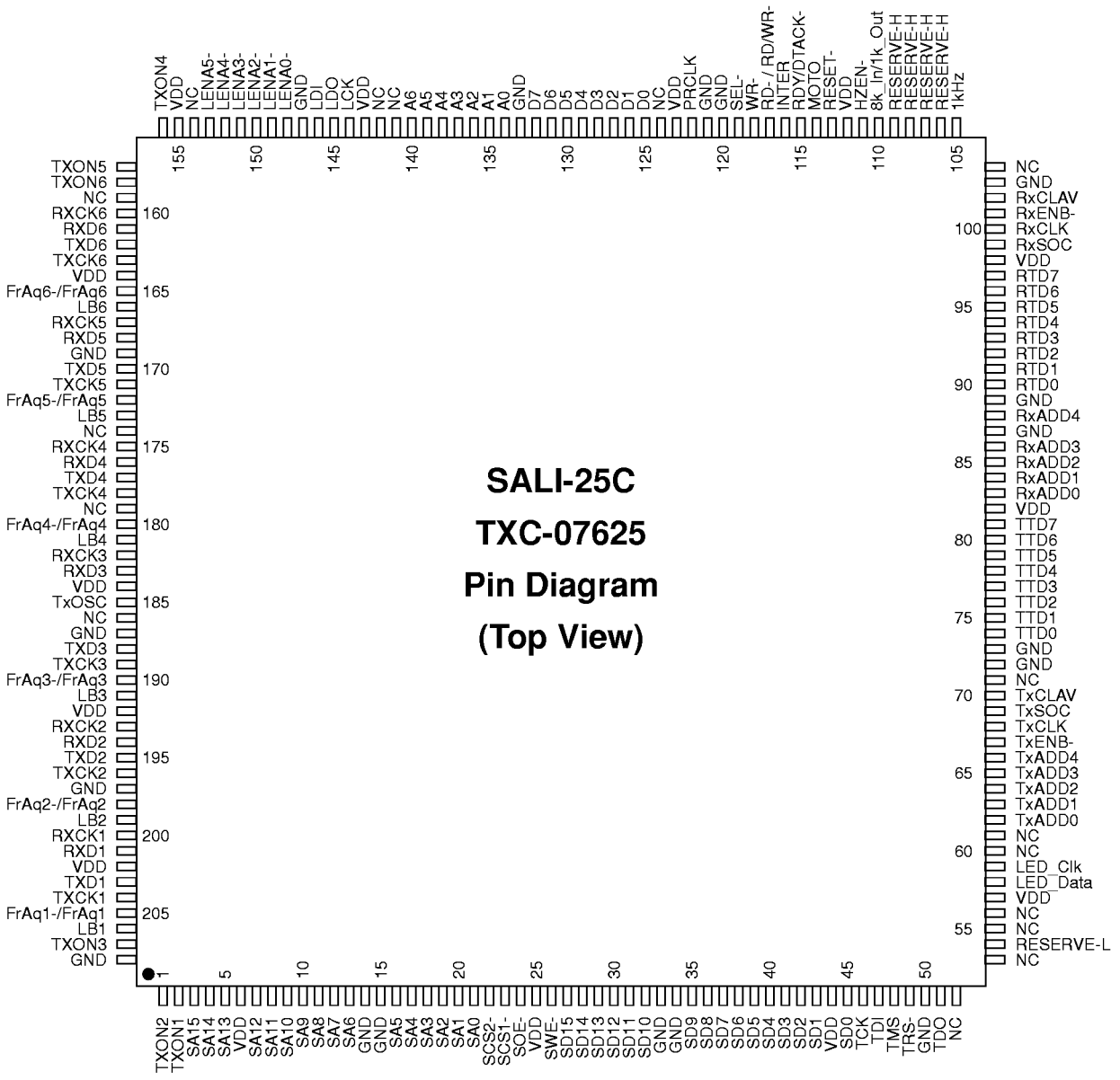
Address (Hex)	Set-up (Hex)	Description
00	F4	not Software Reset
01	F8	set-up ALI-25T to start frequency acquisition
--	--	wait 50 ms
01	F0	use SRAM, single-PHY UTOPIA, multicast, priority queues
02	80	set to use positive edge for event trigger
03	8F	set to output 8K timing mark with internal clock and XCODE is FH.
0A	00	use 1 SRAM & set RINBAND = TINBAND = 0
0B	00	test pattern set to all 0
0C	1E	LINKRES = 30
0D	12	minimum cell buffer size for the lowest priority (11) is 8, for priority 10 is 12
0E	34	minimum cell buffer size for priority 01 is 16, for priority 00 (highest) is 20
0F	00	set to 0
10-17	00	no action needed, reset to 0s
18	00	set all TXONn pins to low, keep ALI-25Ts power up
19	3F	set all LBn pins to high, disable loopback of ALI-25Ts
1A-1C	00	default state, LED's turn green on RX and TX cells on the port line
5D-5F	00	counter value of 000000
5C	01	write to counter 1 (Discarded Cell Counter Channel #6)
5C	02	write to counter 2 (Discarded Cell Counter Channel #5)
		continue incrementing data field for address 5C until 12(hex)
5C	12	write to counter 18 (Transmit Cell Counter Channel #1)
The following sequences should be used when accessing the Multicast Indicator RAM. Write data and read data back (incorrect data) once after SALI-25C is first powered up.		
5B	00	Write data 00 hex to Multi-Port Data Register
5A	00	Write Index Address to Multi-Port Index Register
59	00	Initiates a Write of Data in register 5B to Multi-Port Address pointed by register 5A

Address (Hex)	Set-up (Hex)	Description
5A	00	Write Index Address to Multi-Port Index Register
59	80	Initiate a Read from this address
5B		Read the data from the read cycle performed above (incorrect data)
All subsequent writes and data verification reads to and from the Multi-Port RAM are as follows: This sequence writes 05 hex to address 00 hex and verifies it by reading it twice. This sequence should be used as a guide to access all locations in Multi-Port RAM after the above sequence is performed.		
5B	05	Write Data 05 hex to Multi-Port Data Register
5A	00	Write Index Address to Multi-Port Index Register
59	00	Initiates a Write of data in register 5B to Multi-Port Address pointed by register 5A
5A	00	Write Index Address to Multi-Port Index Register
59	80	Initiate a Read from this address
5B		Read the data from the read cycle performed above (incorrect data)
5A	00	Write Index Address to Multi-Port Index Register
59	80	Initiate a Read from this address
5B		Read the data again from the read cycle performed above (correct data)
End of Multi-Port RAM sequence.		
04^2	C6	turn on channel 6 with ID = 6
05^2	C5	turn on channel 5 with ID = 5
06^2	C4	turn on channel 4 with ID = 4
07^2	C3	turn on channel 3 with ID = 3
08^2	C2	turn on channel 2 with ID = 2
09^2	C1	turn on channel 1 with ID = 1
00^2	91	Software Reset
00^2	F4	not Software Reset

Notes:

1. The multicast indicator location content can only be verified by reading the location twice, immediately after writing to the location, and disregarding the incorrect result of the first read operation.
2. These registers should be programmed last.

PIN DIAGRAM



Note: Active low (inverted) or active-on-falling-edge signals are indicated by '-' at end of symbol (e.g., SOE- is equivalent to $\overline{\text{SOE}}$).

Figure 13. SALI-25C TXC-07625 Pin Diagram

PIN DESCRIPTIONS

The SALI-25C is packaged as a 208-pin plastic quad flat package device, as shown in Figures 13 and 29. The No Connect pins are reserved for possible use to provide new features in future versions of the device. They are not to be connected, in order to assure backwards-compatibility of the new version in existing application designs. Every output pin is tri-stateable. The variable n identifies one of the six channels in the device, and represents values from 1 to 6.

POWER SUPPLY AND GROUND

Symbol	Pin No.	I/O/P*	Type	Name/Function
VDD	6, 25, 44, 57, 82, 98, 112, 123, 143, 155, 164, 184, 192, 202	P		**V_{DD}:** +3.3 volt supply, ±5%.
GND	14, 15, 33, 34, 50, 72, 73, 87, 89, 103, 120, 121, 133, 147, 169, 187, 197, 208	P		**Ground:** 0 volt reference.
NC	52, 53, 55, 56, 60, 61, 71, 104, 124, 141, 142, 154, 159, 174, 179, 186			**No Connect:** NC pins are not to be connected, not even to another NC pin, but must be left floating. Connection of NC pins may impair performance or cause damage to the device. Some NC pins may be assigned functions in future upgrades of the device. Backwards compatibility of the upgraded device in existing applications may rely upon these pins having been left floating.

*Note: I = Input; O = Output; P = Power; T= Tri-state capability.

LINE INPUT

Symbol	Pin No.	I/O/P	Type*	Name/Function
RXDn (n = 1-6)	201, 194, 183, 176, 168, 161	I	TTL	**Receive Line Data Input for Ch. n:** Line input bit-serial data at 32 MHz for channels 1 to 6. RXDn is clocked in on the falling/rising edge of RXCKn, as determined by control bit FALL.
RXCKn (n = 1-6)	200, 193, 182, 175, 167, 160	I	Schmitt Trigger	**Receive Line Clock in for Ch. n:** Line input clock at 32 MHz.
$\overline{\text{FrAqn}}$/ FrAqn (n = 1-6)	205, 198, 190, 180, 172, 165	O(T)	CMOS 2mA	**Frequency Acquisition for Ch. n:** Pulses low for at least 72 µs if RXCKn is detected to be out of sync. with TxOSC. Inverted if INVFRAQ=1.

* See Input, Output and I/O Parameters section for Type definitions.

LINE OUTPUT

Symbol	Pin No.	I/O/P	Type	Name/Function
TXDn (n = 1-6)	203, 195, 188, 177, 170, 162	O(T)	CMOS 4mA	**Transmit Line Data Out for Ch. n:** Line output bit-serial data clocked out on the falling edge of TXCKn.
TXCKn/ $\overline{\text{TXDn}}$ (n = 1-6)	204, 196, 189, 178, 171, 163	O(T)	CMOS 4mA	**Transmit Line Clock Out/Transmit Line Data Inverted Out for Ch. n:** Line output clock at 32 MHz derived from TxOSC, or inverted TXDn data output.
TXONn (n = 1-6)	2, 1, 207, 156, 157, 158	O(T)	CMOS 2mA	**Transmit Line ON for Ch. n:** Active high output used to turn on the transmitter of the external transceiver device.
LBn (n = 1-6)	206, 199, 191, 181, 173, 166	O(T)	CMOS 2mA	**Loopback for External Ch. n:** Control signal used to set the external transceiver to the loopback mode. The microprocessor can control this pin via control bit FLBn.
TxOSC	185	I	Schmitt Trigger	**Transmit Oscillator Input:** Local oscillator input at 32 MHz is used for line transmission and is divided internally to provide the 8 kHz marker when EXT8K=0.

CELL OUTPUT

Symbol	Pin No.	I/O/T	Type	Name/Function
RxSOC	99	O(T)	CMOS 4mA (8mA*)	**Receive Terminal Start of Cell Output:** Active high tri-stateable output, enabled only in cycles following those with $\overline{\text{RxENB}}$ asserted low.
RxCLAV	102	O(T)	CMOS 4mA (8mA*)	**Receive Terminal Cell Available Indicator Output:** Active high tri-stateable output signal which indicates that a complete cell is available for transfer. RxCLAV is driven only during the clock cycle following the one with matching SALI-25C address, RXADD(4-0). RxCLAV is asserted high to indicate it has a complete cell to transfer, otherwise RxCLAV is asserted low.
RTD(7-0)	97-90	O(T)	CMOS 4mA (8mA*)	**Receive Terminal Data Out:** Tri-stateable 8-bit cell data output bus, enabled only in cycles following those with $\overline{\text{RxENB}}$ asserted low.
RxCLK	100	I	Schmitt Trigger	**Receive Input Byte Clock:** Data is transferred and sampled on the rising edge of this input clock. The maximum frequency is 33 MHz.
$\overline{\text{RxENB}}$	101	I	TTL	**Receive Terminal Read Enable Input:** Active low read enable input signal for cell output. Tri-states RxSOC and RTD(7-0) output pins when set high.
RXADD(4-0)	88, 86, 85, 84, 83	I	TTL	**Receive Terminal Physical Device Address:** Five-bit wide address for the ports programmed in this device on ADDn(4-0).

* For UTOPIA Level 2 compliance, these pins are also characterized at 8mA.

CELL INPUT

Symbol	Pin No.	I/O/P	Type	Name/Function
TxCLAV	70	O(T)	CMOS 4mA (8mA*)	**Transmit Terminal Cell Available Indicator Output:** Active high tri-stateable output signal. TxCLAV is driven only during the clock cycle following the one with matching SALI-25C address, TXADD(4-0). TxCLAV is asserted high to indicate that the SALI-25C can accept the transfer of a complete cell, otherwise TxCLAV is asserted low.
TTD(7-0)	81-74	I	TTL	**Transmit Terminal Data In:** Tri-stateable 8-bit cell data input bus, valid when $\overline{\text{TxENB}}$ is asserted low.
TxSOC	69	I	TTL	**Transmit Terminal Start of Cell Input:** Active high input signal that indicates the start of cell input.
TxCLK	68	I	Schmitt Trigger	**Transmit Input Byte Clock:** Data is transferred and sampled on the rising edge of this input clock (max. frequency 33 MHz).
$\overline{\text{TxENB}}$	67	I	TTL	**Transmit Terminal Read Enable Input:** Active low read enable input signal for cell input.
TXADD(4-0)	66-62	I	TTL	**Transmit Terminal Physical Device Address**: Five-bit wide address for the ports programmed in this device on ADDn(4-0).

* For UTOPIA Level 2 compliance, these pins are also characterized at 8mA.

MICROPROCESSOR INTERFACE PORT

Symbol	Pin No.	I/O/P	Type	Name/Function
D(7-0)	132-125	I/O(T)	TTL in CMOS 6mA out	**Data(7-0):** Bidirectional, tri-state, 8-bit data bus used for read output and write input data from/to internal registers.
A(6 -0)	140-134	I	TTL	**Address(6-0):** 7-bit address input bus used to select an internal register for read or write access.
MOTO	114	I	TTL	**Motorola/Intel Microprocessor Interface Select:** This pin defines the operating mode of the microprocessor interface port. High selects Motorola. Low selects Intel.
$\overline{\text{SEL}}$	119	I	TTLp	**Select:** This active low signal enables the microprocessor interface and allows the transfer of information between the SALI-25C and the microprocessor.
$\overline{\text{RD}}$ / RD/$\overline{\text{WR}}$	117	I	TTLp	**Read or Read/Write:** For Intel, $\overline{\text{RD}}$ is set low to read a register; For Motorola, RD/$\overline{\text{WR}}$ is set high to read a register and RD/ $\overline{\text{WR}}$ is set low to write to a register.
$\overline{\text{WR}}$	118	I	TTLp	**Write:** For Intel, $\overline{\text{WR}}$ is set low to write to a register. For Motorola, $\overline{\text{WR}}$ should be tied high.
RDY/ $\overline{\text{DTACK}}$	115	O(T)	CMOS 8mA	**Ready:** For Intel, this active high output signal acknowledges that the data transfer can be completed during this cycle. A low indicates a need for wait states. **Data Transfer Acknowledge:** For Motorola, a low indicates data transfer completion on the data bus.

Symbol	Pin No.	I/O/P	Type	Name/Function
INTER	116	O(T)	CMOS 4mA	**Interrupt:** For Intel, this active high signal indicates an interrupt to the microprocessor. For Motorola, it is an active low signal that indicates an interrupt to the microprocessor. Control bit INVPOLI inverts the polarity for either microprocessor.
PRCLK	122	I	Schmitt Trigger	**Microprocessor Clock In:** This clock is used by the device to run internal state machines. The operational frequency range is from 8.25 to 28 MHz. The nominal frequency is not critical.

MISCELLANEOUS PINS

Symbol	Pin No.	I/O/P	Type	Name/Function
$\overline{\text{RESET}}$	113	I	TTLp	**Hardware Reset:** An active low pulse with minimum width of 200 ns must be applied after power-up to reset all registers and FIFOs. All clocks must be present for proper reset of the status and event registers. In addition, the cell counters and the multicast indicator RAM are required to be initialized by writing to the RAM locations.
8k_In/ 1k_Out	110	I/O(T)	TTL in CMOS 4mA out	**8 kHz Synchronization Event Input or 1 kHz Clock Output:** A positive input pulse indicating the 8 kHz synchronization event if control bit EXT8K is set to 1, or a 1 kHz clock output pulse if EXT8K is set to 0.
1kHz	105	I	TTL	**1 kHz Input:** A positive input pulse used to drive the LED data pin's oscillation rate. This pulse is used for the yellow signal control.
RESERVE-L	54	I	TTL	**Reserve:** Tie this pin to ground for normal operation.
RESERVE-H	106 - 109	I	TTL	**Reserve:** Tie these four pins to VDD for normal operation.

SRAM INTERFACE PORT

Symbol	Pin No.	I/O/P	Type	Name/Function
SD(15-0)	27-32 35-43 45	I/O(T)	TTL in CMOS 4mA out	**SRAM Data:** Bidirectional 16-bit data bus used for read input and write output data of SALI-25C from/to the external SRAM.
SA(15-0)	3-5 7-13 16-21	O(T)	CMOS 4mA	**Address:** 16-bit address output bus used to select external SRAM address for read or write access.
$\overline{\text{SCS1}}$ $\overline{\text{SCS2}}$	23 22	O(T)	CMOS 4mA	**SRAM Chip Select for chip 1 and 2:** These two active low output signals enable the interface to SRAM1 and/or SRAM2 and allow the transfer of information between the SALI-25C and the selected SRAM.
$\overline{\text{SOE}}$	24	O(T)	CMOS 4mA	**SRAM Output (Read) Enable:** This output signal is asserted low to initiate a SRAM read cycle.
$\overline{\text{SWE}}$	26	O(T)	CMOS 4mA	**SRAM Write Enable:** This output signal is asserted low to initiate a SRAM write cycle.

SERIAL LINE CONTROL

Symbol	Pin No.	I/O/P	Type	Name/Function
$\overline{\text{LENAm}}$ (m = 5-0)	153-148	O(T)	CMOS 2 mA	**Line Interface Enable for Ch. n (=m+1):** This active low signal enables the serial port on the external line interface transceiver. When asserted, data can be written to, or read from, the line interface to the associated transceiver.
LCK	144	O(T)	CMOS 2 mA	**Line interface Port Serial Channel Clock:** This signal is used to shift data to and from the line interface serial port. This clock is derived from PRCLK by dividing it by 4. Data out, LDO, is updated on the falling edge of LCK. Data in, LDI, is sampled on the falling edge of LCK. Please see Figure 20.
LDO	145	O(T)	CMOS 2 mA	**Line Interface Port Serial Channel Data Out:** This is the serial data output to the line interface transceiver. This output is shared among the six transceivers. This output is updated on the falling edge of LCK. Typically, the first bit is Read/$\overline{\text{Write}}$ and it is followed by fifteen address bits and two bytes of data.
LDI	146	I	TTL	**Line Interface Port Serial Channel Data In:** This is the serial data input from the line interface transceiver. This input is shared among the six transceivers. This input is sampled on the falling edge of LCK. Two bytes of data are read in from the selected device.

LED CONTROL

Symbol	Pin No.	I/O/P	Type	Name/Function
LED_Clk	59	O(T)	CMOS 2 mA	**LED Control Port Clock Output:** This signal is used to shift data out to the LED driver shift registers.
LED_Data	58	O(T)	CMOS 2 mA	**LED Control Port Data Out:** This is the serial data output to the LED driver shift registers.

BOUNDARY SCAN AND TEST

Symbol	Pin No.	I/O/P	Type	Name/Function
TDO	51	O(T)	CMOS 2 mA	**Test Data Output:** Data and test instructions from internal test registers are provided on this output pin.
$\overline{\text{TRS}}$	49	I	TTLp	**Test Mode Reset:** This pin must either be held low, asserted low, or asserted low then high (i.e., pulsed low for a minimum of 200 nanoseconds) to asynchronously reset the Test Access Port (TAP) controller. Failure to do so may cause the TAP controller to take control of the device's output pins.
TMS	48	I	TTL	**Test Mode Select:** Mode select.
TDI	47	I	TTL	**Test Data Input:** Data and test instruction input.
TCK	46	I	TTL	**Test Clock:** Clocks in signals on the rising edges.
$\overline{\text{HZEN}}$	111	I	TTLp	**High Impedance Enable:** Active low signal that causes all output and bidirectional pins to assume the tri-state condition.

ABSOLUTE MAXIMUM RATINGS AND ENVIRONMENTAL LIMITATIONS

Parameter	Symbol	Min	Max	Unit	Conditions
Supply voltage	V_{DD}	-0.3	+3.9	V	Note 1
DC input voltage	V_{IN}	-1.0	+6.0	V	Note 1
Operating junction temperature	T_J		+91	°C	Note 1
Storage temperature range	T_S	-40	+125	°C	Note 1
Ambient operating temperature	T_A	0	+70	°C	0 ft/min linear air-flow.
Component Temperature x Time	TI		270 x 5	°C x s	
Moisture Exposure Level	ME	5		Level	per EIA/JEDEC JESD22-A112-A
Relative Humidity, non-condensing	RH		100	%	Note 2
ESD Classification	ESD		±2000	V	per MIL-STD-883D Method 3015.7

Notes:
1. Conditions exceeding the Min or Max values may cause permanent failure. Exposure to conditions near the Min or Max values for extended periods may impair device reliability.
2. Pre-assembly storage in non-drypack conditions is not recommended or warranted.

THERMAL CHARACTERISTICS

Parameter	Min	Typ	Max	Unit	Test Conditions
Thermal Resistance: junction to ambient			18.9	°C/W	0 ft/min linear airflow.

POWER REQUIREMENTS

Parameter	Min	Typ	Max	Unit	Test Conditions
V_{DD}	3.135	3.3	3.465	V	
I_{DD}		135	182	mA	
Power dissipation, P_{DD}		446	600	mW	

INPUT, OUTPUT AND I/O PARAMETERS

Input Parameters For Schmitt Trigger

Parameter	Min	Typ	Max	Unit	Test Conditions
V_{T+}		1.7	2.3	V	$3.135 \le V_{DD} \le 3.465$
V_{T-}	0.6	1.0		V	$3.135 \le V_{DD} \le 3.465$
Input leakage current		0.7		µA	$V_{DD} = 3.465$
Input capacitance		3.0		pF	

Input Parameters For TTL

Parameter	Min	Typ	Max	Unit	Test Conditions
V_{IH}	2.0		5.25	V	$3.135 \le V_{DD} \le 3.465$
V_{IL}			0.8	V	$3.135 \le V_{DD} \le 3.465$
Input leakage current			10	µA	$V_{DD} = 3.465$
Input capacitance		3.0		pF	

Input Parameters For TTLp

Parameter	Min	Typ	Max	Unit	Test Conditions
V_{IH}	2.0		5.25	V	$3.135 \le V_{DD} \le 3.465$
V_{IL}			0.8	V	$3.135 \le V_{DD} \le 3.465$
Input leakage current	70	-142	-225	µA	$V_{DD} = 3.465$
Input capacitance		3.0		pF	

Output Parameters For CMOS2mA

Parameter	Min	Typ	Max	Unit	Test Conditions
V_{OH}	2.4			V	$V_{DD} = 3.135$, $I_{OH} = -2.0$
V_{OL}			0.4	V	$V_{DD} = 3.135$, $I_{OL} = 2.0$
I_{OL}			2.0	mA	
I_{OH}			-2.0	mA	
t_{RISE}			4.0	ns	25 pF load
t_{FALL}			4.0	ns	25 pF load
Leakage Tri-state	-10	±1	+10	µA	$V_{IH} = 3.465$, $V_{IL} = 0$
Output capacitance		3.0		pF	

Output Parameters For CMOS4mA (8mA*)

Parameter	Min	Typ	Max	Unit	Test Conditions
V_{OH}	2.4			V	V_{DD} = 3.135, I_{OH} = -4.0
V_{OL}			0.4	V	V_{DD} = 3.135, I_{OL} = 4.0
I_{OL}			8.0	mA	V_{OL} = 0.36V
I_{OH}			-8.0	mA	V_{OH} = 2.75V
I_{OL}			4.0	mA	V_{OL} = 0.04V
I_{OH}			-4.0	mA	V_{OH} = 2.93V
t_{RISE}			3.0	ns	25 pF load
t_{FALL}			3.0	ns	25 pF load
Leakage Tri-state	-10	±1	+10	µA	V_{IH} = 3.465, V_{IL} = 0
Output capacitance		3.0		pF	

* For UTOPIA Level 2 compliance, these pins are also characterized at ± 8mA.

Output Parameters For CMOS6mA

Parameter	Min	Typ	Max	Unit	Test Conditions
V_{OH}	2.4			V	V_{DD} = 3.135, I_{OH} = -6.0
V_{OL}			0.4	V	V_{DD} = 3.135, I_{OL} = 6.0
I_{OL}			6.0	mA	
I_{OH}			-6.0	mA	
t_{RISE}			3.0	ns	25 pF load
t_{FALL}			3.0	ns	25 pF load
Leakage Tri-state	-10	±1	+10	µA	V_{IH} = 3.465, V_{IL} = 0
Output capacitance		3.0		pF	

Output Parameters For CMOS8mA

Parameter	Min	Typ	Max	Unit	Test Conditions
V_{OH}	2.4			V	V_{DD} = 3.135, I_{OH} = -8.0
V_{OL}			0.4	V	V_{DD} = 3.135, I_{OL} = 8.0
I_{OL}			8.0	mA	
I_{OH}			-8.0	mA	
t_{RISE}			3.0	ns	25 pF load
t_{FALL}			3.0	ns	25 pF load
Leakage Tri-state	-10	±1	+10	µA	V_{IH} = 3.465, V_{IL} = 0
Output capacitance		3.0		pF	

Input/Output Parameters For TTL in, CMOS2mA out

See tables above for TTL in and CMOS2mA out

Input/Output Parameters For TTL in, CMOS4mA out

See tables above for TTL in and CMOS4mA out

Input/Output Parameters For TTL in, CMOS6mA out

See tables above for TTL in and CMOS6mA out

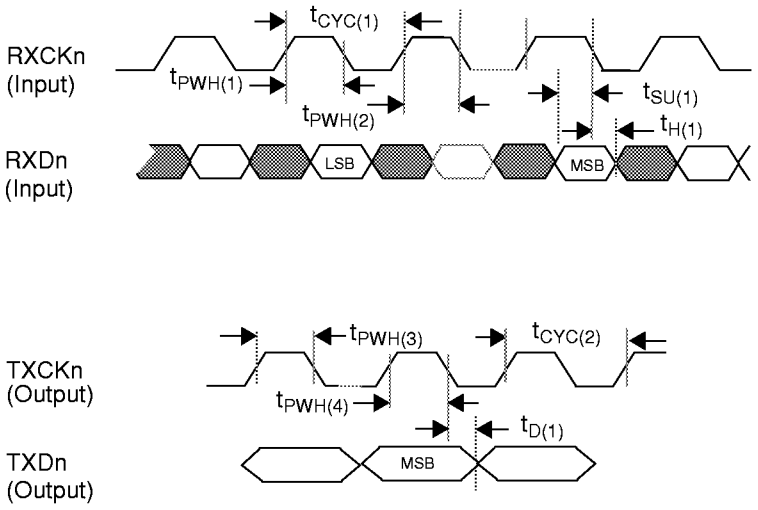
Input/Output Parameters For TTL in, CMOS8mA out

See tables above for TTL in and CMOS8mA out

TIMING CHARACTERISTICS

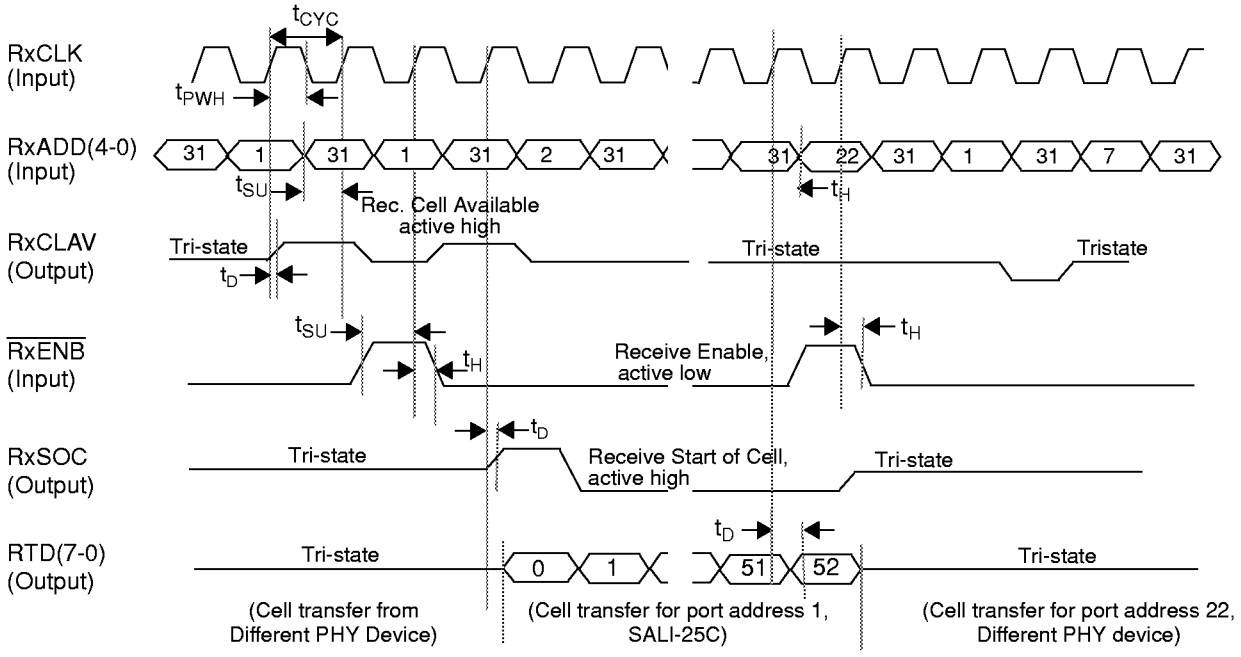
Detailed timing diagrams for the SALI-25C device are illustrated in Figures 14 through 27, with values of the timing intervals tabulated below the waveform diagrams in each figure. All output times are measured with a maximum 25 pF load capacitance. Timing parameters, except clock inputs, are measured at voltage levels of $(V_{IH} + V_{IL})/2$ for input signals or $(V_{OH} + V_{OL})/2$ for output signals. Clock inputs are measured at 2.1V for high and 0.6V for low.

Figure 14. Receive/Transmit Line Interface Timing



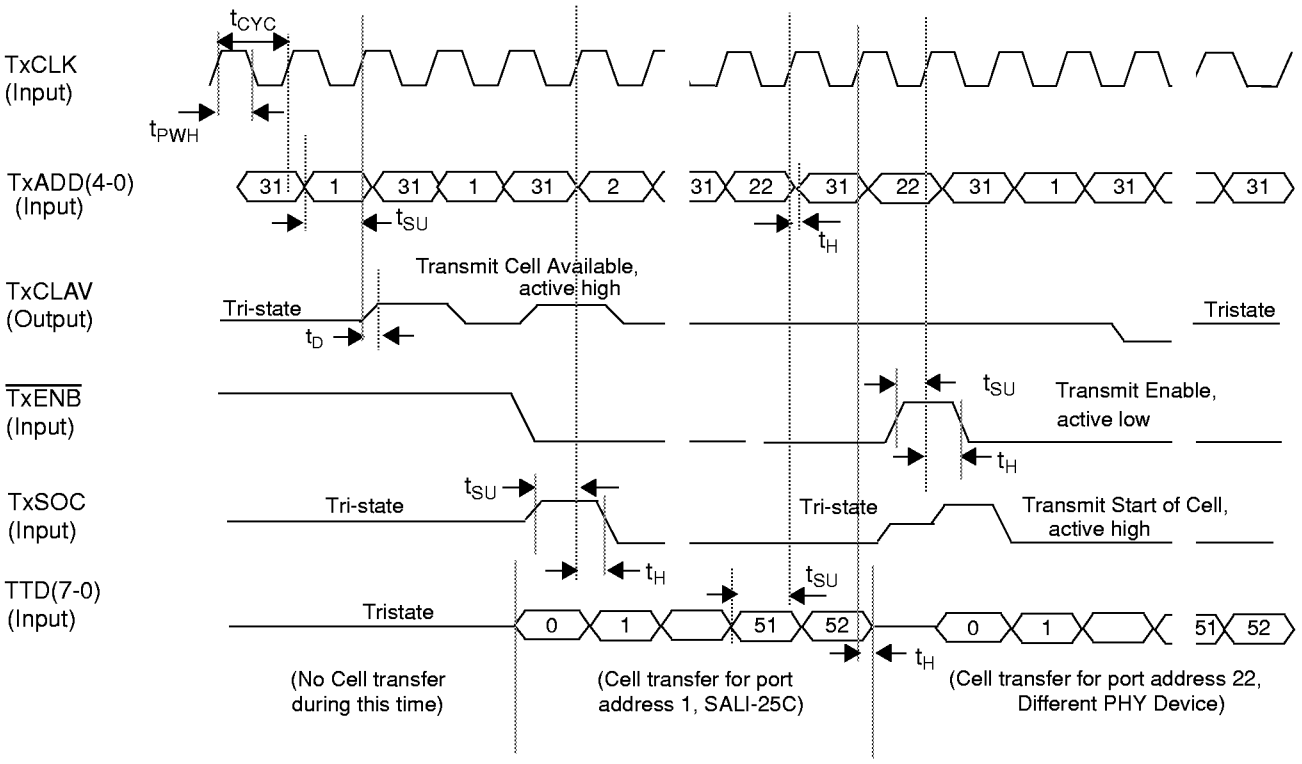
Parameter	Symbol	Min	Typ	Max	Unit
RXCKn clock period	$t_{CYC(1)}$	31.247	31.25	31.253	ns
RXCKn duty cycle distortion, $\|(t_{PWH(1)} - t_{PWH(2)})/2\|$	---			1.5	ns
RXDn set-up time to RXCKn↓ or ↑	$t_{SU(1)}$	8.0			ns
RXDn hold time after RXCKn↓ or ↑	$t_{H(1)}$	1.0			ns
TXCKn clock period	$t_{CYC(2)}$	31.247	31.25	31.253	ns
TXCKn duty cycle distortion, $\|(t_{PWH(3)} - t_{PWH(4)})/2\|$	---			1.5	ns
TXDn delay after TXCKn↓	$t_{D(1)}$	1.0		4.0	ns
RXCKn and TXCKn duty cycle (this is required only when XRAM is set to 1 and/ or FALL is set to 1)	$t_{PWH(1)}/t_{CYC(1)}$ $t_{PWH(3)}/t_{CYC(2)}$	45		55	%

Figure 15. Cell Output Timing, Multi-PHY UTOPIA Mode



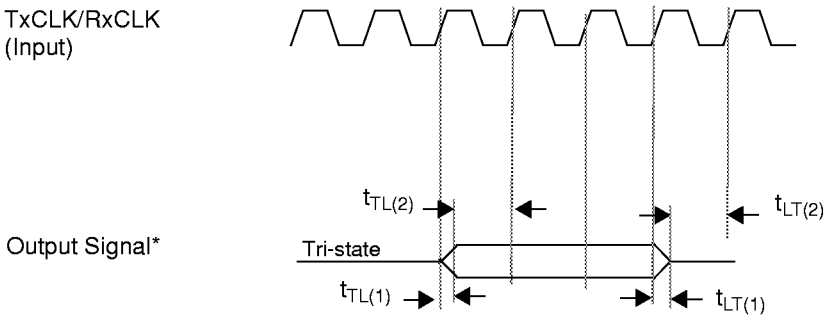
Parameter	Symbol	Min	Typ	Max	Unit
RxCLK clock period	t_{CYC}	30.30			ns
RxCLK duty cycle, t_{PWH}/t_{CYC}	---	40		60	%
$\overline{\text{RxENB}}$, RxADD(4-0) set-up time to RxCLK↑	t_{SU}	8.0			ns
$\overline{\text{RxENB}}$, RxADD(4-0) hold time after RxCLK↑	t_H	1.0			ns
RTD(7-0), RxSOC, RxCLAV delay after RxCLK↑	t_D			16	ns

Figure 16. Cell Input Timing, Multi-PHY UTOPIA Mode



Parameter	Symbol	Min	Typ	Max	Unit
TxCLK clock period	t_{CYC}	30.30			ns
TxCLK duty cycle, t_{PWH}/t_{CYC}	---	40		60	%
TTD(7-0), TxSOC, TxADD(4-0), $\overline{\text{TxENB}}$ set-up time to TxCLK↑	t_{SU}	8.0			ns
TTD(7-0), TxSOC, TxADD(4-0), $\overline{\text{TxENB}}$ hold time after TxCLK↑	t_H	1.0			ns
TxCLAV delay from TxCLK↑	t_D			16	ns

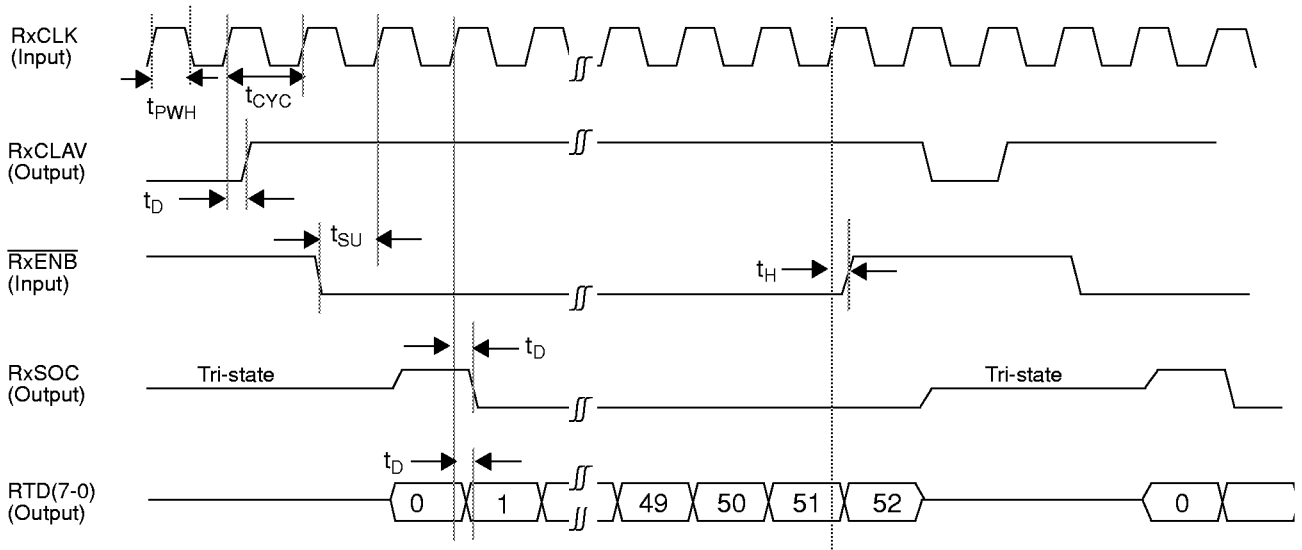
Figure 17. Tri-state Timing for UTOPIA Mode



Parameter	Symbol	Min	Typ	Max	Unit
Output signal* going low impedance before TxCLK/RxCLK↑	$t_{TL(2)}$	8.0			ns
Output signal* going high impedance before TxCLK/RxCLK↑	$t_{LT(2)}$	0.0			ns
Output signal* going low impedance after TxCLK/RxCLK↑	$t_{TL(1)}$	1.0			ns
Output signal* going high impedance after TxCLK/RxCLK↑	$t_{LT(1)}$	1.0		16	ns

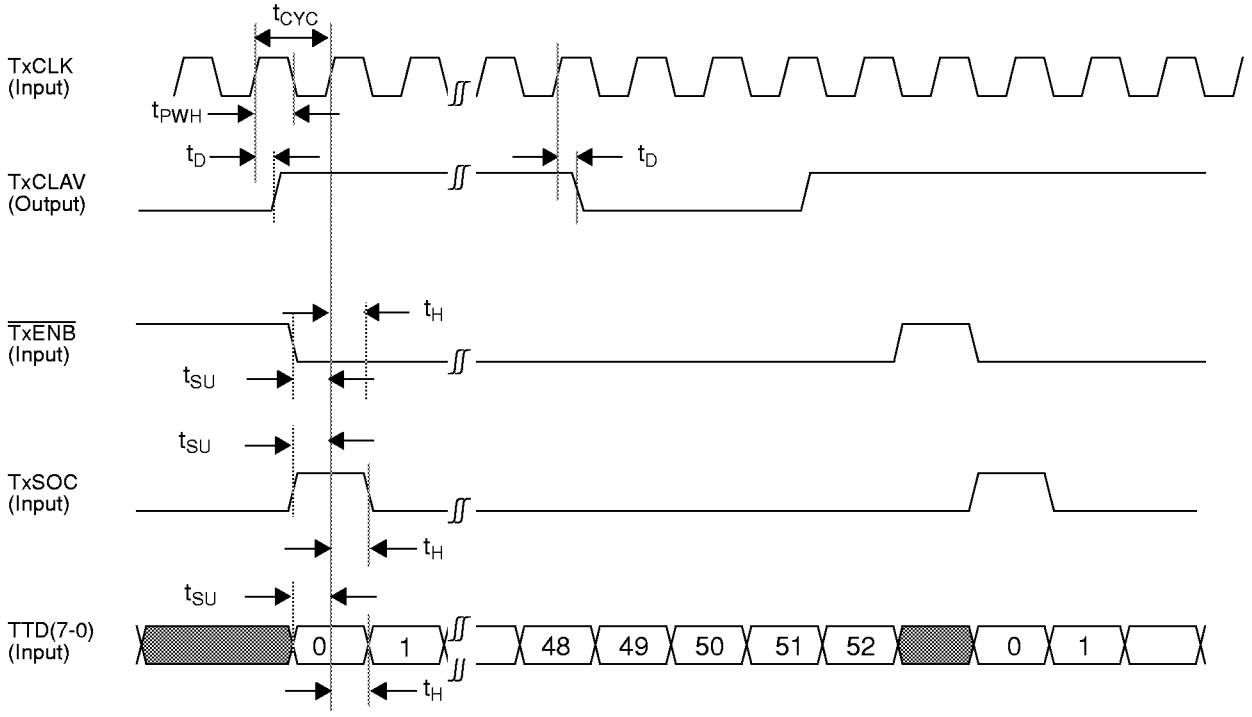
* Note: Output signal is TxCLAV, RTD(7-0), RxSOC or RxCLAV

Figure 18. Cell Output Timing, single-PHY UTOPIA Mode.



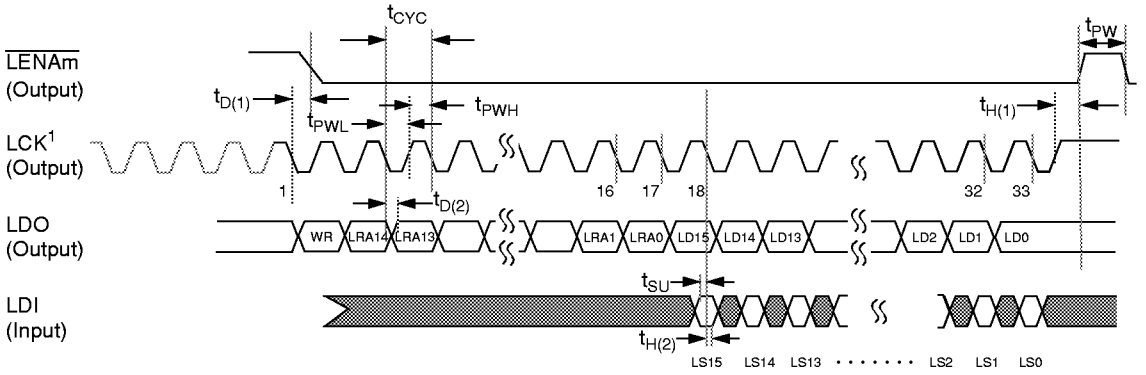
Parameter	Symbol	Min	Typ	Max	Unit
RxCLK clock period	t_{CYC}	30.30			ns
RxCLK duty cycle, t_{PWH}/t_{CYC}		40		60	%
RTD(7-0), RxSOC, RxCLAV delay after RxCLK↑	$t_{D(1)}$			16	ns
$\overline{\text{RxENB}}$ set-up time to RxCLK↑	t_{SU}	8.0			ns
$\overline{\text{RxENB}}$ hold time after RxCLK↑	t_H	1.0			ns

Figure 19. Cell Input Timing, Single-PHY UTOPIA Mode



Parameter	Symbol	Min	Typ	Max	Unit
TxCLK clock period	t_{CYC}	30.30			ns
TxCLK duty cycle, t_{PWH}/t_{CYC}		40		60	%
TTD(7-0), TxSOC, $\overline{\text{TxENB}}$ set-up time to TxCLK↑	t_{SU}	8.0			ns
TTD(7-0), TxSOC, $\overline{\text{TxENB}}$ hold time after TxCLK↑	t_H	1.0			ns
TxCLAV delay from TxCLK↑	t_D			16	ns

Figure 20. Serial Line Control Interface Port Timing

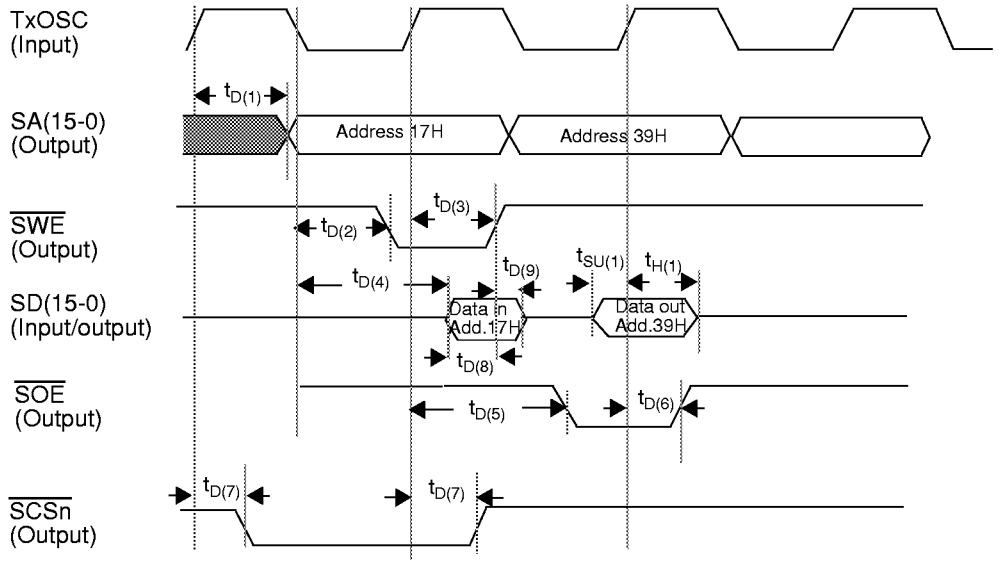


1. There could be up to 4 clocks before $\overline{\text{LENAm}}$ is asserted.

Parameter	Symbol	Min	Typ	Max	Unit
LCK clock period	t_{CYC}		4 x CP*		ns
LCK low time	t_{PWL}		2 x CP*		ns
LCK high time	t_{PWH}		2 x CP*		ns
$\overline{\text{LENAm}}$ active delay after LCK↓	$t_{D(1)}$			3 x CP*	ns
LCK↓ delay to LDO valid	$t_{D(2)}$		3.0		ns
LDI set-up to LCK↓	t_{SU}	17.0			ns
LDI hold after LCK↓	$t_{H(2)}$		1 x CP*		ns
$\overline{\text{LENAm}}$ hold after LCK↑	$t_{H(1)}$	1 x CP*			ns
$\overline{\text{LENAm}}$ inactive pulse width	t_{PW}	4 x CP*			ns

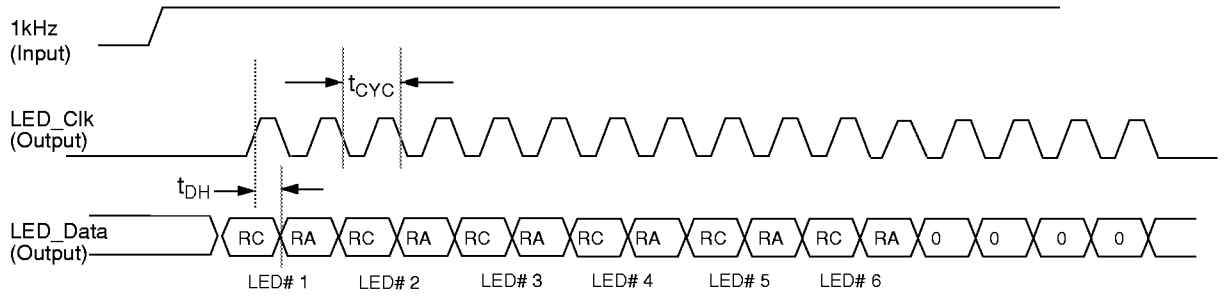
* Note: CP is the PRCLK clock period

Figure 21. External SRAM Timing - Read/Write



Parameter	Symbol	Min	Typ	Max	Unit
SA(15-0) delay after TxOSC ↑	$t_{D(1)}$			19.5	ns
$\overline{SWE}$↓ delay after TxOSC↓	$t_{D(2)}$			15.0	ns
$\overline{SWE}$↑ delay after TxOSC↑	$t_{D(3)}$			18.2	ns
SD(15-0) delay after TxOSC↓	$t_{D(4)}$			28.5	ns
$\overline{SOE}$↓ delay after TxOSC↑	$t_{D(5)}$			23.2	ns
$\overline{SOE}$↑ delay after TxOSC↑	$t_{D(6)}$			14.1	ns
$\overline{SCSn}$ change delay after TxOSC↑	$t_{D(7)}$			16.6	ns
SD(15-0) setup to TxOSC↑	$t_{SU(1)}$	-2.0			ns
SD(15-0) hold after TxOSC↑	$t_{H(1)}$	8.0			ns
$\overline{SWE}$↑ delay after SD(15-0)	$t_{D(8)}$	7.0			ns
SD(15-0), SA(15-0) change delay after $\overline{SWE}$↑	$t_{D(9)}$	1.0			ns

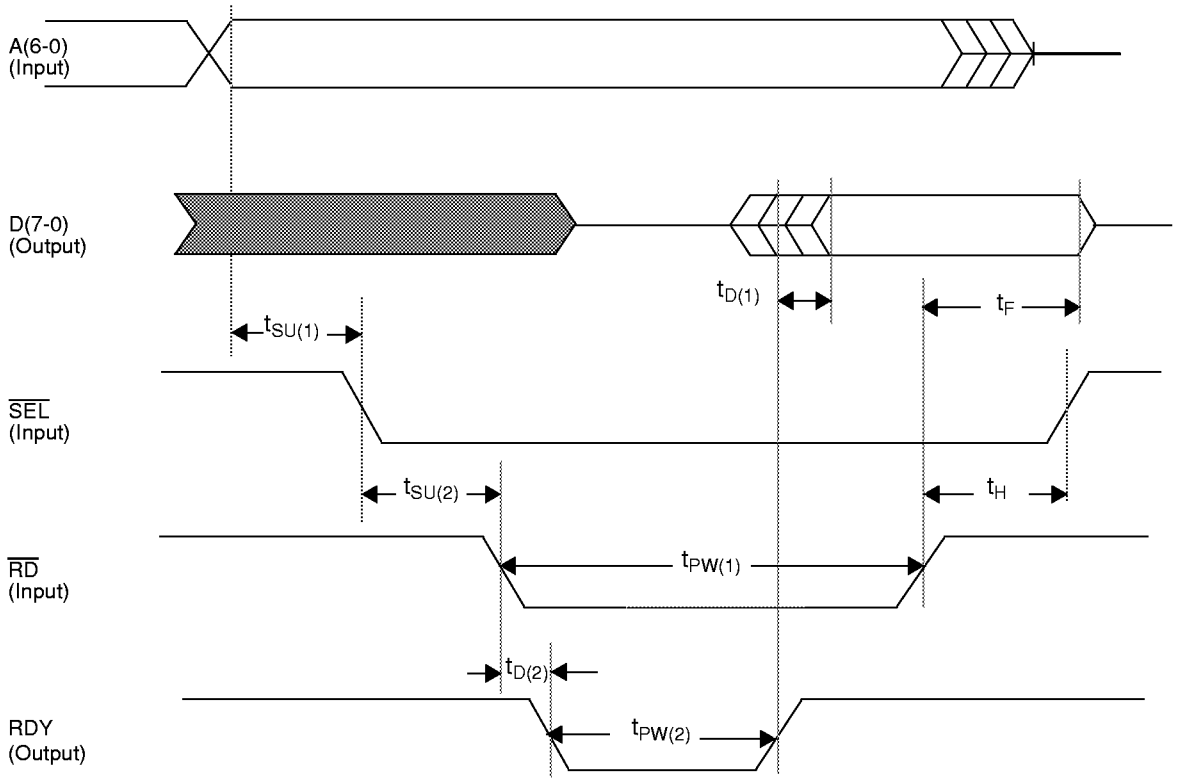
Figure 22. Serial LED Control Port Data Output Timing



Parameter	Symbol	Min	Typ	Max	Unit
LED_Clk clock frequency	t_{CYC}	4 x CP*			ns
LED_Data hold time after LED_Clk↑	t_{DH}	2 x CP*			ns

* Note: CP is the PRCLK clock period.

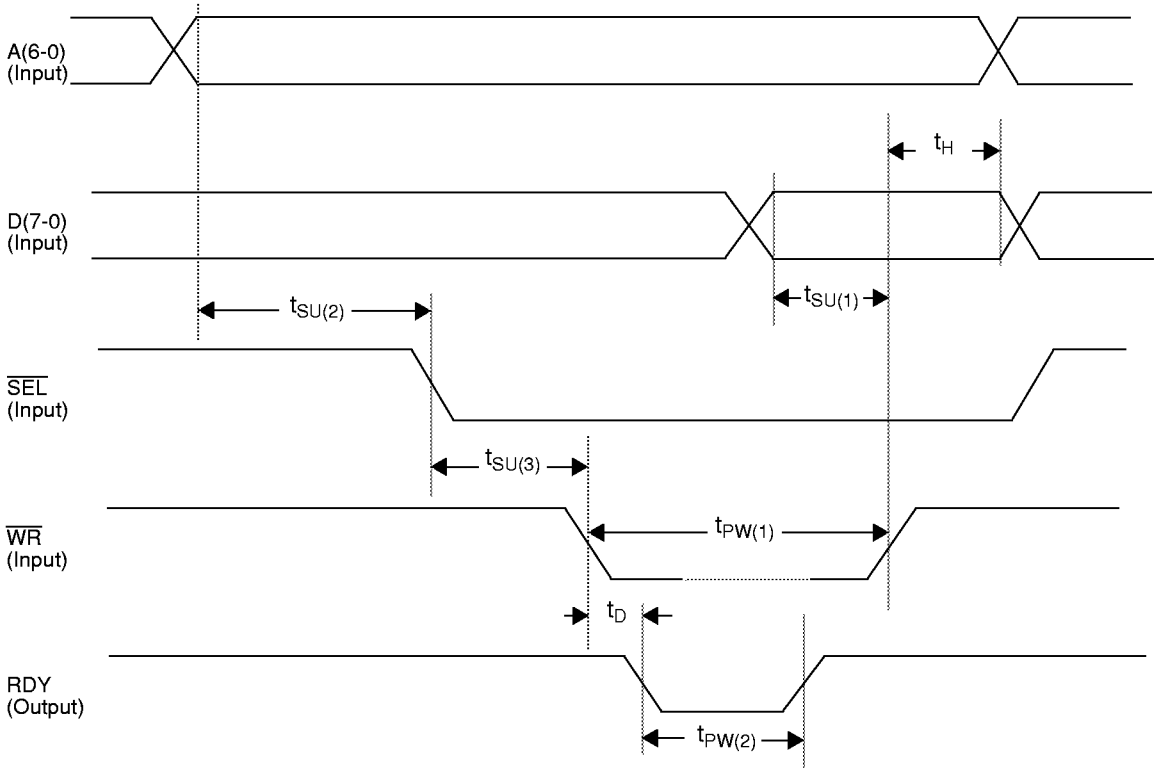
Figure 23. Microprocessor Read Timing - Intel Mode



Parameter	Symbol	Min	Typ	Max	Unit
A(6-0) address set-up time to $\overline{SEL}\downarrow$	$t_{SU(1)}$	0.0			ns
D(7-0) data valid delay after RDY$\uparrow$	$t_{D(1)}$	-2 x CP*			ns
D(7-0) data float time after $\overline{RD}\uparrow$	t_F	10			ns
$\overline{SEL}$ set-up time to $\overline{RD}\downarrow$	$t_{SU(2)}$	0.0			ns
$\overline{RD}$ pulse width	$t_{PW(1)}$	2.5 x CP *			ns
$\overline{SEL}$ hold time after $\overline{RD}\uparrow$	t_H	0.0			ns
RDY delay after $\overline{RD}\downarrow$	$t_{D(2)}$			15	ns
RDY pulse width	$t_{PW(2)}$	1 x CP *		4 x CP *	ns

* Note: CP is the PRCLK clock period.

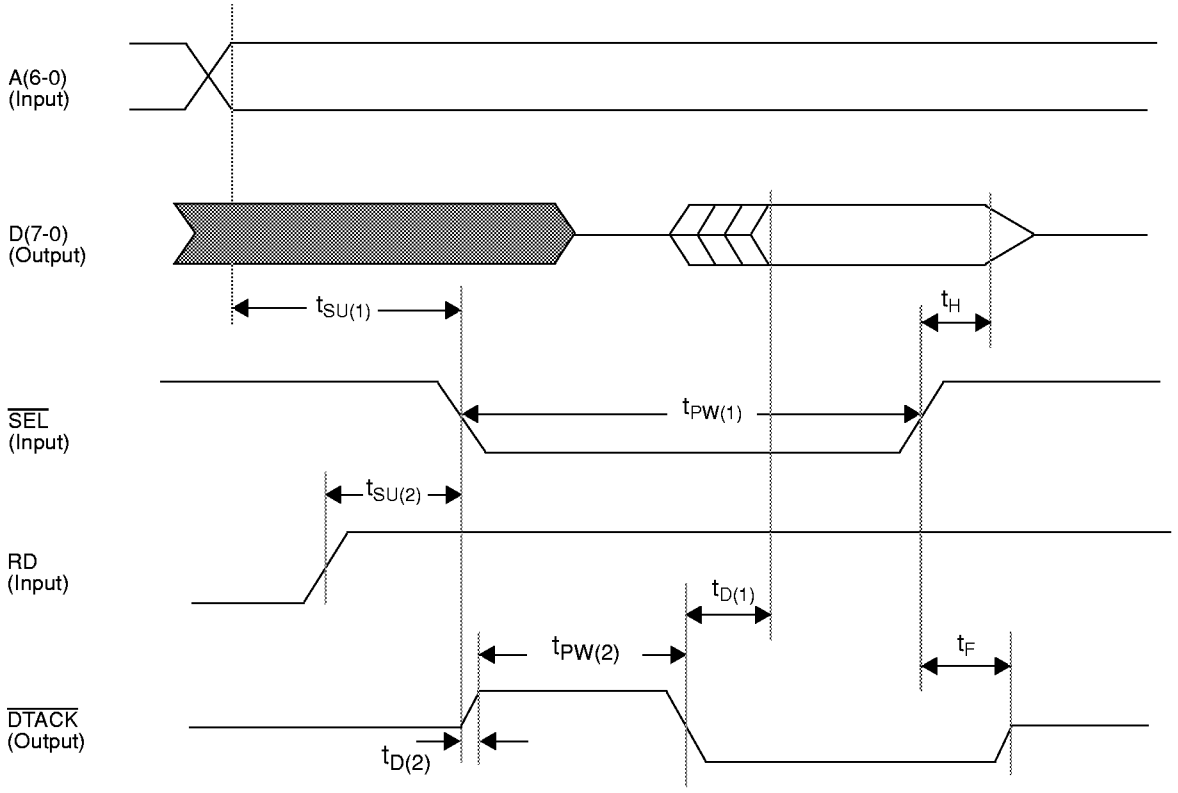
Figure 24. Microprocessor Write Timing - Intel Mode



Parameter	Symbol	Min	Typ	Max	Unit
A(6-0) address set-up time to $\overline{SEL}\downarrow$	$t_{SU(2)}$	0.0			ns
D(7-0) data valid set-up time to $\overline{WR}\uparrow$	$t_{SU(1)}$	5.0	20		ns
D(7-0) data valid hold time after $\overline{WR}\uparrow$	t_H	6.0			ns
$\overline{SEL}$ set-up time to $\overline{WR}\downarrow$	$t_{SU(3)}$	0.0			ns
$\overline{WR}$ pulse width	$t_{PW(1)}$	2.5 x CP*			ns
RDY delay after $\overline{WR}\downarrow$	t_D			10	ns
RDY pulse width	$t_{PW(2)}$	0.0		4 x CP *	ns

* Note: CP is the PRCLK clock period.

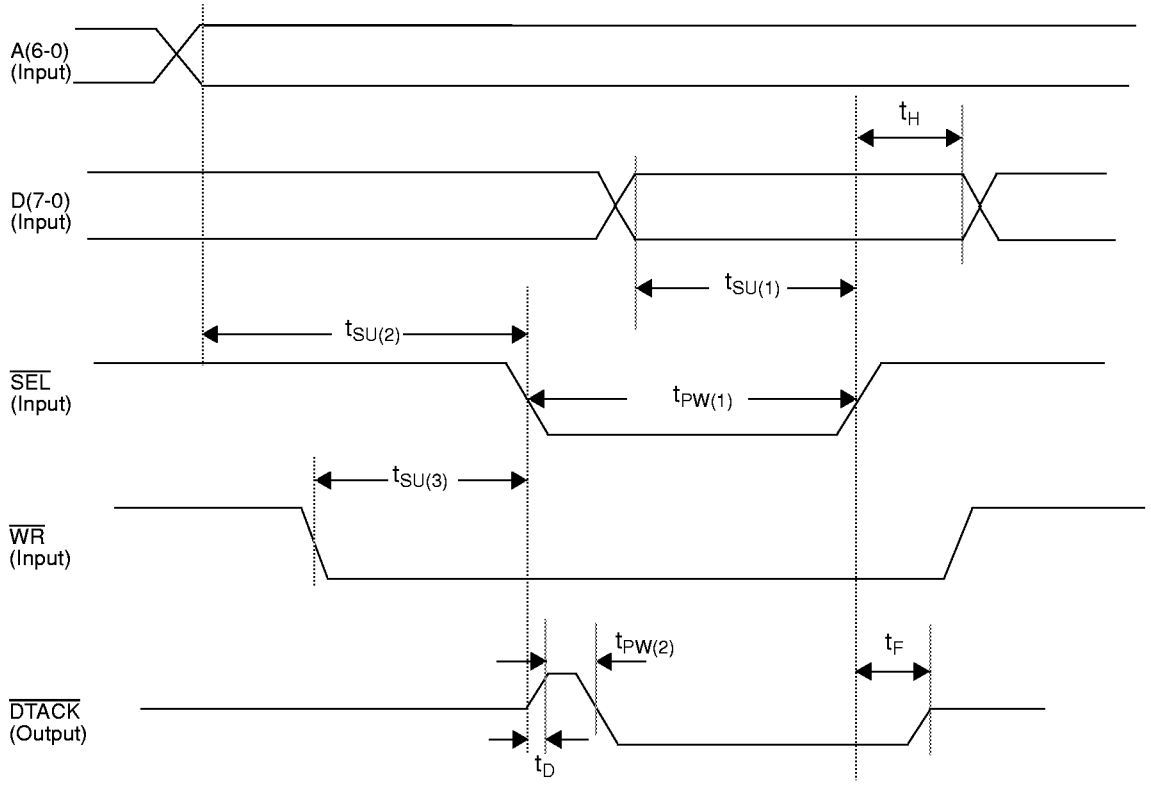
Figure 25. Microprocessor Read Timing - Motorola Mode



Parameter	Symbol	Min	Typ	Max	Unit
A(6-0) address valid set-up time to $\overline{SEL}\downarrow$	$t_{SU(1)}$	0.0			ns
D(7-0) data output delay after $\overline{DTACK}\downarrow$	$t_{D(1)}$	-2 x CP*			ns
D(7-0) data hold time after $\overline{SEL}\uparrow$	t_H	20			ns
RD set-up time to $\overline{SEL}\downarrow$	$t_{SU(2)}$	0.0			ns
$\overline{SEL}$ pulse width	$t_{PW(1)}$	2.5 x CP*			ns
$\overline{DTACK}$ pulse width	$t_{PW(2)}$	1 x CP *		4 x CP *	ns
$\overline{DTACK}$ float time after $\overline{SEL}\uparrow$	t_F	10			ns
$\overline{DTACK}$ delay after $\overline{SEL}\downarrow$	$t_{D(2)}$			11	ns

* Note: CP is the PRCLK clock period.

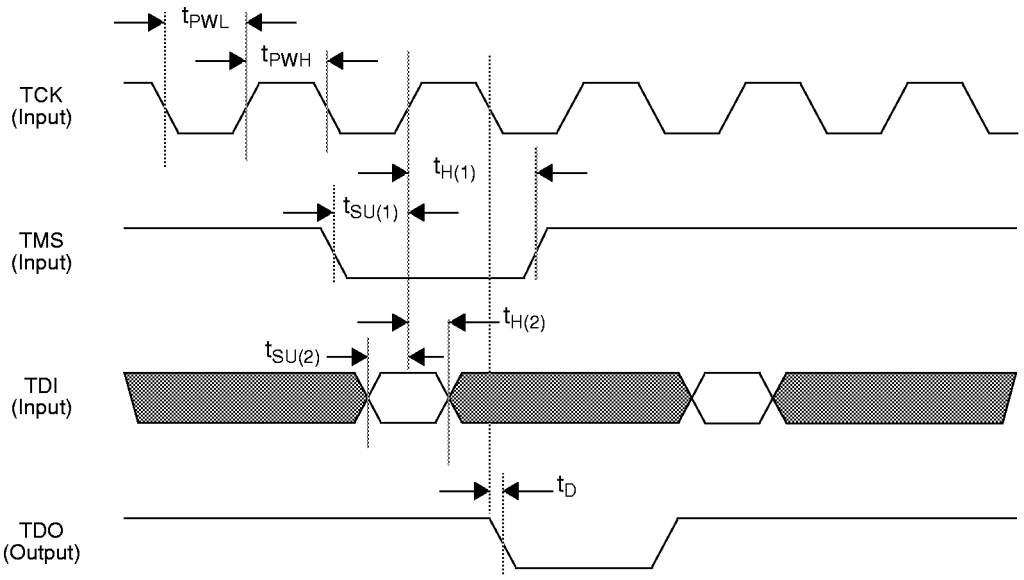
Figure 26. Microprocessor Write Timing - Motorola Mode



Parameter	Symbol	Min	Typ	Max	Unit
A(6-0) address valid set-up time to $\overline{SEL}\downarrow$	$t_{SU(2)}$	0.0			ns
D(7-0) data valid set-up time before $\overline{SEL}\uparrow$	$t_{SU(1)}$	5.0	20		ns
D(7-0) data valid hold time after $\overline{SEL}\uparrow$	t_H	5.0			ns
$\overline{WR}$ set-up time to $\overline{SEL}\downarrow$	$t_{SU(3)}$	0.0			ns
$\overline{SEL}$ pulse width	$t_{PW(1)}$	2.5 x CP*			ns
$\overline{DTACK}$ pulse width	$t_{PW(2)}$	0.0		4 x CP *	ns
$\overline{DTACK}$ float time after $\overline{SEL}\uparrow$	t_F	10			ns
$\overline{DTACK}$ delay after $\overline{SEL}\downarrow$	t_D			13	ns

* CP is the PRCLK clock period.

Figure 27. Boundary Scan Timing



Parameter	Symbol	Min	Max	Unit
TCK clock period	-	-	6.25	MHz
TCK clock high time	t_{PWH}	50		ns
TCK clock low time	t_{PWL}	50		ns
TMS setup time to TCK↑	$t_{SU(1)}$	8.0	-	ns
TMS hold time after TCK↑	$t_{H(1)}$	2.0	-	ns
TDI setup time to TCK↑	$t_{SU(2)}$	3.0	-	ns
TDI hold time after TCK↑	$t_{H(2)}$	2.0	-	ns
TDO delay from TCK↓	t_D	-	9.0	ns

OPERATION

TEST ACCESS PORT

High Impedance State

An active low $\overline{\text{HZEN}}$ input pin is provided. It may be used to place all tri-stateable output and bidirectional pins of the SALI-25C into a high impedance state for systems that do not support the IEEE 1149.1 standard.

Boundary Scan Support

The IEEE 1149.1 Standard defines the requirements of a boundary scan architecture that has been specified by the IEEE Joint Test Action Group (JTAG). Boundary scan is a specialized scan architecture that provides observability and controllability for the interface pins of the device. The Test Access Port block, which implements the boundary scan functions, consists of a Test Access Port (TAP) controller, instruction and data registers, and a boundary scan register path bordering the input and output pins, as illustrated in Figure 28. The boundary scan test bus interface consists of four input signals (i.e., the Test Clock (TCK), Test Mode Select (TMS), Test Data Input (TDI) and Test Reset ($\overline{\text{TRS}}$) input signals) and a Test Data Output (TDO) output signal. A brief description of boundary scan operation is provided below; further information is available in the IEEE Standard document.

The TAP controller receives external control information via a Test Clock (TCK) signal, a Test Mode Select (TMS) signal, and a Test Reset ($\overline{\text{TRS}}$) signal, and it sends control signals to the internal scan paths. The scan path architecture consists of a two-bit serial instruction register and two or more serial data registers. The instruction and data registers are connected in parallel between the serial Test Data Input (TDI) and Test Data Output (TDO) signals. The Test Data Input (TDI) signal is routed to both the instruction and data registers and is used to transfer serial data into a register during a scan operation. The Test Data Output (TDO) is selected to send data from either register during a scan operation.

When boundary scan testing is not being performed, the boundary scan register is transparent, allowing the input and output signals at the device pins to pass to and from the SALI-25C device's internal logic, as illustrated in Figure 28. During boundary scan testing, the boundary scan register disables the normal flow of input and output signals to allow the device to be controlled and observed via scan operations. A timing diagram for the boundary scan feature is provided in Figure 27.

The maximum frequency the SALI-25C device will support for boundary scan is 6.25 MHz. The SALI-25C device performs the following boundary scan test instructions:

- EXTEST
- SAMPLE/PRELOAD
- BYPASS
- TXCIDCODE

EXTEST Test Instruction:

One of the required boundary scan tests is the external boundary test (EXTEST) instruction. When this instruction is shifted in, the SALI-25C device is forced into an off-line test mode. While in this test mode, the test bus can shift data through the boundary scan registers to control the external SALI-25C input and output leads.

SAMPLE/PRELOAD Test Instruction:

When the SAMPLE/PRELOAD instruction is shifted in, the SALI-25C device remains fully operational. While in this test mode, SALI-25C input data, and data destined for device outputs, can be captured and shifted out for inspection. The data is captured in response to control signals sent to the TAP controller.

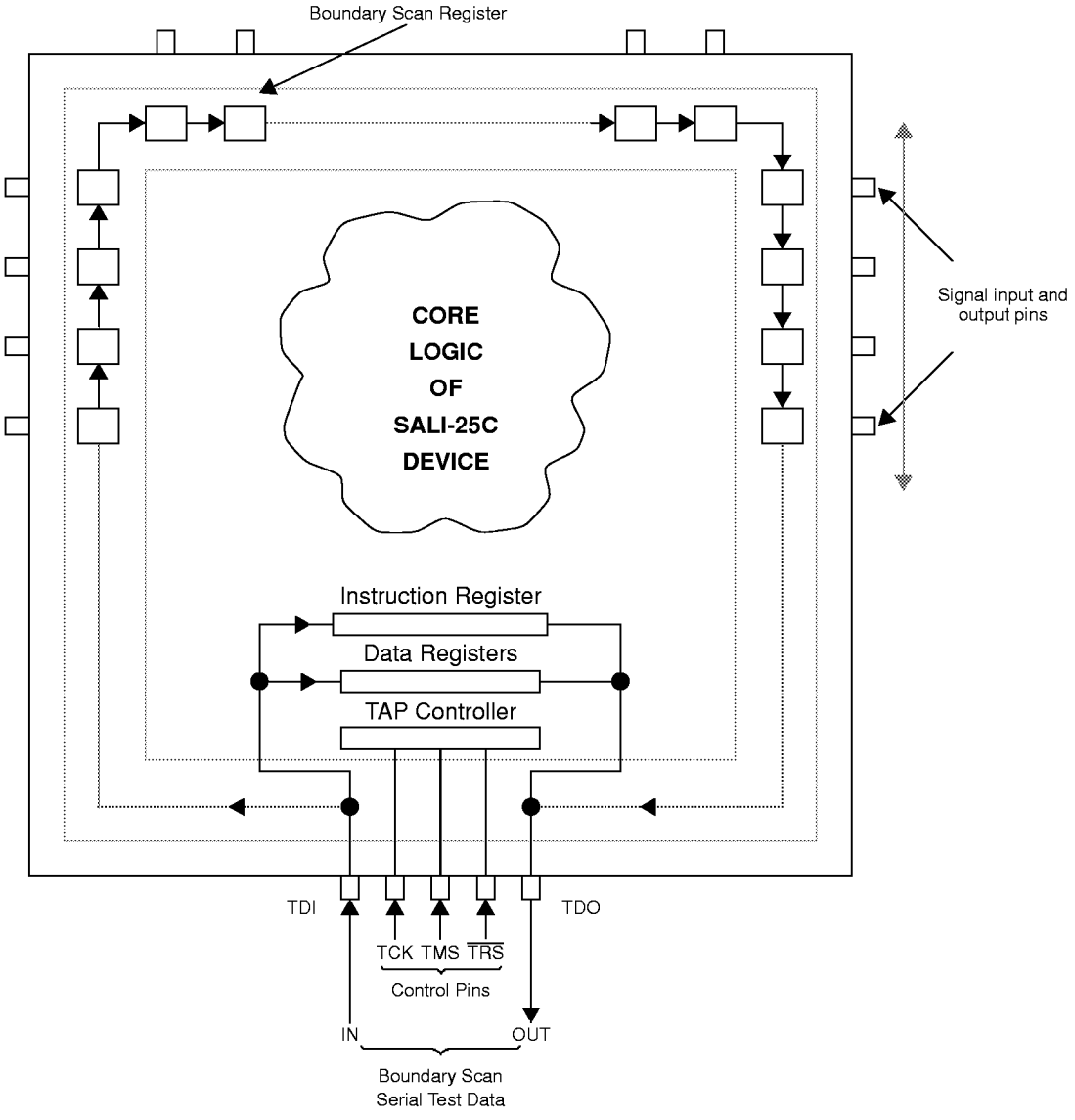
BYPASS Test Instruction:

When the BYPASS instruction is shifted in, the SALI-25C device remains fully operational. While in this test mode, a scan operation will transfer serial data from the TDI input, through an internal scan cell, to the TDO pin. The purpose of this instruction is to abbreviate the scan path through the circuits that are not being tested to only a single clock delay.

TXCIDCODE Test Instruction:

When the TXCIDCODE instruction is shifted in, the SALI-25C device remains fully operational. While in this test mode, a scan operation will transfer out from the TDO pin the following 4-byte (32-bit) sequence that identifies the SALI-25C device: version number code, initially 0H (4 bits), part code 1DC9H, representing the 07625 decimal code in the TranSwitch part number (16 bits), manufacturer ID code 06BH for TranSwitch (11 bits), and a fixed 1H code (1 bit).

Figure 28. Boundary Scan Schematic



Boundary Scan Chain

There are 191 scan cells in the SALI-25C boundary scan chain. Bidirectional signals require two scan cells. Additional scan cells are used for direction control as needed. A BSDL file for board level ATE testing is available upon request. The following table shows the listed order of the scan cells and their functions.

Scan Cell No.	I/O/E	Pin No.	Symbol	Comments
0	I	47	TDI	
1	I	54	RESERVE-L	
2	O	58	LED_Data	
3	O	59	LED_Clk	
4	I	62	TxADD0	
5	I	63	TxADD1	
6	I	64	TxADD2	
7	I	65	TxADD3	
8	I	66	TxADD4	
9	I	67	$\overline{\text{TxENB}}$	
10	I	68	TxCLK	
11	I	69	TxSOC	
12	O	70	TxCLAV	
13	I	74	TTD0	
14	I	75	TTD1	
15	I	76	TTD2	
16	I	77	TTD3	
17	I	78	TTD4	
18	I	79	TTD5	
19	I	80	TTD6	
20	I	81	TTD7	
21	I	83	RxADD0	
22	I	84	RxADD1	
23	I	85	RxADD2	
24	I	86	RxADD3	
25	I	88	RxADD4	
26	O	90	RTD0	
27	O	91	RTD1	
28	O	92	RTD2	
29	O	93	RTD3	

Scan Cell No.	I/O/E	Pin No.	Symbol	Comments
30	O	94	RTD4	
31	O	95	RTD5	
32	O	96	RTD6	
33	O	97	RTD7	
34	O	99	RxSOC	
35	I	100	RxCLK	
36	I	101	$\overline{\text{RxENB}}$	
37	O	102	RxCLAV	
38	I	105	1kHz	
39	I	106	RESERVE-H	
40	I	107	RESERVE-H	
41	I	108	RESERVE-H	
42	I	109	RESERVE-H	
43/44	I/O	110	8k_In/1k_Out	
45	I	111	$\overline{\text{HZEN}}$	
46	I	113	$\overline{\text{RESET}}$	
47	I	114	MOTO	
48	O	115	RDY/$\overline{\text{DTACK}}$	
49	O	116	INTER	
50	I	117	$\overline{\text{RD}}$ / RD/$\overline{\text{WR}}$	
51	I	118	$\overline{\text{WR}}$	
52	I	119	$\overline{\text{SEL}}$	
53	I	122	PRCLK	
54/55	I/O	125	D0	
56/57	I/O	126	D1	
58/59	I/O	127	D2	
60/61	I/O	128	D3	
62/63	I/O	129	D4	
64/65	I/O	130	D5	
66/67	I/O	131	D6	
68/69	I/O	132	D7	
70	I	134	A0	
71	I	135	A1	
72	I	136	A2	

Scan Cell No.	I/O/E	Pin No.	Symbol	Comments
73	I	137	A3	
74	I	138	A4	
75	I	139	A5	
76	I	140	A6	
77	O	144	LCK	
78	O	145	LDO	
79	I	146	LDI	
80	O	148	$\overline{\text{LENA0}}$	
81	O	149	$\overline{\text{LENA1}}$	
82	O	150	$\overline{\text{LENA2}}$	
83	O	151	$\overline{\text{LENA3}}$	
84	O	152	$\overline{\text{LENA4}}$	
85	O	153	$\overline{\text{LENA5}}$	
86	O	156	TXON4	
87	O	157	TXON5	
88	O	158	TXON6	
89	I	160	RXCK6	
90	I	161	RXD6	
91	O	162	TXD6	
92	O	163	TXCK6	
93	O	165	$\overline{\text{FrAq6}}$/FrAq6	
94	O	166	LB6	
95	I	167	RXCK5	
96	I	168	RXD5	
97	O	170	TXD5	
98	O	171	TXCK5	
99	O	172	$\overline{\text{FrAq5}}$/FrAq5	
100	O	173	LB5	
101	I	175	RXCK4	
102	I	176	RXD4	
103	O	177	TXD4	
104	O	178	TXCK4	
105	O	180	$\overline{\text{FrAq4}}$/FrAq4	
106	O	181	LB4	

Scan Cell No.	I/O/E	Pin No.	Symbol	Comments
107	I	182	RXCK3	
108	I	183	RXD3	
109	I	185	TxOSC	
110	O	188	TXD3	
111	O	189	TXCK3	
112	O	190	$\overline{\text{FrAq3}}$/FrAq3	
113	O	191	LB3	
114	I	193	RXCK2	
115	I	194	RXD2	
116	O	195	TXD2	
117	O	196	TXCK2	
118	O	198	$\overline{\text{FrAq2}}$/FrAq2	
119	O	199	LB2	
120	I	200	RXCK1	
121	I	201	RXD1	
122	O	203	TXD1	
123	O	204	TXCK1	
124	O	205	$\overline{\text{FrAq1}}$/FrAq1	
125	O	206	LB1	
126	O	207	TXON3	
127	O	1	TXON2	
128	O	2	TXON1	
129	O	3	SA15	
130	O	4	SA14	
131	O	5	SA13	
132	O	7	SA12	
133	O	8	SA11	
134	O	9	SA10	
135	O	10	SA9	
136	O	11	SA8	
137	O	12	SA7	
138	O	13	SA6	
139	O	16	SA5	
140	O	17	SA4	

Scan Cell No.	I/O/E	Pin No.	Symbol	Comments
141	O	18	SA3	
142	O	19	SA2	
143	O	20	SA1	
144	O	21	SA0	
145	O	22	$\overline{SCS2}$	
146	O	23	$\overline{SCS1}$	
147	O	24	$\overline{SOE}$	
148	O	26	$\overline{SWE}$	
149/150	I/O	27	SD15	
151/152	I/O	28	SD14	
153/154	I/O	29	SD13	
155/156	I/O	30	SD12	
157/158	I/O	31	SD11	
159/160	I/O	32	SD10	
161/162	I/O	35	SD9	
163/164	I/O	36	SD8	
165/166	I/O	37	SD7	
167/168	I/O	38	SD6	
169/170	I/O	39	SD5	
171/172	I/O	40	SD4	
173/174	I/O	41	SD3	
175/176	I/O	42	SD2	
177/178	I/O	43	SD1	
179/180	I/O	45	SD0	
181	E	--	SDEN	Bi-directional enable for SD bus.
182	E	--	DEN	Bi-directional enable for µp data bus.
183	E	--	RDYEN	Output enable for RDY (pin 115).
184	E	--	HIZ	Enable signal derived from $\overline{HZEN}$ (pin 111).
185	E	--	RXCLAVEN	Output enable for RxCLAV.
186	E	--	RXSOCEN	Output enable for RxSOC.
187	E	--	RTDEN	Output enable for RTD bus.
188	E	--	TXCLAVEN	Output enable for TxCLAV.
189	E	--	8K/1KEN	Bi-directional enable for 8k_In/1k_Out (pin 110).
190	O	51	TDO	

MEMORY MAP

All memory map locations are identified in the tables shown below. Detailed descriptions are provided in the next section.

Upon hardware reset, all configuration registers (00H-0FH), all control registers (10H-1CH, 59H-5FH), and all status, event and interrupt mask registers (30H-42H) are cleared to zeros. Internal RAM locations (counter addresses 01H to 12H, session addresses 00H to 3FH) should be cleared by writing 0s to them through the counters' read/write control registers and session multicast indicator read/write control registers, as described below.

Reading and writing of any of the internal RAM locations is achieved through the corresponding read/write control registers. To read a counter, first write a 1 into the read-write bit CRW with the corresponding RAM address bits CADD(4-0) set to the address code of the desired counter. This will place the 24-bit counter bits onto the corresponding registers (CB23-CB0) from which they may be read. To write to a 24-bit counter, first write the desired value into the corresponding registers (CB23-CB0) and then write a 0 to the read-write bit CRW with CADD(4-0) set to select the desired counter. The read-write operation of the multicast indicator RAMs is the same as described for the 24-bit counters, except that these RAM locations use MPD(7-0) for data, MPI(5-0) for address and MPRW for read-write, and that they can only be verified by reading the location twice immediately after it has been written, disregarding the result of the first read operation.

CONFIGURATION AND CONTROL, AND COMMON MODE STATUS REGISTERS

Address (Hex)	Mode[1]	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
00	R/W	SRST (SOFTWARE RESET) = 91 (Hex)							
01	R/W	XRAM[3]	U1[3]	MCAST[3]	4Q[3]	INVFRAQ[3]	FALL[3]	TTP[3]	DROPCELL[3]
02	R/W	IPOS[3]	INEG[3]	INVPOLI[3]	Set to 0				
03	R/W	8KEN[3]	EXT8K[3]	NTDAT[3]	NRZ[3]	XCODE			
04	R/W	TXEN6	RXEN6	XOFF6	ADD6(4-0)[3]				
05	R/W	TXEN5	RXEN5	XOFF5	ADD5(4-0)[3]				
06	R/W	TXEN4	RXEN4	XOFF4	ADD4(4-0)[3]				
07	R/W	TXEN3	RXEN3	XOFF3	ADD3(4-0)[3]				
08	R/W	TXEN2	RXEN2	XOFF2	ADD2(4-0)[3]				
09	R/W	TXEN1	RXEN1	XOFF1	ADD1(4-0)[3]				
0A	R/W	Set to 0		4K[3]	RINBAND[3]		TINBAND[3]		
0B	R/W	TESTPAT(7-0)[3]							
0C	R/W	LINKRES[3]							
0D	R/W	MINLP/MINLP11[3] (See Note 2)				MINLP/MINLP10[3] (See Note 2)			
0E	R/W	MINLP01[3]				MINLP00[3]			
0F	R/W	Set to 0							

Notes:
1. R/W=Read/Write. Unused bits in used R/W locations should be set to 0.
2. The nibbles MINLP11 and MINLP10 are used together as byte MINLP when control bit 4Q is set to 0.
3. To change these global configuration bits after normal operation has started requires a software reset (SRST in address 00H).

SERIAL LINE CONTROL INTERFACE PORT REGISTERS

Address (Hex)	Mode*	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
10	R/W	Unused					LN2	LN1	LN0
11	R/W	LRW	LRA14	LRA13	LRA12	LRA11	LRA10	LRA9	LRA8
12	R/W	LRA7	LRA6	LRA5	LRA4	LRA3	LRA2	LRA1	LRA0
13	R	LS15	LS14	LS13	LS12	LS11	LS10	LS9	LS8
14	R	LS7	LS6	LS5	LS4	LS3	LS2	LS1	LS0
15	R/W	LD15	LD14	LD13	LD12	LD11	LD10	LD9	LD8
16	R/W	LD7	LD6	LD5	LD4	LD3	LD2	LD1	LD0
17	R/W	Unused							LSTATUS

* Note: R=Read-only; R/W=Read/Write. Unused bits in used R/W locations should be set to 0.

EXTERNAL DEVICE CONTROL

Address (Hex)	Mode*	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
18	R/W	Unused	INVTXO	FTOFF1	FTOFF2	FTOFF3	FTOFF4	FTOFF5	FTOFF6
19	R/W	Unused		FLB6	FLB5	FLB4	FLB3	FLB2	FLB1
1A	R/W	Unused		LED6C(2-0)			LED5C(2-0)		
1B	R/W	Unused		LED4C(2-0)			LED3C(2-0)		
1C	R/W	Unused		LED2C(2-0)			LED1C(2-0)		
1D-2F	R/W	Unused							

* Note: R/W=Read/Write. Unused bits in used R/W locations should be set to 0.

STATUS, EVENT AND INTERRUPT MASK REGISTERS

Address (Hex)	Mode*	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
30	R(L)	Unused		CHERR6	CHERR5	CHERR4	CHERR3	CHERR2	CHERR1
31	R	Unused		DROPC6	ROTO6	5BCODE6	RBFUL6	RHECE6	FREQE6
32	R/(L)	Unused		DROPC6	ROTO6	5BCODE6	RBFUL6	RHECE6	FREQE6
33	R/W	Unused		DROPC6	ROTO6	5BCODE6	RBFUL6	RHECE6	FREQE6
34	R	Unused		DROPC5	ROTO5	5BCODE5	RBFUL5	RHECE5	FREQE5
35	R/(L)	Unused		DROPC5	ROTO5	5BCODE5	RBFUL5	RHECE5	FREQE5
36	R/W	Unused		DROPC5	ROTO5	5BCODE5	RBFUL5	RHECE5	FREQE5
37	R	Unused		DROPC4	ROTO4	5BCODE4	RBFUL4	RHECE4	FREQE4
38	R/(L)	Unused		DROPC4	ROTO4	5BCODE4	RBFUL4	RHECE4	FREQE4
39	R/W	Unused		DROPC4	ROTO4	5BCODE4	RBFUL4	RHECE4	FREQE4
3A	R	Unused		DROPC3	ROTO3	5BCODE3	RBFUL3	RHECE3	FREQE3
3B	R/(L)	Unused		DROPC3	ROTO3	5BCODE3	RBFUL3	RHECE3	FREQE3
3C	R/W	Unused		DROPC3	ROTO3	5BCODE3	RBFUL3	RHECE3	FREQE3
3D	R	Unused		DROPC2	ROTO2	5BCODE2	RBFUL2	RHECE2	FREQE2
3E	R/(L)	Unused		DROPC2	ROTO2	5BCODE2	RBFUL2	RHECE2	FREQE2
3F	R/W	Unused		DROPC2	ROTO2	5BCODE2	RBFUL2	RHECE2	FREQE2
40	R	Unused		DROPC1	ROTO1	5BCODE1	RBFUL1	RHECE1	FREQE1
41	R/(L)	Unused		DROPC1	ROTO1	5BCODE1	RBFUL1	RHECE1	FREQE1
42	R/W	Unused		DROPC1	ROTO1	5BCODE1	RBFUL1	RHECE1	FREQE1
43	R	Reserved							
44	R/(L)	Reserved							
45	R/W	Set to 0							**Set to 1**
46	R	Reserved							
47	R(L)	Reserved							
48	R/W	Set to 0							
49-4F		Unused							

* Note: R = Read-only; R(L) = Read-only (latched) - clears to 0 when read; R/W = Read/Write.
Unused bits in used R/W locations should be set to 0, unless otherwise indicated.
Unused bits in used R and R(L) registers should be disregarded.

SESSION MULTICAST INDICATOR READ/WRITE CONTROL REGISTERS (CUBIT MODE)

Address (Hex)	Mode[1]	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
59	W	MPRW	Unused						
5A	W	Unused		MPI5	MPI4	MPI3	MPI2	MPI1	MPI0
5B	R/W	MPD7	MPD6	MPD5	MPD4	MPD3	MPD2	MPD1	MPD0

Notes:
1. R/W=Read/Write; W=Write-only. Unused bits in used W locations should be set to 0.
2. See Note 2 of Counters table below for description of similar method of operation. However, verification of a write operation requires two read operations immediately following it, with the result of the first read operation being disregarded.

SESSION ADDRESS MPI(5-0) IN HEX

Session #	Address (Hex)
0	00
• • •	• • •
63	3F

COUNTERS READ/WRITE CONTROL REGISTERS

Address (Hex)	Mode[1]	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
5C	W	CRW	Unused		CADD4	CADD3	CADD2	CADD1	CADD0
5D	R/W	CB23	CB22	CB21	CB20	CB19	CB18	CB17	CB16
5E	R/W	CB15	CB14	CB13	CB12	CB11	CB10	CB9	CB8
5F	R/W	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0

Notes:
1. Mode W = Write-only; R/W = Read/Write. Unused bits in used W locations should be set to 0.
2. Reading and writing of any of the three cell-counters for each channel (18 total) is performed through the Counter Read/Write Control registers. To read a counter, first write register 5CH with CRW=1 and CADD(4-0) set to the address code of the desired counter, taken from the following table. This will place the 24-bit count in registers 5DH-5FH, from which it may be read. To write to a counter, first write the 24-bit count value into registers 5DH-5FH, then write register 5CH with CRW=0 and CADD(4-0) set to the address code of the desired counter, taken from the following table.

COUNTERS ADDRESS CADD(4-0) IN HEX

Channel	1	2	3	4	5	6
Discarded Cell Counter	06	05	04	03	02	01
Received Cell Counter	0C	0B	0A	09	08	07
Transmitted Cell Counter	12	11	10	0F	0E	0D

Note: CADD0 is the LSB. Example - Received Cell Counter for Channel 2 is 0BH, CADD(4-0) = 0 1011.

MEMORY MAP DESCRIPTIONS

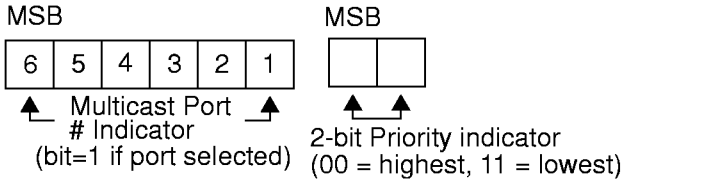
Note: The LSB of a multi-bit field within a register is the lowest-numbered bit, unless otherwise indicated.

CONTROL BITS

Configuration and Control Registers

Address (Hex)	Bit	Symbol	Description	
			Bit Equal to 1 (High)	Bit Equal to 0 (Low)
00	7-0	SRST	**Software Reset:** 91 (Hex) written to this location for a minimum of 200 ns will reset all lines and status registers. Configuration registers are not cleared. Global configuration bits that were changed before reset will be inserted during reset. Normal operation commences when any other value is written.	
01	7	XRAM	**External SRAM:** A cell input to the UTOPIA transmit interface is first stored in the external SRAM, then sent to the internal RAM before being sent as output on the line.	A cell input to the UTOPIA transmit interface is stored only in the internal RAM before being sent as output on the line. No external SRAM is used.
	6	U1	**UTOPIA Mode:** single-PHY UTOPIA	multi-PHY UTOPIA
	5	MCAST	**Multicast:** multicast function is enabled for transmitted cells and the inband multiport indicator is controlled by TINBAND for single- or multi-PHY.	Unicast is enabled. For single-PHY, the inband port indicator is controlled by TINBAND. For multi-PHY, the port indicator is coded in the TxADD(4-0) pins.
	4	4Q	**4 Priority Queues:** The transmitted cells are stored in 4 priority queues per port. The minimum numbers of cell buffer blocks provided are set by the four MINLPij nibbles.	One queue per port. The minimum number of cell buffer blocks provided is set by the 6 LSBs of the byte MINLP which is formed by MINLP11 and MINLP10.
	3	INVFRAQ	**Invert FRAQn pins:** The $\overline{\text{FrAqn}}$ output pins are changed to active high, i.e., FrAqn.	The $\overline{\text{FrAqn}}$ output pins are active low.
	2	FALL	**Falling Edge:** Line signals are sampled on the falling edge of RXCKn.	Line signals are sampled on the rising edge of RXCKn.
	1	TTP	**Transmit Test Pattern:** Line signals are sent with the test pattern stored in TESTPAT(7-0)	Normal line transmission
	0	DROPCELL	**Drop Cell:** Transmitted cell received from UTOPIA interface is dropped if the corresponding line buffer is full when the cell is ready to be transferred from the UTOPIA cell buffer to the line buffer.	No new transmitted cell is admitted from the UTOPIA interface if the number of cells destined to the corresponding line reaches the line buffer limit.

Address (Hex)	Bit	Symbol	Description	
			Bit Equal to 1 (High)	Bit Equal to 0 (Low)
02	7	IPOS	**Interrupt on Positive:** An interrupt output signal INTER is generated at the start (rising edge) of an event status bit.	Event start will not generate an interrupt.
	6	INEG	**Interrupt on Negative:** An interrupt output signal INTER is generated at the end (falling edge) of an event status bit.	Event end will not generate an interrupt.
	5	INVPOLI	**Interrupt Polarity Inversion:** Polarity of INTER output pin is inverted to active low for Intel and active high for Motorola.	Normal interrupt polarity of output pin INTER: active high for Intel, active low for Motorola.
	4-0		Set to 0.	
03	7	8KEN	**8 kHz Marker Enable:** 8 kHz timing marker is sent as output on the transmit lines.	No timing marker is sent as output.
	6	EXT8K	**External 8 kHz:** The 8 kHz timing is sourced from the 8k_In/1k_Out input pin.	The 8 kHz timing is sourced internally and a 1 kHz clock is provided as output on the 8k_In/1k_Out pin.
	5	NTDAT	**Negative Transmit Data Rail:** The TXCKn/$\overline{\text{TXDn}}$ output pins are configured as $\overline{\text{TXDn}}$ (negative data rail).	The TXCKn/$\overline{\text{TXDn}}$ output pins are configured as TXCKn (transmit line clock output).
	4	NRZ	**NRZ:** Line Input and output data is NRZ; NRZI/NRZ conversion is bypassed in both directions.	Line input and output data is NRZI; NRZI is converted to and from NRZ.
	3-0	XCODE	**XOFF Code:** This code is sent in the four GFC bit positions of the line output as the XOFF code, if enabled. Bit 3 is the first bit sent.	
04	7	TXEN6	**TX Enable:** Ch. 6 transmit block is enabled.	Ch. 6 transmit block is held in reset after completion of the current cell cycle.
	6	RXEN6	**RX Enable:** Ch. 6 receive block is enabled.	Ch. 6 receive block is held in reset after completion of the current cell cycle.
	5	XOFF6	**XOFF for Line 6:** XCODE is transmitted in 4 GFC bits for line 6.	0000 is transmitted in 4 GFC bits for line 6.
	4-0	ADD6(4-0)	**Address for Line 6:** 5-bit UTOPIA Level II address set for line 6.	
05	7 6 5 4-0	TXEN5 RXEN5 XOFF5 ADD5(4-0)	Channel 5 control bits, corresponding to those defined for Channel 6 in register 04H.	

Address (Hex)	Bit	Symbol	Description	
			Bit Equal to 1 (High)	Bit Equal to 0 (Low)
06	7 6 5 4-0	TXEN4 RXEN4 XOFF4 ADD4(4-0)	Channel 4 control bits, corresponding to those defined for Channel 6 in register 04H.	
07	7 6 5 4-0	TXEN3 RXEN3 XOFF3 ADD3(4-0)	Channel 3 control bits, corresponding to those defined for Channel 6 in register 04H.	
08	7 6 5 4-0	TXEN2 RXEN2 XOFF2 ADD2(4-0)	Channel 2 control bits, corresponding to those defined for Channel 6 in register 04H.	
09	7 6 5 4-0	TXEN1 RXEN1 XOFF1 ADD1(4-0)	Channel 1 control bits, corresponding to those defined for Channel 6 in register 04H.	
0A	7-6		Set to 0.	
	5	4K	**4K External FIFO:** Uses two 128k x 8 external SRAMs to provide 4K cell FIFO if XRAM is set to 1.	Uses one 64k x 16 external SRAM to provide 2K cell FIFO if XRAM is set to 1.
	4-3	RINBAND	**Received Port Address Location:** Sets inband port address transport mode in received cell if U1 is set to 1: 00 = 4 LSBs of the port address inserted in GFC bits 01 = 4 LSBs of the port address inserted in 4 MSBs of the HEC byte 10 = 3 LSBs of the port address inserted in VPI 7:5 bits 11 = 3 LSBs of the port address inserted in VPI 4:2 bits.	
	2-0	TINBAND	 **Multicast & Priority Indicator Byte In the Transmitted Cell** **TINBAND:** controls which bytes are used to carry the port ID, the multi-port and priority queue information in the transmitted cell: TINBAND — BYTE USED FOR MULTICAST & PRIORITY 000 — MC-6 = LSB MS Tag, PRI-2 = LSB LS Tag 001 — HEC Byte (MC-6 = MSB, PRI-2 = LSB) 010 — VPI7:5 is the port ID, no PRI-2 011 — MC-6 = VPI7:2, PRI-2 = VCI15:14 100 — GFC/VPI Byte (MC-6 = MSB, PRI-2 = LSB) others — future use	
0B	7-0	TESTPAT (7-0)	**Test Pattern:** Eight-bit test pattern which is sent as output on all six lines, MSB first, if TTP is set to 1.	

Address (Hex)	Bit	Symbol	Description	
			Bit Equal to 1 (High)	Bit Equal to 0 (Low)
0C	7-0	LINKRES	**Cell Buffers Reserved for Linked Lists:** This number is used internally and should be set to the following value: [3 x (MINLP11 + MINLP10 + MINLP01 + MINLP00)] if 4Q is set to 1, or 3 x MINLP if 4Q is set to 0.	
0D	7-4	MINLP/ MINLP11	If 4Q=1, MINLP11 and MINLP10 are 1/4 of the minimum cell buffer size reserved for links with priority 11 and 10 respectively. These nibbles can be set from 0 to 14. If 4Q=0, these 2 nibbles are combined as a byte (MINLP) setting the minimum buffer size for all 6 channel queues. The MINLP byte can be set from 0 to 63, using bits 5-0.	
	3-0	MINLP/ MINLP10		
0E	7-4	MINLP01	If 4Q=1, this is 1/4 of the minimum cell buffer size reserved for links with priority 01. This nibble is not used if 4Q=0. It can be set from 0 to 14.	
	3-0	MINLP00	If 4Q=1, this is 1/4 of the minimum cell buffer size reserved for links with priority 00. This nibble is not used if 4Q=0. It can be set from 0 to 14.	
0F	7-0		Set to 0.	

STATUS AND EVENT BITS

Status Registers

Address (Hex)	Bit	Symbol	Description	Conditions	
				Enter (to 1)	Exit (to 0)
31, 34, 37, 3A, 3D, 40 (n=6, 5, 4, 3, 2, 1)	7-6	Unused			
	5	DROPCn (n = 6-1)	Dropped a cell received for transmission on line n.	Cell received for corresponding line from UTOPIA was dropped.	This status indication is a pulse to 1 that lasts for 1 clock cycle.
	4	ROTOn (n = 6-1)	Received a cell on "transmitter off" line n.	Received cell on channel with the transmitter turned off on corresponding line.	This status indication is a pulse to 1 that lasts for 1 clock cycle.
	3	5BCODEn (n = 6-1)	Received a 5B code error on line n.	Received an illegal 5B code on corresponding line.	Received a legal 5B code on corresponding line.
	2	RBFULn (n = 6-1)	Receive buffer is full for line n.	The last cell receive buffer for the corresponding line is being filled i.e., after receiving the correct HEC.	At least 2 cell spaces are available in the receive buffer for the corresponding line.
	1	RHECEn (n = 6-1)	Received bad cell has been discarded for line n.	Received cell with HEC error on the corresponding line.	Received cell with correct HEC
	0	FREQEn (n = 6-1)	Frequency error on receive line n.	RXCKn is out of sync. with TxOSC.	RXCKn is in sync. with TxOSC.

Event Registers

Address (Hex)	Bit	Symbol	Description	Conditions	
				Enter (to 1)	Exit (to 0)
30	7-6	Unused	Disregard		
	5-0	CHERRn (n = 6-1)	Common Mode Error Indication for Ch. n	Any of the six events is set to 1 for the corresponding channel event register (see the following address).	Cleared to 0 when the corresponding event register is read by the microprocessor.
32, 35, 38, 3B, 3E, 41 (n=6, 5, 4, 3, 2, 1)	7-6	Unused	Disregard		
	5	DROPCn (n = 6-1)	Dropped a cell received for transmission on line n.	When the corresponding status bit in address 31, 34, 37, 3A, 3D or 40 changes from 0 to 1 if IPOS is set, and/or from 1 to 0 if INEG is set.	Cleared to 0 when read by the microprocessor.
	4	ROTOn (n = 6-1)	Received a cell on "transmitter off" line n.		
	3	5BCODEn (n = 6-1)	Received a 5B code error on line n.		
	2	RBFULn (n = 6-1)	Receive buffer is full for line n.		
	1	RHECEn (n = 6-1)	Received bad cell has been discarded for line n.		
	0	FREQEn (n = 6-1)	Frequency error on receive line n.		

Interrupt Mask Bits

Address (Hex)	Bit	Symbol	Description	
			Bit Equal to 1 (High)	Bit Equal to 0 (Low)
33, 36, 39, 3C, 3F, 42 (n=6, 5, 4, 3, 2, 1)	7-6	Unused	Set to 0.	
	5	DROPCn	No interrupt is generated on pin INTER when this event bit is set to 1 for the corresponding line (see addresses 32, 35, 38, 3B, 3E and 41).	An interrupt is generated on pin INTER when this event bit is set to 1 for the corresponding line (see addresses 32, 35, 38, 3B, 3E and 41).
	4	ROTOn		
	3	5BCODEn		
	2	RBFULn		
	1	RHECEn		
	0	FREQEn		
45	7-1		Set to 0.	
	0		**Set to 1.**	
48	7-0		Set to 0.	

Serial Port and External Device Control Registers

Address	Bit	Symbol	Description
10	7-3	Unused	Set to 0.
	2-0	LN(2-0)	**Line Number:** These bits select the line interface number (m = 0 - 5) for which the read/write operations are to occur. LN0 is the LSB. Only line numbers 000 to 101 are valid and they correspond to pins $\overline{\text{LENA0}}$ to $\overline{\text{LENA5}}$ respectively. Line numbers 110 and 111 are interpreted as 101. Writing to this location enables the corresponding $\overline{\text{LENAm}}$ pin by setting it to low, and activates the serial port read/write operation for line n = m + 1 (e.g., 000 for line 1).
11	7	LRW	**Line Control Read/Write:** Writing a 1 to this bit enables a read operation on the selected serial line control interface. Writing a 0 to this bit enables a write operation on the selected serial line control interface. This is the first bit shifted out on the serial port.
11 12	6-0 7-0	LRA(14-8) LRA(7-0)	**Line Register Address:** These fifteen bits provide the register address in the line interface device selected by LN(2-0) to which read/write operations will occur. These bits are shifted out MSB (LRA14) first.
13 14	7-0 7-0	LS(15-8) LS(7-0)	**Line Scan:** After a read operation from the selected line interface device, these sixteen bits provide the data read from the serial line interface device, with the first bit in the MSB (LS15).
15 16	7-0 7-0	LD(15-8) LD(7-0)	**Line Data:** These sixteen bits provide the data that is to be written to the selected line interface, with the first bit in the MSB (LD15).
17	7-1	Unused	Set to 0.
	0	LSTATUS	**Line Status:** LSTATUS = 1 indicates that the selected line interface is in use. LSTATUS = 0 indicates that the line interface operation has been completed. This bit may be used to avoid accessing any of the serial port registers at addresses 10H to 16H during an operation, which would cause an error.
18	7	Unused	Set to 0.
	6	INVTXO	**Invert Tx On:** When set to 1, this bit inverts the polarity of all six TXONn output pins.
	5-0	FTOFFn (n = 1 - 6)	**Force Tx Off:** Setting FTOFFn = 1 or setting TXENn = 0 sets the corresponding TXONn pin inactive. Setting FTOFFn = 0 and TXENn = 1 sets the corresponding TXONn pin active
19	7-6	Unused	Set to 0.
	5-0	FLBn (n = 6 - 1)	**Force Loopback:** 1 sets the corresponding LBn pin high, 0 sets it low.
1A, 1B, 1C	7-6	Unused	Set to 0.

<table>
<tr><th>Address</th><th>Bit</th><th>Symbol</th><th>Description</th></tr>
<tr><td>1A

1B

1C</td><td>5-3
2-0
5-3
2-0
5-3
2-0</td><td>LED6C(2-0)
LED5C(2-0)
LED4C(2-0)
LED3C(2-0)
LED2C(2-0)
LED1C(2-0)</td><td>LED Control Bits (2-0): Three control bits are provided for each LED for line n. They control the setting of the two data bits (RA and RC) sent out on the serial port that activate the lighting of the LEDs. The control settings and the corresponding data bit values are as follows:
<table>
<tr><th>LEDnC(2-0)</th><th>RA</th><th>RC</th><th>Condition and LED Color</th></tr>
<tr><td>000 (default)</td><td>0</td><td>1</td><td>Received or transmitted a cell on the port line. Port will output this data for a minimum of 50 ms (green).</td></tr>
<tr><td>000</td><td>0</td><td>0</td><td>No Tx or Rx cell (LED off).</td></tr>
<tr><td>001</td><td>0</td><td>1</td><td>Set by microproc. (green).</td></tr>
<tr><td>010</td><td>1</td><td>0</td><td>Set by microproc. (red).</td></tr>
<tr><td>011</td><td colspan="2">RA = D & RC = $\overline{D}$ oscillating at 1 kHz</td><td>Set by microproc. (yellow).</td></tr>
<tr><td>111</td><td colspan="2">RA = D & RC = $\overline{D}$ oscillating at 1 kHz and turned on/off at 3 Hz</td><td>Set by microprocessor (yellow, flashing at 3 Hz).</td></tr>
<tr><td>other</td><td>0</td><td>0</td><td>Set by microproc. (LED off).</td></tr>
</table></td></tr>
<tr><td>1D-2F</td><td>7-0</td><td>Unused</td><td>Disregard</td></tr>
</table>

Multicast Indicator Read/Write Control Registers

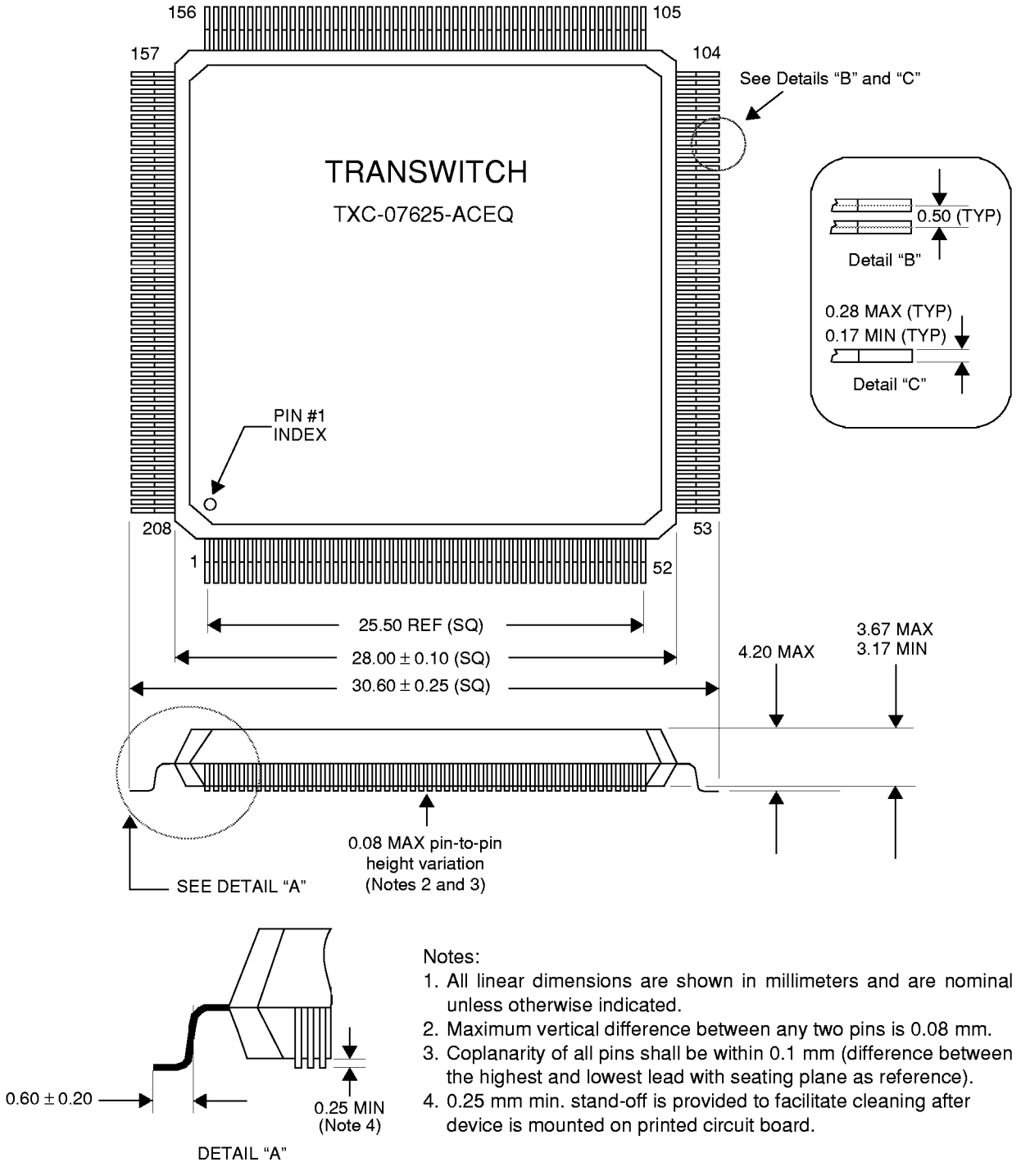
Address	Bit	Symbol	Description
59	7	MPRW	**Multi-port Read/Write:** Writing 1 to this bit results in a read operation on the addressed multicast multi-port indicator. Writing 0 to this bit results in a write operation on the addressed multicast multi-port indicator.
	6-0	Unused	Set to 0.
5A	7-6	Unused	Set to 0.
	5-0	MPI(5-0)	**Multi-Port Index:** These bits are the index address to the multi-port indicator.
5B	7-0	MPD(7-0)	**Multi-Port Data Bits (7-0):** Latched multi-port data. MPD0 is the LSB. These bits receive the data read from the address location designated by the index MPI(5-0) when a 1 is written into MPRW. These bits are written into the designated index address location when a 0 is written into MPRW.

COUNTERS READ/WRITE CONTROL REGISTERS

Address	Bit	Symbol	Description
5C	7	CRW	**Counter Control Read/Write:** Writing a 1 to this bit results in a read operation on the addressed counter. Writing a 0 to this bit results in a write operation on the addressed counter.
	6-5	Unused	Set to 0.
	4-0	CADD(4-0)	**Counter Address:** These five bits identify the counter address for which the read or write operation will occur. The valid addresses are 01H to 12H (1 to 18 decimal) as tabulated in the Memory Map section. Writing to an invalid address results in no operation, and reading from an invalid address retrieves the count from the most recently accessed counter.
5D 5E 5F	7-0 7-0 7-0	CB(23-16) CB(15-8) CB(7-0)	**Counter Bits (23-0):** For a read operation, these bits are the latched 24-bit counter value read from the counter designated by CADD(4-0) after writing a 1 in CRW. For a write operation, these bits are written into the 24-bit counter designated by CADD(4-0) when a 0 is written into CRW. CB0 is LSB of the counter.

PACKAGE INFORMATION

The SALI-25C device is available in a 208-pin plastic quad flat package (PQFP) suitable for surface mounting, as shown in Figure 29



Notes:
1. All linear dimensions are shown in millimeters and are nominal unless otherwise indicated.
2. Maximum vertical difference between any two pins is 0.08 mm.
3. Coplanarity of all pins shall be within 0.1 mm (difference between the highest and lowest lead with seating plane as reference).
4. 0.25 mm min. stand-off is provided to facilitate cleaning after device is mounted on printed circuit board.

Figure 29. SALI-25C TXC-07625 208-Pin Plastic Quad Flat Package

ORDERING INFORMATION

Part Number: TXC-07625-ACEQ 208-pin Plastic Quad Flat Package (PQFP)

RELATED PRODUCTS

TXC-05551, SARA-2 ATM Cell Processing IC Device. Used with application-specific microcode to perform complete segmentation and reassembly (SAR) for implementing ATM adapter cards, legacy LAN to ATM hubs, and routers. PCI-based host interface. Supports CBR, VBR and UBR services. Integrated SONET/SDH framer.

TXC-05801, CUBIT Device (ATM *CellBus* Bus Switch). Implements cost effective ATM multiplexing and switching systems, based on the 32-bit *CellBus* bus architecture. A single-chip solution, the CUBIT has the ability to send and also receive cells for control purposes over the same *CellBus* bus. *CellBus* bus technology works at aggregate rates of up to 1 gigabit per second and provides header translation, multiplexing, concentration and switching functions for a wide variety of small-to-medium size ATM systems. This device is not recommended for use in new designs, which should use CUBIT-*Pro.*

TXC-05802, CUBIT-*Pro* VLSI Device. A *CellBus* bus-based ATM cell switching device that supports unicast and multicast transfers, and has all necessary functions for implementing a switch: inlet queuing, cell address translation, cell routing, and outlet cell queuing. This is a derivative of the CUBIT device that has enhanced capabilities.

TXC-07025, ALI-25 VLSI Chip Set (ATM Line Interface). ALI-25C Controller and ALI-25T Transceiver devices together provide the complete ATM 25 Mbit/s physical layer function (TC, PMD) and operate over existing STP or UTP-3, 4, 5 cable plant.

STANDARDS DOCUMENTATION SOURCES

Telecommunication technical standards and reference documentation may be obtained from the following organizations:

ANSI (U.S.A.):

American National Standards Institute (ANSI)
11 West 42nd Street
New York, New York 10036

Tel: 212-642-4900
Fax: 212-302-1286

The ATM Forum (U.S.A.):

ATM Forum World Headquarters
303 Vintage Park Drive
Foster City, CA 94404-1138

Tel: 415-578-6860
Fax: 415-525-0182

ATM Forum European Office
14 Place Marie - Jeanne Bassot
Levallois Perret Cedex
92593 Paris France

Tel: 33 1 46 39 56 26
Fax: 33 1 46 39 56 99

Bellcore (U.S.A.):

Bellcore
Attention - Customer Service
8 Corporate Place
Piscataway, NJ 08854

Tel: 800-521-CORE (In U.S.A.)
Tel: 908-699-5800
Fax: 908-336-2559

EIA - Electronic Industries Association (U.S.A.):

Global Engineering Documents
Suite 407
7730 Carondelet Avenue
Clayton, MO 63105

Tel: 800-854-7179 (In U.S.A.)
Fax: 314-726-6418

ETSI (Europe):

European Telecommunications Standards Institute
ETSI, 06921 Sophia - Antipolis
Cedex France

Tel: 33 92 94 42 00
Fax: 33 93 65 47 16

ITU-T (International):

Publication Services of International Telecommunication Union (ITU)
Telecommunication Standardization Sector (T)
Place des Nations
CH 1211
Geneve 20, Switzerland

Tel: 41-22-730-5285
Fax: 41-22-730-5991

MIL-STD Military Standard (U.S.A.):

Standardization Documents Order Desk
700 Robbins Avenue
Building 4D
Philadelphia, PA 19111-5094

Tel: 212-697-1187
Fax: 215-697-2978

TTC (Japan):

TTC Standard Publishing Group of the
Telecommunications Technology Committee
2nd Floor, Hamamatsucho - Suzuki Building,
1 2-11, Hamamatsu-cho, Minato-ku, Tokyo

Tel: 81-3-3432-1551
Fax: 81-3-3432-1553

LIST OF DATA SHEET CHANGES

This change list identifies those areas within this updated SALI-25C Data Sheet that have significant differences relative to the previous and now superseded SALI-25C Data Sheet:

Updated SALI-25C Data Sheet: Edition 4, February 1999

Previous SALI-25C Data Sheet: Edition 3, January 1998

The page numbers indicated below of this updated Data Sheet include significant changes relative to the previous Data Sheet.

Page Number of Updated Data Sheet — **Summary of the Change**

All — Changed edition number and date.

1 — Changed fourth line under Line Interface heading in Features section. Changed copyright date from 1998 to 1999.

21 — Added first paragraph and moved first paragraph from top of page 22 to follow it.

24 — Changed Symbols marked next to pins in Figure 13 as follows:

Pin No.	From	To
103	NC	GND
104	GND	NC
108	NC	RESERVE-H
109	NC	RESERVE-H

The change of pins 108 and 109 from NC to RESERVE-H has been made to prevent faulty operation under some adverse operating conditions (please refer to Technical Bulletin TB-526, document number TXC--7625-TB1).

25 — In the Power Supply and Ground table, deleted pin 104 from GND row and added pin 103 to this row. Also deleted pins 103, 108 and 109 from NC row and added pin 104 to this row.

28 — In the Miscellaneous Pins table, added pins 108 and 109 to RESERVE-H row.

29 — Replaced text in Name/Function column for Symbol $\overline{TRS}$, pin 49.

51 — Changed Symbol from NC to RESERVE-H for Scan Cell No. 40 and 41, Pin No. 108 and 109.

71 — Replaced List of Data Sheet Changes section with content referring to Edition 4.

- NOTES -

- NOTES -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