Am95C71

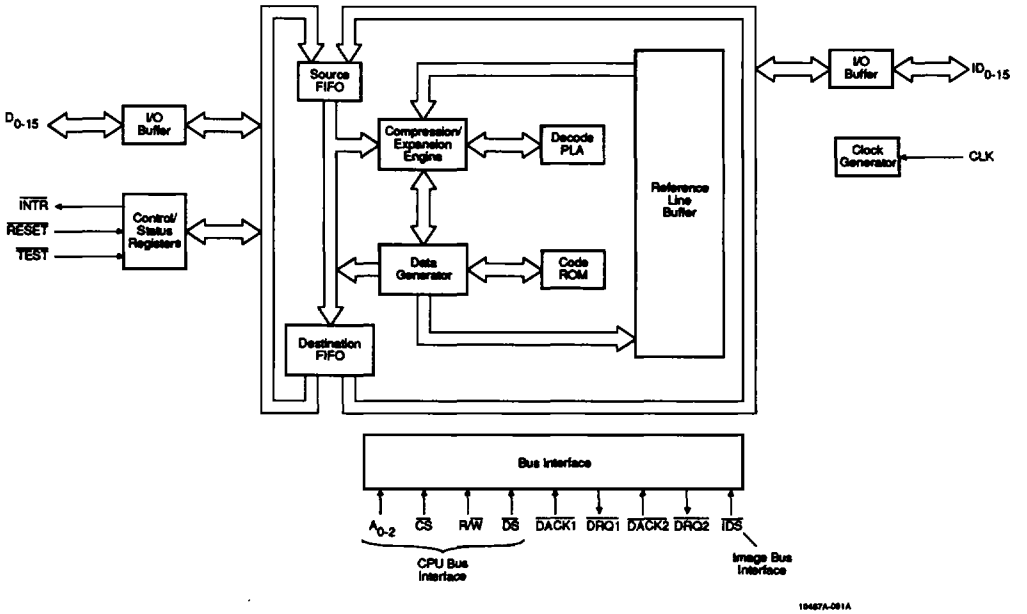
Video Compression/Expansion Processor (VCEP)

PRELIMINARY

DISTINCTIVE CHARACTERISTICS

- Throughput exceeding an average rate of 50 Mb/s when compressing or expanding
- Full CCITT Group 3 and Group 4 compression/expansion: allows MH, MR and MMR coding and transparent mode
- Dual-bus architecture with single-bus mode option
- Supports bit-boundary image width up to 8191 pixels in one-dimensional (1D) mode and 6911 pixels in two-dimensional (2D) mode
- Has on-chip 6911-pixel reference-line buffer allowing high-performance 2D coding
- Provides error detection and recovery capability
- Supports programmable k-Parameter for 2D coding
- 16-word FIFOs on input and output
- Half-duplex operation

BLOCK DIAGRAM



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GENERAL DESCRIPTION

The Am95C71 Video Compression/Expansion Processor (VCEP) is a high-performance CMOS processor which compresses and expands binary image data using the internationally standardized CCITT Group 3 and Group 4 algorithms.

The VCEP supports the Modified Huffman (MH), Modified Read (MR), and Modified-Modified Read (MMR) coding schemes used by the CCITT Groups 3 and 4 standards. MH coding is a one-dimensional technique which identifies and then codes run-lengths of black or white pixels. MR coding compresses a single scan line using MH coding, followed by k-1 scan lines coded in such a way as to reflect differences from the pixel patterns of the previous scan line (two-dimensional or 2D coding); the value of the k-Parameter is defined by the user and will generally be set to a larger number on communication links with lower bit-error rates.

MMR coding is a full 2D-coding scheme which uses an all-white imaginary reference line when coding the first scan line. All lines on the page are coded two-dimensionally. For a typical binary image, MMR coding offers the best compression, followed by MR and then MH. Compressed data may be corrupted during transmission or storage. Error-free (or error-protected) transmission media are used with Group 4 coding, since error recovery is not possible. The CCITT standard refers to MH and MR coding as Group 3 techniques and MMR coding as a Group 4 technique. Group 3 error recovery facility is provided on the VCEP.

The extent of data compression provided by Group 3 and Group 4 compression techniques depends on the specific data patterns contained in the image. Typically, an originally black-or-white (binary) image will yield compression ratios between 5:1 and 50:1, whereas a binary image produced from a grey-scale or color original may compress poorly, even resulting in a compressed file larger than the raw image. Alternatively, the user may program the VCEP into transparent mode where data is simply passed from source FIFO to destination FIFO without compressing or modifying the data.

When 2D (MR or MMR) coding is performed, the previous scan line is used as a reference to code the current line. To significantly increase performance the VCEP stores the reference line in an on-chip buffer.

The VCEP is a slave-mode device with two 16-bit bus interfaces. The user may select either bus to be source or destination and the VCEP to compress, expand or pass through (transparent mode) data. Data is buffered on input and output by 16-word FIFOs. The VCEP, therefore, may be used as a single-bus or dual-bus device, with FIFO buffers on input and output.

The VCEP may either compress, expand, or pass through data; it cannot do these functions simultaneously or in a multiplexed fashion and is therefore termed a half-duplex device.

However, it is possible for the VCEP to multiplex data compression from several sources if a full scan line is processed from each source, and MH coding is selected. Multiplexed expansion is not supported.

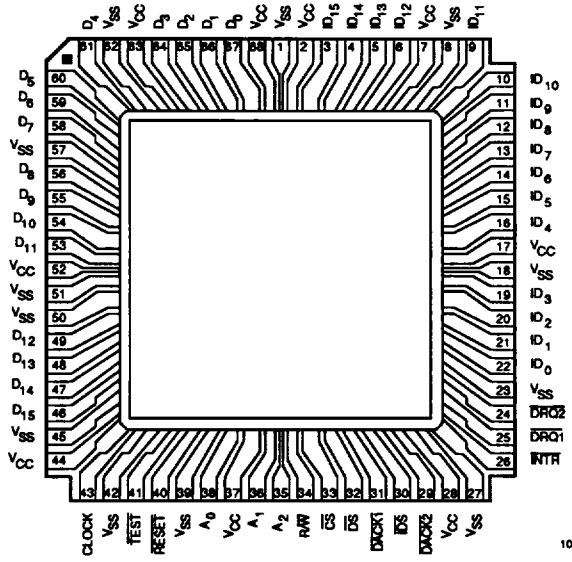
The VCEP has several mechanisms to detect data errors on expansion. For MH and MR modes, if the expanded scan line is longer or shorter than the user-programmed length, the VCEP sets a flag and halts. Illegal codes, negative run lengths in 2D coding, and other illegal fields are detected as errors. Since the VCEP has no on-chip DMA, the host CPU is responsible for error recovery; for example, by replicating the previous scan line when an error is found in the current scan line.

The VCEP has programmable bus burst and dwell counters to allow the user control over the length of the VCEP's data requests and the time between requests.

All registers on the VCEP are set up by the CPU via the VCEP's CPU bus, selecting specific registers with three address lines. In the dual-bus configuration, data is accessed on the Image bus by a slave-mode access which does not require an address.

CONNECTION DIAGRAMS
Top View

LCC



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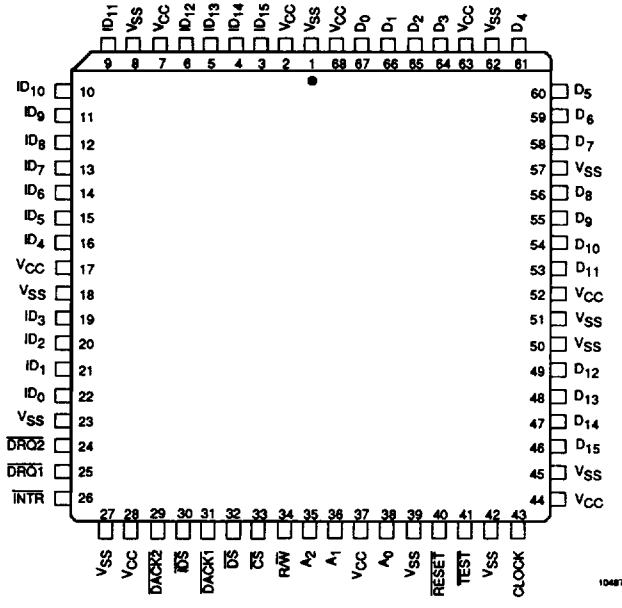
PLCC



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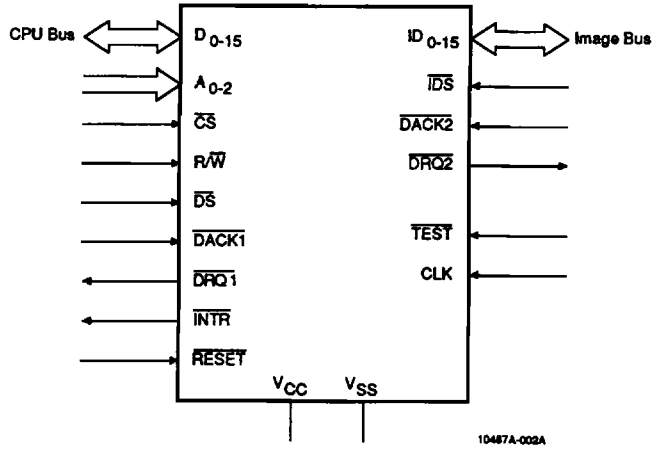
Note: Pin 1 is marked for orientation.

LOGIC SYMBOL



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ORDERING INFORMATION

Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of: **a. Device Number**
b. Speed Option (if applicable)
c. Package Type
d. Temperature Range
e. Optional Processing

AM95C71 -20 J C

e. OPTIONAL PROCESSING
Blank = Standard processing

d. TEMPERATURE RANGE
C = Commercial (0 to +70°C)

c. PACKAGE TYPE
J = 68-Pin Plastic Leaded Chip Carrier (PL 068)
L = 68-Pin Ceramic Leadless Chip Carrier (CA2068)

b. SPEED OPTION
-20 = 20 MHz
-16 = 16 MHz

a. DEVICE NUMBER/DESCRIPTION
Am95C71
Video Compression/Expansion Processor (VCEP)

Valid Combinations	
AM95C71-20	JC, LC
AM95C71-16	

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released combinations, and to obtain additional data on AMD's standard military grade products.