CY7C185A
CY7C186A

CYPRESS SEMICONDUCTOR

8,192 x 8 Static R/W RAM

2

Features

- **Automatic power-down when deselected**
- **CMOS for optimum speed/power**
- **High speed**
  - **20 ns**
- **Low active power**
  - **688 mW**
- **Low standby Power**
  - **220 mW**
- **TTL-compatible imputs and outputs**
- **Capable of withstanding greater than 2001V electrostatic discharge**

Functional Description

The CY7C185A and CY7C186A are high-performance CMOS static RAMs organized as 8192 words by 8 bits. Easy memory expansion is provided by an active LOW chip enable ($\overline{CE_1}$), an active HIGH chip enable (CE_2), an active LOW output enable ($\overline{OE}$), and three-state drivers. Both devices have an automatic power-down feature ($\overline{CE_1}$), reducing the power consumption by 68% when deselected. The CY7C185A is in the space saving 300-mil-wide DIP package and leadless chip carrier. The CY7C186A is in the standard 600-mil-wide package.

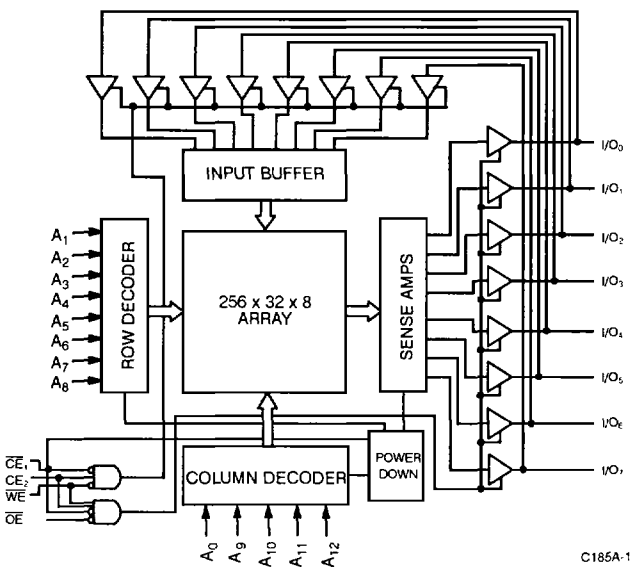
Writing to the device is accomplished when the chip enable one ($\overline{CE_1}$) and write enable ($\overline{WE}$) inputs are both LOW, and the chip enable two (CE_2) input is HIGH. Data on the eight I/O pins (I/O_0 through I/O_7) is written into the memory location specified on the address pins (A_0 through A_{12}).

Reading the device is accomplished by taking chip enable one ($\overline{CE_1}$) and output enable ($\overline{OE}$) LOW, while taking write enable ($\overline{WE}$) and chip enable two (CE_2) HIGH. Under these conditions, the contents of the memory location specified on the address pins will appear on the I/O pins.

The I/O pins remain in high-impedance state when chip enable one ($\overline{CE_1}$) or output enable ($\overline{OE}$) is HIGH, or write enable ($\overline{WE}$) or chip enable two (CE_2) is LOW.

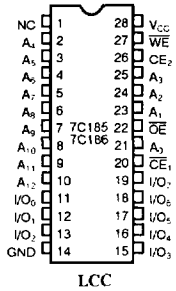
A die coat is used to insure alpha immunity.

Logic Block Diagram

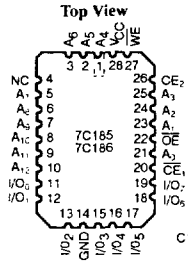


Pin Configurations

DIP/SOJ
Top View



LCC
Top View



Selection Guide

		7C185A-20 7C186A-20	7C185A-25 7C186A-25	7C185A-35 7C186A-35	7C185A-45 7C186A-45	7C185A-55 7C186A-55
Maximum Access Time (ns)		20	25	35	45	55
Maximum Operating Current (mA)	Commercial	125	125	125	125	125
	Military	135	125	125	125	125
Maximum Standby Current (mA)	Commercial	40/20	30/20	30/20	30/20	30/20
	Military	40/20	40/20	30/20	30/20	30/20

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... – 65°C to + 150°C

Ambient Temperature with Power Applied ..... – 55°C to + 125°C

Supply Voltage to Ground Potential (Pin 28 to Pin 14) ..... – 0.5V to + 7.0V

DC Voltage Applied to Outputs in High Z State ..... – 0.5V to + 7.0V

DC Input Voltage ..... – 3.0V to + 7.0V

Output Current into Outputs (Low) ..... 20 mA

Static Discharge Voltage ..... > 2001V (per MIL-STD-883, Method 3015)

Latch-Up Current ..... > 200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to + 70°C	5V ± 10%
Military[1]	– 55°C to + 125°C	5V ± 10%

Electrical Characteristics Over the Operating Range[2]

Parameters	Description	Test Conditions		7C185A-20 7C186A-20 Min.	7C185A-20 7C186A-20 Max.	7C185A-25 7C186A-25 Min.	7C185A-25 7C186A-25 Max.	7C185A-35,45,55 7C186A-35,45,55 Min.	7C185A-35,45,55 7C186A-35,45,55 Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = – 4.0 mA		2.4		2.4		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8.0 mA			0.4		0.4		0.4	V
V_{IH}	Input HIGH Voltage			2.2	V_{CC}	2.2	V_{CC}	2.2	V_{CC}	V
V_{IL}	Input LOW Voltage[3]			–3.0	0.8	–3.0	0.8	–3.0	0.8	V
I_{IX}	Input Load Current	GND ≤ V_I ≤ V_{CC}		–10	+ 10	–10	+ 10	–10	+ 10	µA
I_{OZ}	Output Leakage Current	GND ≤ V_I ≤ V_{CC}, Output Disabled		–10	+ 10	–10	+ 10	–10	+ 10	µA
I_{OS}	Output Short Circuit Current[4]	V_{CC} = Max., V_{OUT} = GND			–300		–300		–300	mA
I_{CC}	V_{CC} Operating Supply Current	V_{CC} = Max. I_{OUT} = 0 mA	Com'l		125		125		125	mA
			Mil		135		125		125	mA
I_{SB1}	Automatic $\overline{CE}_1$ Power-Down Current	Max. V_{CC}, $\overline{CE}_1$ ≥ V_{IH}, Min. Duty Cycle = 100%	Com'l		40		30		30	mA
			Mil		40		40		30	mA
I_{SB2}	Automatic $\overline{CE}_1$ Power-Down Current	Max. V_{CC}, $\overline{CE}_1$ ≥ V_{CC} –0.3V V_{IN} ≥ V_{CC} –0.3V or V_{IN} ≥ 0.3V	Com'l		20		20		20	mA
			Mil		20		20		20	mA

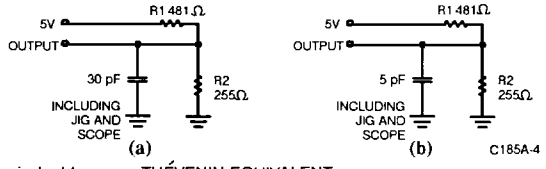
Capacitance[5]

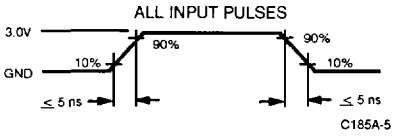
Parameters	Description	Test Conditions	Max.	Units
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	10	pF
C_{OUT}	Output Capacitance		10	pF

Notes:

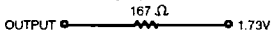
1. T_A is the "instant on" case temperature.
2. See the last page of this specification for Group A subgroup testing information.
3. V_{IL} (min.) = – 3.0V for pulse durations less than 30 ns.
4. Not more than 1 output should be shorted at one time. Duration of the short circuit should not exceed 30 seconds.
5. Tested initially and after any design or process changes that may affect these parameters.
6. Test conditions assume signal transition time of 5 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified I_{OL}/I_{OH} and 30-pF load capacitance.
7. t_{HZOE}, t_{HZCE}, and t_{HZWE} are specified with C_L = 5 pF as in part (b) of AC Test Loads. Transition is measured ± 500 mV from steady state voltage.
8. At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE} for any given device.
9. Device is continuously selected. $\overline{OE}$, $\overline{CE}$ = V_{IL}, CE_2 = V_{IH}
10. Address valid prior to or coincident with $\overline{CE}$ transition low.
11. $\overline{WE}$ is HIGH for read cycle.
12. The internal write time of the memory is defined by the overlap of $\overline{CE}_1$ LOW, CE_2 HIGH, and $\overline{WE}$ LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.
13. Data I/O is high impedance if $\overline{OE}$ = V_{IH}.
14. If $\overline{CE}$ goes HIGH simultaneously with $\overline{WE}$ HIGH, the output remains in a high-impedance state.

AC Test Loads and Waveforms





Equivalent to: THÉVENIN EQUIVALENT

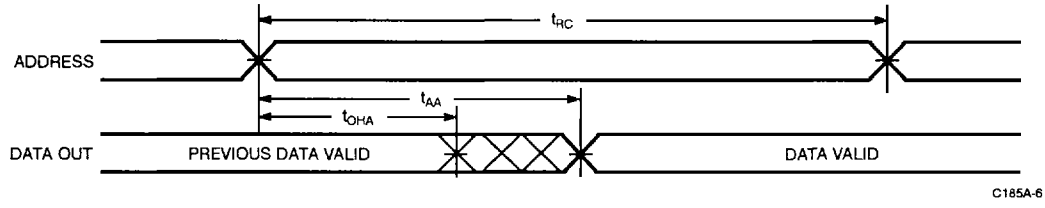


Switching Characteristics Over the Operating Range[2,6]

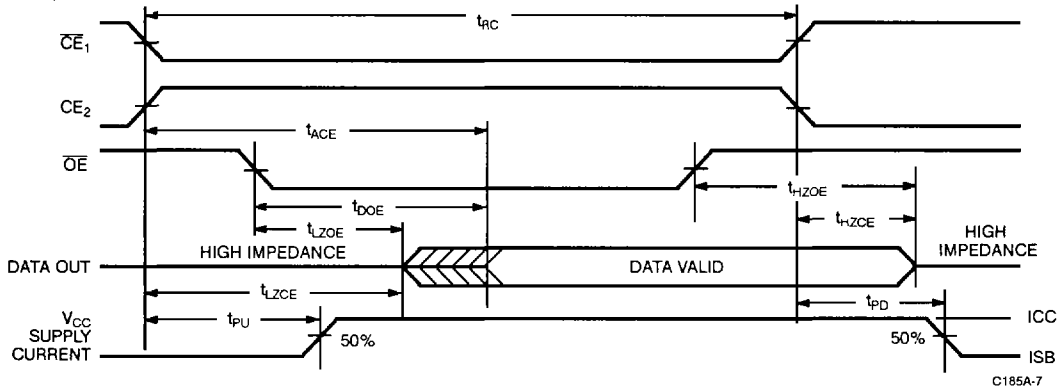
Parameters	Description	7C185A-20 7C186A-20		7C185A-25 7C186A-25		7C185A-35 7C186A-35		7C185A-45 7C186A-45		7C185A-55 7C186A-55		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE												
t_{RC}	Read Cycle Time	20		25		35		45		55		ns
t_{AA}	Address to Data Valid		20		25		35		45		55	ns
t_{OHA}	Data Hold from Address Change	3		3		3		3		3		ns
t_{ACE1}	$\overline{CE}_1$ LOW to Data Valid		20		25		35		45		55	ns
t_{ACE2}	CE_2 HIGH to Data Valid		20		25		25		30		40	ns
t_{DOE}	$\overline{OE}$ LOW to Data Valid		10		12		15		20		25	ns
t_{LZOE}	$\overline{OE}$ LOW to Low Z	3		3		3		3		3		ns
t_{HZOE}	$\overline{OE}$ HIGH to High Z[7]		8		10		12		15		20	ns
t_{LZCE1}	$\overline{CE}_1$ LOW to Low Z[8]	5		5		5		5		5		ns
t_{LZCE2}	CE_2 HIGH to Low Z	3		3		3		3		3		ns
t_{HZCE}	$\overline{CE}_1$ HIGH to High Z[7, 8] CE_2 LOW to High Z		8		10		15		15		20	ns
t_{PU}	$\overline{CE}_1$ LOW to Power-Up	0		0		0		0		0		ns
t_{PD}	$\overline{CE}_1$ HIGH to Power-Down		20		20		20		25		25	ns
WRITE CYCLE[9]												
t_{WC}	Write Cycle Time	20		20		25		40		50		ns
t_{SCE1}	$\overline{CE}_1$ LOW to Write End	15		20		25		30		40		ns
t_{SCE2}	CE_2 HIGH to Write End	15		20		20		25		30		ns
t_{AW}	Address Set-Up to Write End	15		20		25		30		40		ns
t_{HA}	Address Hold from Write End	0		0		0		0		0		ns
t_{SA}	Address Set-Up to Write Start	0		0		0		0		0		ns
t_{PWE}	$\overline{WE}$ Pulse Width	15		15		20		20		25		ns
t_{SD}	Data Set-Up to Write End	10		10		15		15		25		ns
t_{HD}	Data Hold from Write End	0		0		0		0		0		ns
t_{HZWE}	$\overline{WE}$ LOW to High Z[7]		7		7		10		15		20	ns
t_{LZWE}	$\overline{WE}$ HIGH to Low Z	5		5		5		5		5		ns

Switching Waveforms

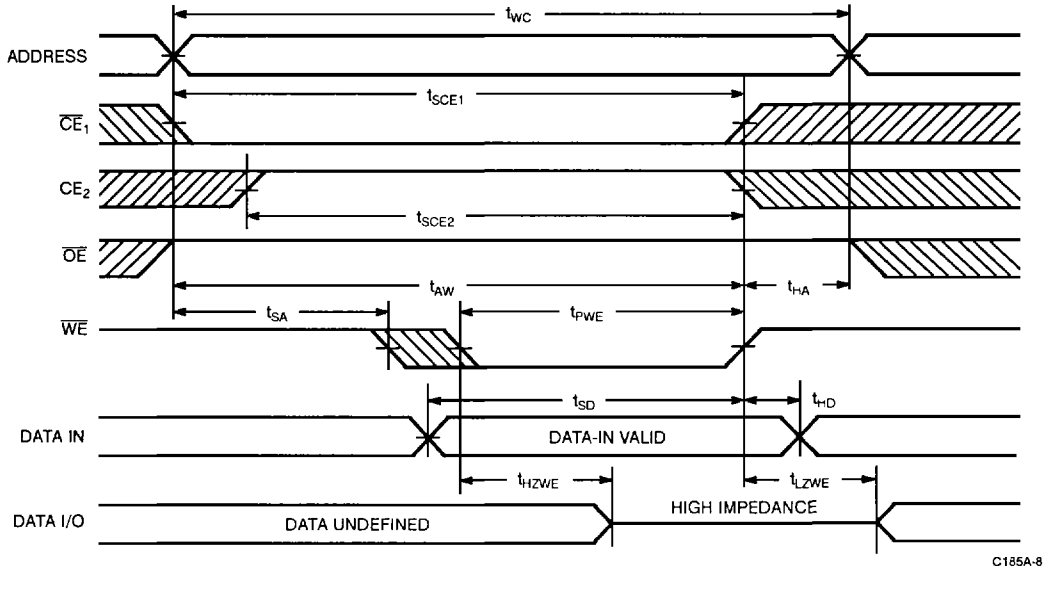
Read Cycle No. 1 [9, 10]



Read Cycle No. 2 [10, 11]

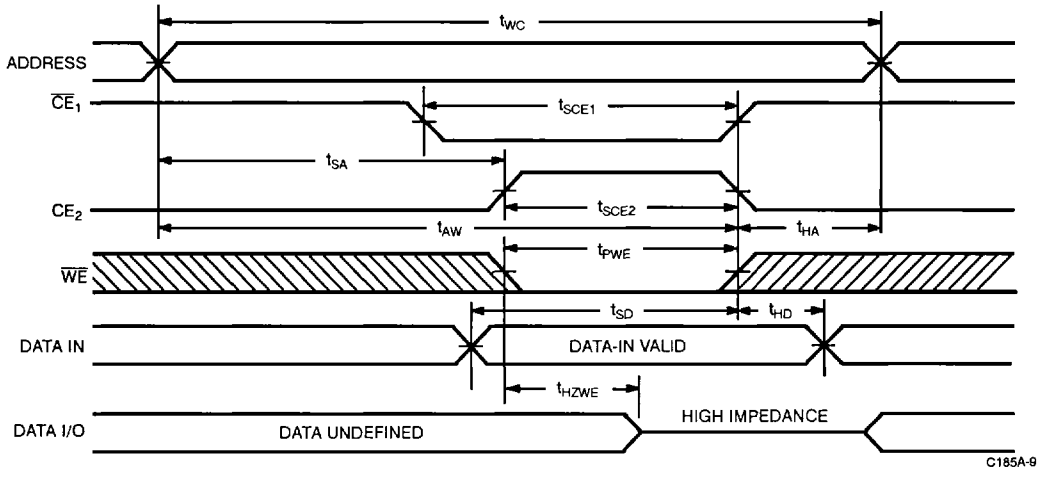


Write Cycle No. 1 ($\overline{WE}$ Controlled) [12, 13]

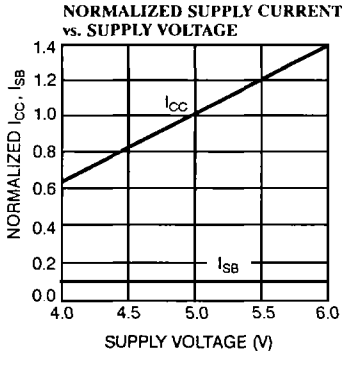


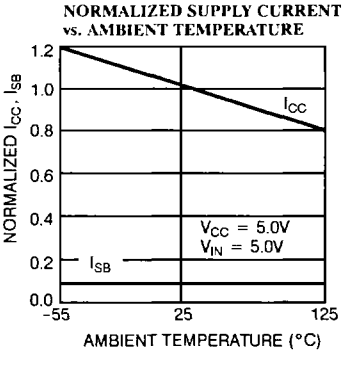
Switching Waveforms (continued)

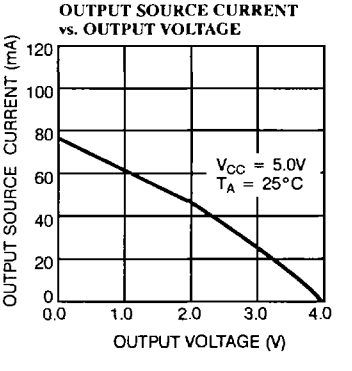
Write Cycle No. 2 ($\overline{CE}$ Controlled) [12, 13, 14]

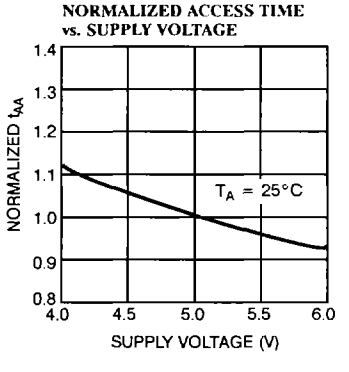


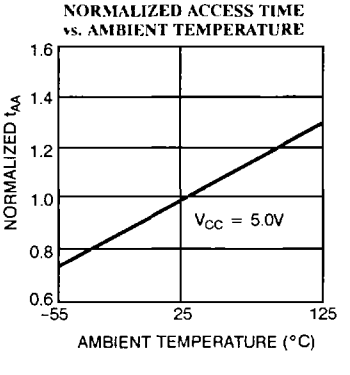
Typical DC and AC Characteristics

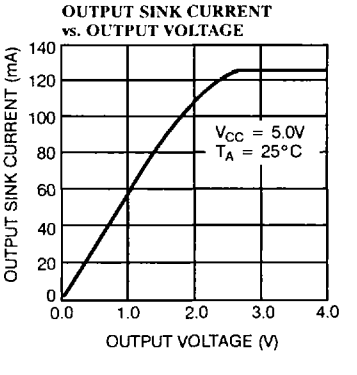




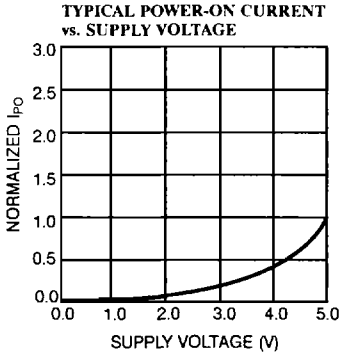


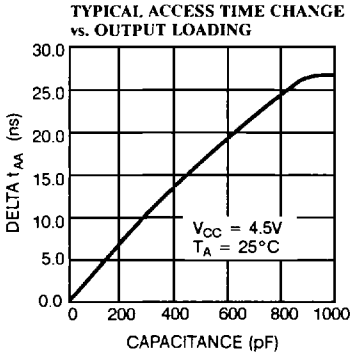


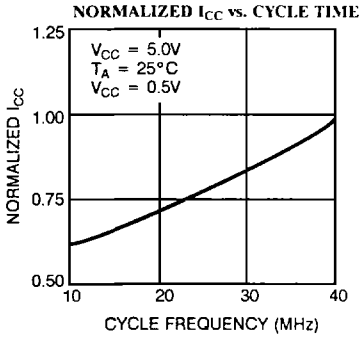




Typical DC and AC Characteristics (continued)







Truth Table

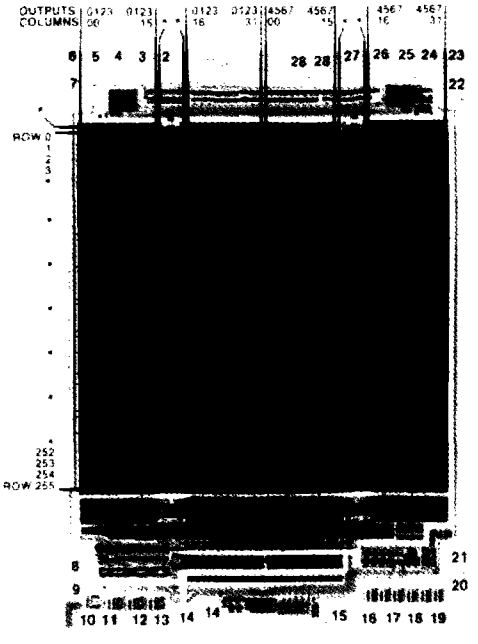
$\overline{CE}_1$	CE_2	$\overline{WE}$	$\overline{OE}$	Inputs/Outputs	Mode
H	X	X	X	High Z	Deselect/Power-Down
X	L	X	X	High Z	Deselect
L	H	H	L	Data Out	Read
L	H	L	X	Data In	Write
L	H	H	H	High Z	Deselect

Ordering Information

Speed (ns)	Ordering Code	Package Type	Operating Range
20	CY7C185A-20PC	P21	Commercial
	CY7C185A-20VC	V21	
	CY7C185A-20DC	D22	
	CY7C185A-20LC	L54	
	CY7C185A-20DMB	D22	Military
	CY7C185A-20LMB	L54	
	CY7C185A-20KMB	K74	
25	CY7C185A-25PC	P21	Commercial
	CY7C185A-25VC	V21	
	CY7C185A-25DC	D22	
	CY7C185A-25LC	L54	
	CY7C185A-25DMB	D22	Military
	CY7C185A-25LMB	L54	
	CY7C185A-25KMB	K74	
35	CY7C185A-35PC	P21	Commercial
	CY7C185A-35VC	V21	
	CY7C185A-35DC	D22	
	CY7C185A-35LC	L54	
	CY7C185A-35DMB	D22	Military
	CY7C185A-35LMB	L54	
	CY7C185A-35KMB	K74	
45	CY7C185A-45PC	P21	Commercial
	CY7C185A-45VC	V21	
	CY7C185A-45DC	D22	
	CY7C185A-45LC	L54	
	CY7C185A-45DMB	D22	Military
	CY7C185A-45LMB	L54	
	CY7C185A-45KMB	K74	
55	CY7C185A-55PC	P21	Commercial
	CY7C185A-55VC	V21	
	CY7C185A-55DC	D22	
	CY7C185A-55LC	L54	
	CY7C185A-55DMB	D22	Military
	CY7C185A-55LMB	L54	
	CY7C185A-55KMB	K74	

Speed (ns)	Ordering Code	Package Type	Operating Range
20	CY7C186A-20PC	P15	Commercial
	CY7C186A-20DC	D16	
	CY7C186A-20DMB	P15	Military
25	CY7C186A-25PC	P15	Commercial
	CY7C186A-25DC	D16	
	CY7C186A-25DMB	D16	Military
35	CY7C186A-35PC	P15	Commercial
	CY7C186A-35DC	D16	
	CY7C186A-35DMB	D16	Military
45	CY7C186A-45PC	P15	Commercial
	CY7C186A-45DC	D16	
	CY7C186A-45DMB	D16	Military
55	CY7C186A-55PC	P15	Commercial
	CY7C186A-55DC	D16	
	CY7C186A-55DMB	D16	Military

Bit Map



Address Designators

Address Name	Address Function	Pin Number
A4	X3	2
A5	X4	3
A6	X5	4
A7	X6	5
A8	X7	6
A9	Y1	7
A10	Y4	8
A11	Y3	9
A12	Y0	10
A0	Y2	21
A1	X0	23
A2	X1	24

MILITARY SPECIFICATIONS

Group A Subgroup Testing

DC Characteristics

Parameters	Subgroups
V_{OH}	1, 2, 3
V_{OL}	1, 2, 3
V_{IH}	1, 2, 3
V_{IL} Max.	1, 2, 3
I_{IX}	1, 2, 3
I_{OZ}	1, 2, 3
I_{OS}	1, 2, 3
I_{CC}	1, 2, 3
I_{SB1}	1, 2, 3
I_{SB2}	1, 2, 3

Switching Characteristics

Parameters	Subgroups
READ CYCLE	
t_{RC}	7, 8, 9, 10, 11
t_{AA}	7, 8, 9, 10, 11
t_{OHA}	7, 8, 9, 10, 11
t_{ACE1}	7, 8, 9, 10, 11
t_{ACE2}	7, 8, 9, 10, 11
t_{DOE}	7, 8, 9, 10, 11
WRITE CYCLE	
t_{WC}	7, 8, 9, 10, 11
t_{SCE1}	7, 8, 9, 10, 11
t_{SCE2}	7, 8, 9, 10, 11
t_{AW}	7, 8, 9, 10, 11
t_{HA}	7, 8, 9, 10, 11
t_{SA}	7, 8, 9, 10, 11
t_{PWE}	7, 8, 9, 10, 11
t_{SD}	7, 8, 9, 10, 11
t_{HD}	7, 8, 9, 10, 11

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