HARRIS SEMICONDUCTOR

HS-26CT31RH

Radiation Hardened Quad Differential Line Driver

March 1995

Features

- 1.2 Micron Radiation Hardened CMOS
  - Total Dose Up to 300K RAD(Si)
- Latchup Free
- EIA RS-422 Compatible Outputs (Except for IOS)
- TTL Compatible Inputs
- High Impedance Outputs when Disabled or Powered Down
- Low Power Dissipation 2.75mW Standby (Max)
- Single 5V Supply
- Low Output Impedance 10Ω or Less
- Full -55°C to +125°C Military Temperature Range

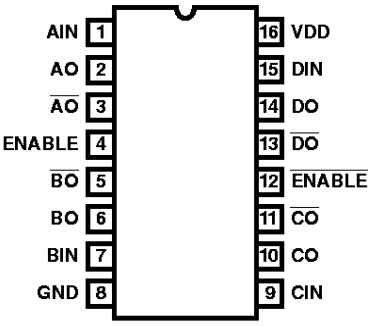
Description

The Harris HS-26CT31RH is a quad differential line driver designed for digital data transmission over balanced lines and meets the requirements of EIA standard RS-422. Radiation hardened CMOS processing assures low power consumption, high speed, and reliable operation in the most severe radiation environments.

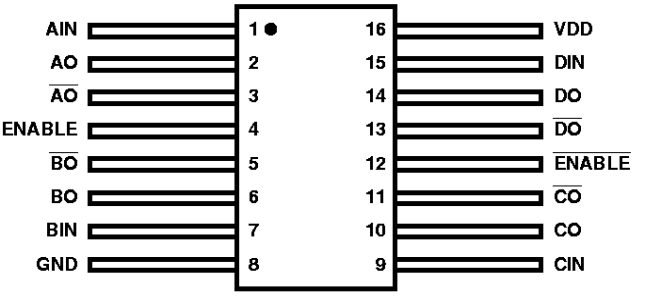
The HS-26CT31RH accepts TTL signal levels and converts them to RS-422 compatible outputs. This circuit uses special outputs that enable the drivers to power down without loading down the bus. Enable and disable pins allow several devices to be connected to the same data source and addressed independently.

Pinouts

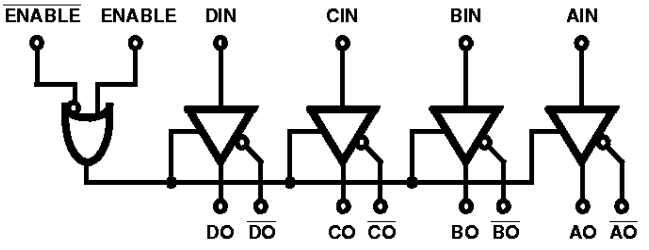
HS1-26CT31RH 16 LEAD CERAMIC SIDEBRAZE DIP
CASE OUTLINE D2, CONFIGURATION C
TOP VIEW



HS9-26CT31RH 16 LEAD FLATPACK
CASE OUTLINE F5A, CONFIGURATION B
TOP VIEW



Logic Diagram



TRUTH TABLE

DEVICE POWER ON/OFF	INPUTS			OUTPUT	
	ENABLE	ENABLE	IN	OUT	OUT
ON	0	1	X	HI-Z	HI-Z
ON	1	X	0	0	1
ON	X	0	0	0	1
ON	1	X	1	1	0
ON	X	0	1	1	0
OFF (0V)	X	X	X	HI-Z	HI-Z

Ordering Information

PART NUMBER	TEMPERATURE RANGE	SCREENING LEVEL	PACKAGE
HS1-26CT31RH-8	-55°C to +125°C	Harris Class B Equivalent	16 Lead Sidebraze DIP
HS1-26CT31RH-Q	-55°C to +125°C	Harris Class S Equivalent	16 Lead Sidebraze DIP
HS9-26CT31RH-8	-55°C to +125°C	Harris Class B Equivalent	16 Lead Flatpack
HS9-26CT31RH-Q	-55°C to +125°C	Harris Class S Equivalent	16 Lead Flatpack
HS1-26CT31RH/Sample	+25°C	Sample	16 Lead Sidebraze DIP
HS1-26CT31RH/Proto	-55°C to +125°C	Prototype	16 Lead Sidebraze DIP
HS9-26CT31RH/Sample	+25°C	Sample	16 Lead Flatpack
HS9-26CT31RH/Proto	-55°C to +125°C	Prototype	16 Lead Flatpack

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

Spec Number **518791**
File Number **2929.1**

Absolute Maximum Ratings

Supply Voltage . . . . . -0.5V to +7.0V
Input, Output or I/O Voltage . . . . . -0.5 to VDD+0.5V
Output Voltage with Power Off (0V) . . . . . -.5V to +7.0V
DC Diode Input Current (Any Input) . . . . . ±20mA
DC Drain Current (Any One Input) 350mA
DC VDD or Ground Current 400mA
Storage Temperature Range . . . . . -65°C to +150°C
Lead Temperature (Soldering 10s) . . . . . +300°C
ESD Classification . . . . . Class 1

Reliability Information

Thermal Resistance	θ_{JA}	θ_{JC}
DIP Package	75°C/W	16°C/W
Flatpack Package	95°C/W	24°C/W

Maximum Package Power Dissipation at +125°C
For T = -55°C to +100°C 1W
For T = +100°C to +125°C, Derate Linearly at
DIP Package . . . . . 13.3mW/°C
Flatpack Package . . . . . 10.5mW/°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Operating Conditions

Operating Voltage Range . . . . . +4.5V to +5.5V
Operating Temperature Range . . . . . -55°C to +125°C
Input Rise and Fall Time . . . . . 500ns Max
Input Low Voltage (VIL) . . . . . 0V to 0.8V Max
Input High Voltage (VIH) . . . . . VDD to VDD/2V Min

TABLE 1. DC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	(NOTE 1) CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
High Level Output Voltage	VOH	VDD = 4.5V, and 5.5V IO = -20mA (Notes 2, 6)	1, 2, 3	-55°C, +25°C, +125°C	2.5	-	V
Low Level Output Voltage	VOL	VDD = 4.5V and 5.5V IO = 20mA (Notes 2, 6)	1, 2, 3	-55°C, +25°C, +125°C	-	0.5	V
Differential Output Voltage	VT, $\overline{VT}$	VDD = VIH = 4.5V, VIL = 0V, RL = R1 + R2 (Note 3)	1, 2, 3	-55°C, +25°C, +125°C	2.0	-	V
Difference in Differential Output	|VT| - |$\overline{VT}$|	VDD = VIH = 4.5V, VIL = 0V, RL = R1 + R2 (Note 3)	1, 2, 3	-55°C, +25°C, +125°C	-	0.4	V
Common Mode Output Voltage	VOS, $\overline{VOS}$	VDD = VIH = 4.5V, VIL = 0V, RL = R1 + R2 (Note 3)	1, 2, 3	-55°C, +25°C, +125°C	-	3.0	V
Difference in Common Mode Output	|VOS - VOS|	VDD = VIH = 4.5V, VIL = 0V, RL = R1 + R2 (Note 3)	1, 2, 3	-55°C, +25°C, +125°C	-	0.4	V
High Level Input Voltage	VIH	VDD = 4.5V, 5.5V (Note 5)	1, 2, 3	-55°C, +25°C, +125°C	VDD/ 2.0	-	V
Low Level Input Voltage	VIL	VDD = 4.5V, 5.5V (Note 5)	1, 2, 3	-55°C, +25°C, +125°C	-	0.8	V
Standby Supply Current	IDDSB	VDD = 5.5V, Output = Open VIN = VDD or GND	1, 2, 3	-55°C, +25°C, +125°C	-	500	µA
Three-State Output Leakage Current	IOZ	VDD = 5.5V, Force Voltage = 0V or VCC (Note 7)	1, 2, 3	-55°C, +25°C, +125°C	-	±5	µA
Delta Supply Current	ΔICC	VDD = 5.5V, VIN = 2.4V, 0.5V	1, 2, 3	-55°C, +25°C, +125°C	-	2.0	mA
Input Leakage	IIN	VDD = 5.5V, VIN = VDD or GND	1, 2, 3	-55°C, +25°C, +125°C	-	±1.0	µA
Output Leakage Current Power OFF	IOFF	VDD = 0V, VOUT = 6V, -250mV, Inputs = GND	1, 2, 3	-55°C, +25°C, +125°C	-100	100	µA

TABLE 1. DC ELECTRICAL PERFORMANCE CHARACTERISTICS (Continued)

PARAMETER	SYMBOL	(NOTE 1) CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Input Clamp Voltage	VIC	At -1.0mA	1, 2, 3	-55°C, +25°C, +125°C	-	-1.5	V
		At +1.0mA	1, 2, 3	-55°C, +25°C, +125°C	-	+1.5	V

NOTES:

1. All voltages referenced to device ground.
2. Force/Measure functions may be interchanged.
3. These test conditions are detailed in EIA specification RS-422. (R1 = R2 = 50Ω.)
4. Only one input pin set up to VIN per test. All other pins set to VCC or GND.
5. This parameter tested as inputs levels in VOL/VOH, IOZ, functional test.
6. VIL = 0.8V, VIH = VCC/2.
7. The inputs are conditioned to have the output in the opposite state of the forcing IOZ condition.

TABLE 2. AC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	(NOTES 1, 2) CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Propagation Delay	TPLH, TPHL	VDD = 4.5V	9, 10, 11	-55°C, +25°C, +125°C	2	22	ns
Propagation Delay	TPZH	VDD = 4.5V	9, 10, 11	-55°C, +25°C, +125°C	5	28	ns
Propagation Delay	TPZL	VDD = 4.5V	9, 10, 11	-55°C, +25°C, +125°C	5	28	ns
Propagation Delay	TPHZ	VDD = 4.5V	9, 10, 11	-55°C, +25°C, +125°C	2	22	ns
Propagation Delay	TPLZ	VDD = 4.5V	9, 10, 11	-55°C, +25°C, +125°C	2	22	ns
Rise and Fall Times	TTHL, TTLH	VDD = 4.5V	9, 10, 11	-55°C, +25°C, +125°C	1	10	ns
Output Skew	TSKEW (Note 3)	VDD = 4.5V, RL = 100Ω, CL = 40pF	9, 10, 11	-55°C, +25°C, +125°C	-	3	ns

NOTES:

1. All voltages referenced to device ground.
2. See Table EIA RS-422
3. Skew is defined as the difference in propagation delays between complementary outputs at the 50% point.

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	(NOTE 1) CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Input Capacitance	CIN	VDD = Open, f = 1MHz	1	-55°C, +25°C, +125°C	-	12	pF
Output Capacitance	COUT	VDD = Open, f = 1MHz	1	-55°C, +25°C, +125°C	-	12	pF
Operating Short Circuit	IOS	VDD = 5.5V, VIN = VDD or GND, VOUT = 0V	2	-55°C, +25°C, +125°C	-30	-150	mA
On-State Resistance	RON	VDD = 4.5V, VOUT = 1.5V, VIN = VDD or GND	1	-55°C, +25°C, +125°C	-	10	Ω

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS (Continued)

PARAMETER	SYMBOL	(NOTE 1) CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Dynamic Current	IDYN	VCC = 4.5V, FQ = 1MHz, VIN = VCC or GND,	1, 5	+125°C, +25°C	Typical 3		mA
Power Dissipation Capacitance	CPD	VCC = 4.5V, FQ = 1MHz	1, 4	+25°C	Typical 170		pF

NOTES:

1. Parameters listed in Table 3 are controlled via design or process parameters and are not directly tested. These parameters are characterized upon initial design and after major design or process changes that affect these parameters.
2. Only one output at a time may be shorted.
3. Power Up/Down Feature: Outputs will remain in the Hi-Z state with VDD ≤ 2.5V and become active at VDD ≥ 4.0V. The active output state will be determined by the input conditions.
4. This parameter is a per channel measurement.
5. This parameter measured with a 100pF load. One channel only.

TABLE 4. POST IRRADIATION ELECTRICAL PERFORMANCE CHARACTERISTICS

The post irradiation electrical performance characteristics are the same as the parameters listed in Tables 1, 2.

TABLE 5. BURN-IN DELTA PARAMETERS (+25°C) AND GROUP B, SUBGROUP 5 DELTA PARAMETERS

PARAMETER	SYMBOL	DELTA LIMITS
Standby Supply Current	IDDSB	±100µA
Three-State Output Leakage Current	IOZ	±1.0µA
Low Level Output Voltage	VOL	±60mV
High Level Output Voltage	VOH	±150mV
Input Leakage Current	IIL, IIH	±150nA

TABLE 6. APPLICABLE SUBGROUPS

CONFORMANCE GROUPS		METHOD	-Q SUBGROUPS	READ AND RECORD
Initial Test (Pre Burn-In)		100%/5004	1, 7, 9	See Table 5
Interim Test I (Post Burn-In)		100%/5004	1, 7, 9	See Table 5
Interim Test II (Post Burn-In)		100%/5004	1, 7, 9	See Table 5
PDA		100%/5004	1, 7, 9, Δ	-
Interim Test III (Post-Burn-In)		100%/5004	1, 7, 9	See Table 5
PDA		100%/5004	1, 7, 9, Δ	-
Final Test		100%/5004	2, 3, 8A, 8B, 10, 11	-
Group A		Samples/5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11	-
Group B	B5	Samples/5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11, Δ	Subgroups 1, 2, 3, 9, 10, 11
	B6	Samples/5005	1, 7, 9	-
Group D		Samples/5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11	-

TABLE 6A. APPLICABLE SUBGROUPS

CONFORMANCE GROUPS	METHOD	-8 SUBGROUPS
Initial Test (Pre Burn-In)	100%/5004	1, 7, 9
Interim Test (Post-Burn-In)	100%/5004	1, 7, 9
PDA	100%/5004	1, 7, 9
Final Test	100%/5004	2, 3, 8A, 8B, 10, 11

TABLE 6A. APPLICABLE SUBGROUPS (Continued)

CONFORMANCE GROUPS		METHOD	-8 SUBGROUPS
Group A		Samples/5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11
Group C	C-1	Samples/5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11
Group D		Samples/5005	1, 7, 9

TABLE 7. TOTAL DOSE IRRADIATION

CONFOMRANCE GROUPS	METHOD	TEST		READ AND RECORD	
		PRE-RAD	POST-RAD	PRE-RAD	POST-RAD
Group E Subgroup 2	5005	1, 7, 9	Table 4	1, 7, 9	Table 4

TABLE 8. BURN-IN TEST CONNECTIONS (+125°C < T_A < 139°C, VCC = 6V, ±0.5V)

TEST	OPEN	GROUND	VDD	1/2VDD	50KHz	25KHz
Static Burn-In I	2, 3, 5, 6, 10, 11, 13, 14	1, 4, 7, 8, 9, 12, 15	16	-	-	-
Static Burn-In II	2, 3, 5, 6, 10, 11, 13, 14	8	1, 4, 7, 9, 12, 15, 16	-	-	-
Dynamic Burn-In	-	8, 12	4, 16	2, 3, 5, 6, 10, 11, 13, 14	1, 7, 9, 15	-

NOTE: Each pin except for VDD and Ground will have a series resistor as specified below.

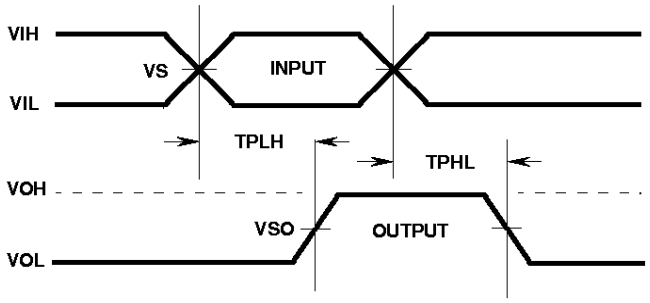
Static Burn-In	Dynamic Burn-In
10kΩ ± 5%	200Ω ± 5%

TABLE 9. IRRADIATION TEST CONNECTIONS (T_A = +25°C, ±5°C, VDD = 5V, ±10%)

TEST	OPEN	GROUND	VDD	1/2VDD	50KHz	25KHz
Radiation Exposure	2, 3, 5, 6, 10, 11, 13, 14	8	1, 4, 7, 9, 12, 15, 16	-	-	-

NOTE: Each pin except for VDD and Ground will have a 47kΩ resistor ±5%.

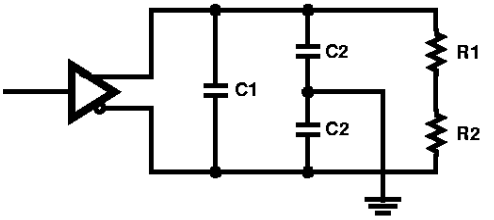
Propagation Delay Timing Diagram



AC VOLTAGE LEVELS

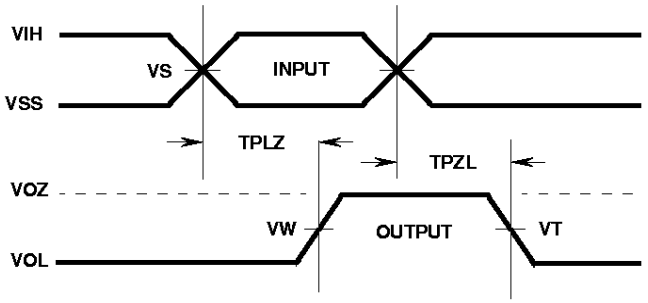
PARAMETER	HS-26CT31RH	UNITS
VDD	4.50	V
VIH	3.00	V
VS	1.30	V
VIL	0	V
GND	0	V
VSO	50	%

Propagation Delay Load Circuit



C1 = C2 = C3 = 40pF
R1 = R2 = 50Ω

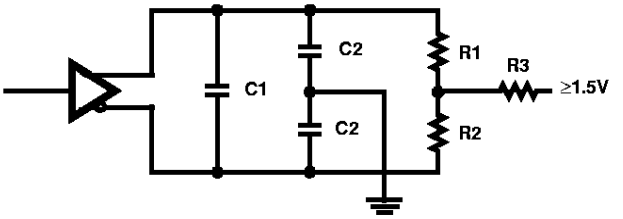
Three-State Low Timing Diagrams



THREE–STATE LOW VOLTAGE LEVELS

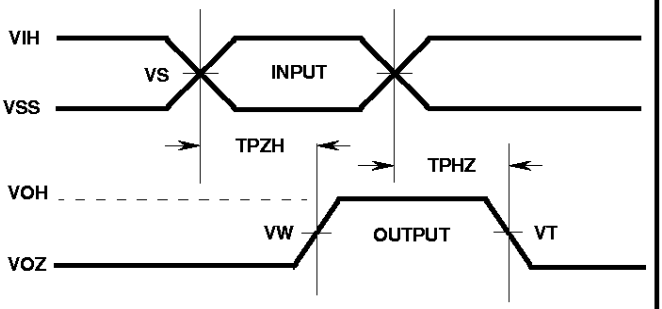
PARAMETER	HS-26CT31RH	UNITS
VDD	4.50	V
VIH	3.00	V
VS	1.30	V
VW	VOL + 0.3	V
VT	0.80	V

Three-State Low Load Circuit



C1 = C2 = C3 = 40pF
R1 = R2 = 50Ω
R3 = 500Ω

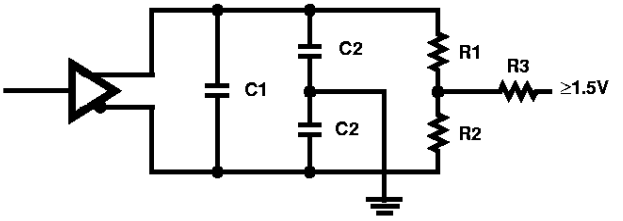
Three-State High Timing Diagrams



THREE-STATE HIGH VOLTAGE LEVELS

PARAMETER	HS-26CT31RH	UNITS
VDD	4.50	V
VIH	3.00	V
VS	1.30	V
VT	VOH - 0.3	V
VW	2.00	V

Three-State High Load Circuit



C1 = C2 = C3 = 40pF
R1 = R2 = 50Ω
R3 = 500Ω

Harris - Space Level Product Flow -Q

Wafer Lot Acceptance (All Lots) Method 5007 (Includes SEM)

Radiation Verification (Each Wafer) Method 1019, 300k RAD (Si), 4 Samples/Wafer, 0 Rejects

100% Nondestructive Bond Pull Method 2023

100% Internal Visual Inspection Method 2010

100% Temperature Cycling Method 1010 Condition C

100% Constant Acceleration

100% Particle Impact Noise Detection Testing

100% External Visual Inspection

100% Serialization

100% Initial Electrical Test

100% Static Burn-In1: 24 Hour, +125°C Min, Method 1015

100% Interim Electrical Test 1 (Note 1)

100% Static Burn-In 2: 24 Hour, +125°C Min, Method 1015

100% Interim Electrical Test 2 (Note 1)

100% Dynamic Burn-In 240 Hour, +125°C or Equivalent, Method 1015

100% Interim Electrical 3 (Note 1)

100% Final Electrical Test

100% Fine and Gross Seal Method 1014

100% Radiographics Method 2012 (2 Views)

100% External Visual Method 2009

Group A (All Tests) Method 5005 (Class S)

Group B (Optional) Method 5005 (Class S) (Note 2)

Group D (Optional) Method 5005 (Class S) (Note 2)

CSI and/or GSI (Optional (Note 2)

Data Package Generation (Note 3)16

NOTES:

1. Failure from interim electrical tests 1 and 2 are combined for determining PDA (PDA = 5% for subgroups 1, 7, 9 and delta failures combined, PDA = 3% for subgroup 7 failures). Interim electrical tests 3 PDA (PDA = 5% for subgroups 1, 7, 9 and delta failures combined, PDA = 3% for subgroup 7 failures).
2. These steps are optional, and should be listed on the purchase order if required.
3. Data Package Contents:
   Cover Sheet (P.O. Number, Customer Number, Lot Date Code, Harris Number, Lot Number, Quantity).
   Certificate of Conformance (as found on shipper).
   Lot Serial Number Sheet (Good Unit(s) Serial Number and Lot Number).
   Variables Data (All Read, Record, and delta operations).
   Attribute Summary from Post Seal through Final Test.
   Group A Attributes Data Summary.
   Wafer Lot Acceptance Report (Method 5007) to include SEM photos. NOTE: SEM photos to include % of step coverage.
   X-Ray Report and File(s), including parameter measurements.
   GAMMA Radiation Report with initial shipment of devices from the same wafer lot; containing a Cover Page, Disposition, Rad Dose, Lot Number, Test Package, Spec Number(s), Test Equipment, etc. Irradiation Read and Record data will be on file at Harris.

Harris -8 Product Flow

Internal Visual Inspection

Gamma Radiation Assurance Tests Method 1019

Customer Pre-Cap Visual Inspection (Notes 1, 2)

Temperature Cycling Method 1010 Condition C (50 Cycles)

Constant Acceleration Method 2001 Y1 30KG

Fine and Gross Leak Tests Method 1014

Marking

Initial Electrical Tests (T0)

Dynamic Burn-In 160 Hours, +125°C Method 1015 or Equivalent Condition D

Electrical Tests Subgroups 1, 7, 9 (T1) Method 5004

PDA Calculation 5% Subgroups 1, 7 Method 5004

Electrical Test +125°C, -55°C Method 5004

Group A Inspection Method 5005

Customer Source Inspection (Note 2)

Group B Inspection (Notes 2, 4) Method 5005 (Optional)

Group C Inspection (Notes 2, 4) Method 5005 (Optional)

Group D Inspection (Notes 2, 4) Method 5005 (Optional)

External Visual Inspection Method 2009

Data Package Generation (Note 3)

NOTES:

1. Visual inspection is performed to MIL-STD-883 Method 2010, Condition B.
2. These steps are optional, and should be listed on the purchase order if required.
3. Data Package Contents:
   Test Attributes (including Group A) -55°C, +25°C, +125°C
   Radiation Testing Certificate of Conformance
4. Group B, C and D data package contains Attributes Data only.

Metallization Topology

DIE DIMENSIONS:
87 mils x 188 mils
(2219µm x 4770µm)

METALLIZATION:
M1: Mo/Tiw
Thickness: 5800Å
M2: Al/Si/Cu
Thickness:10kÅ ± 1kÅ

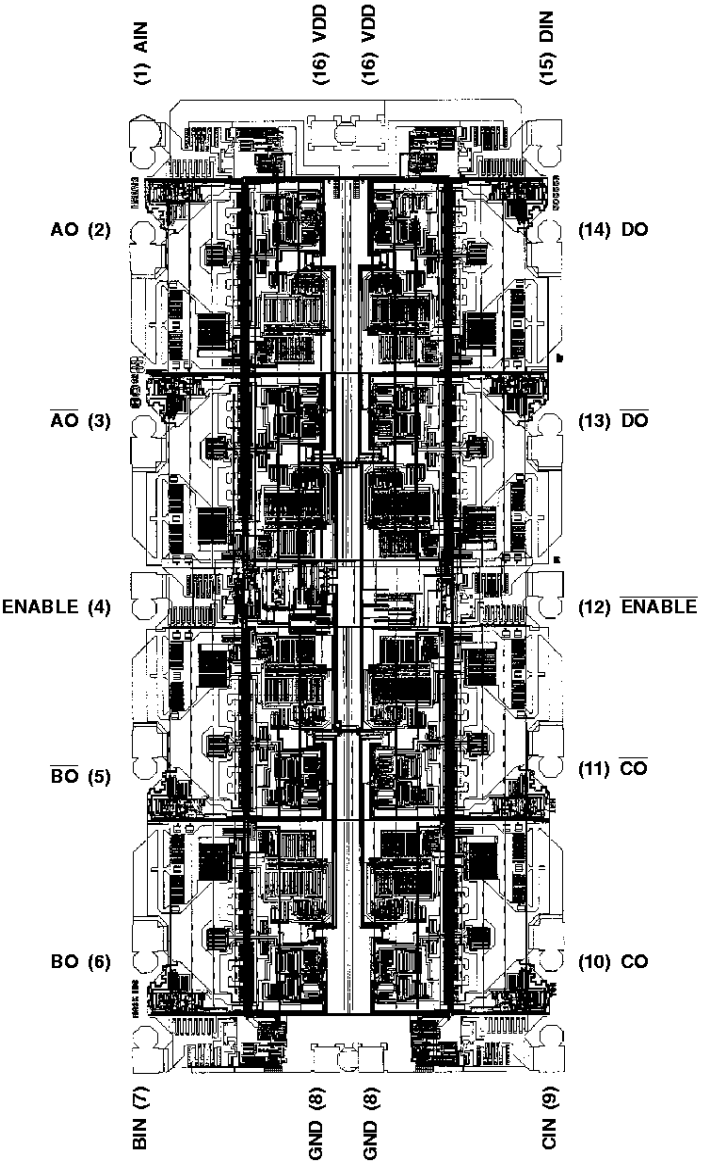
GLASSIVATION:
Type: SiO_2
Thickness: 10kÅ ± 1kÅ

WORST CASE CURRENT DENSITY:
$<2.0 \times 10^5 A/cm^2$

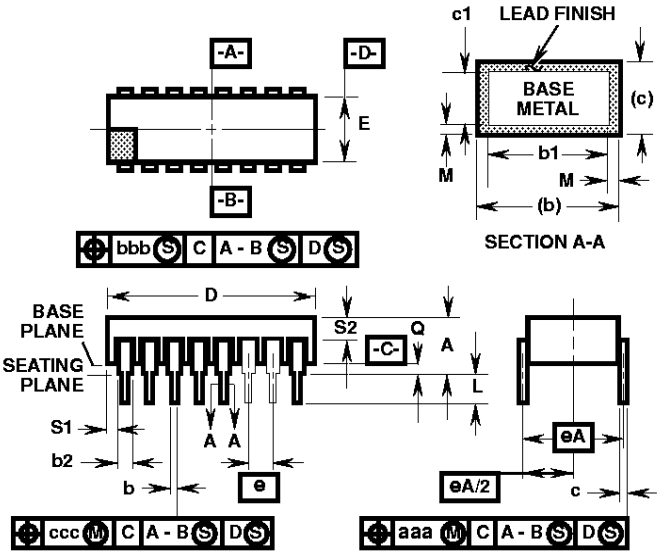
BOND PAD SIZE: 110µm x 100µm

Metallization Mask Layout

HS-26CT31RH



Ceramic Dual-In-Line Metal Seal Packages (SBDIP)



D16.3 MIL-STD-1835 CDIP2-T16 (D-2, CONFIGURATION C)
16 LEAD CERAMIC DUAL-IN-LINE METAL SEAL PACKAGE

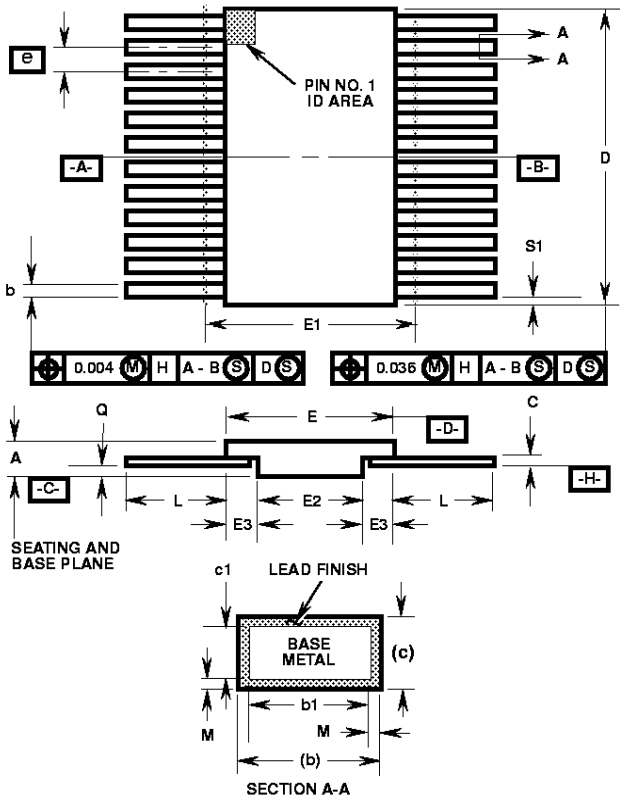
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.200	-	5.08	-
b	0.014	0.026	0.36	0.66	2
b1	0.014	0.023	0.36	0.58	3
b2	0.045	0.065	1.14	1.65	-
b3	0.023	0.045	0.58	1.14	4
c	0.008	0.018	0.20	0.46	2
c1	0.008	0.015	0.20	0.38	3
D	-	0.840	-	21.34	-
E	0.220	0.310	5.59	7.87	-
e	0.100 BSC		2.54 BSC		-
eA	0.300 BSC		7.62 BSC		-
eA/2	0.150 BSC		3.81 BSC		-
L	0.125	0.200	3.18	5.08	-
Q	0.015	0.060	0.38	1.52	5
S1	0.005	-	0.13	-	6
S2	0.005	-	0.13	-	7
α	90^o	105^o	90^o	105^o	-
aaa	-	0.015	-	0.38	-
bbb	-	0.030	-	0.76	-
ccc	-	0.010	-	0.25	-
M	-	0.0015	-	0.038	2
N	16		16		8

Rev. 0 4/94

NOTES:

1. Index area: A notch or a pin one identification mark shall be located adjacent to pin one and shall be located within the shaded area shown. The manufacturer's identification shall not be used as a pin one identification mark.
2. The maximum limits of lead dimensions b and c or M shall be measured at the centroid of the finished lead surfaces, when solder dip or tin plate lead finish is applied.
3. Dimensions b1 and c1 apply to lead base metal only. Dimension M applies to lead plating and finish thickness.
4. Corner leads (1, N, N/2, and N/2+1) may be configured with a partial lead paddle. For this configuration dimension b3 replaces dimension b2.
5. Dimension Q shall be measured from the seating plane to the base plane.
6. Measure dimension S1 at all four corners.
7. Measure dimension S2 from the top of the ceramic body to the nearest metallization or lead.
8. N is the maximum number of terminal positions.
9. Braze fillets shall be concave.
10. Dimensioning and tolerancing per ANSI Y14.5M - 1982.
11. Controlling dimension: INCH.

Ceramic Metal Seal Flatpack Packages (Flatpack)



K16.A MIL-STD-1835 CDFP4-F16 (F-5A, CONFIGURATION B)
16 LEAD CERAMIC METAL SEAL FLATPACK PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.045	0.115	1.14	2.92	-
b	0.015	0.022	0.38	0.56	-
b1	0.015	0.019	0.38	0.48	-
c	0.004	0.009	0.10	0.23	-
c1	0.004	0.006	0.10	0.15	-
D	-	0.440	-	11.18	3
E	0.245	0.285	6.22	7.24	-
E1	-	0.315	-	8.00	3
E2	0.130	-	3.30	-	-
E3	0.030	-	0.76	-	7
e	0.050 BSC		1.27 BSC		-
k	0.008	0.015	0.20	0.38	2
L	0.250	0.370	6.35	9.40	-
Q	0.026	0.045	0.66	1.14	8
S1	0.005	-	0.13	-	6
M	-	0.0015	-	0.04	-
N	16		16		-

Rev. 1 2-20-95

NOTES:

1. Index area: A notch or a pin one identification mark shall be located adjacent to pin one and shall be located within the shaded area shown. The manufacturer's identification shall not be used as a pin one identification mark. Alternately, a tab (dimension k) may be used to identify pin one.
2. If a pin one identification mark is used in addition to a tab, the limits of dimension k do not apply.
3. This dimension allows for off-center lid, meniscus, and glass overrun.
4. Dimensions b1 and c1 apply to lead base metal only. Dimension M applies to lead plating and finish thickness. The maximum limits of lead dimensions b and c or M shall be measured at the centroid of the finished lead surfaces, when solder dip or tin plate lead finish is applied.
5. N is the maximum number of terminal positions.
6. Measure dimension S1 at all four corners.
7. For bottom-brazed lead packages, no organic or polymeric materials shall be molded to the bottom of the package to cover the leads.
8. Dimension Q shall be measured at the point of exit (beyond the meniscus) of the lead from the body. Dimension Q minimum shall be reduced by 0.0015 inch (0.038mm) maximum when solder dip lead finish is applied.
9. Dimensioning and tolerancing per ANSI Y14.5M - 1982.
10. Controlling dimension: INCH.